Version DMH/4

EGT3
ENGINEERING TRIPOS PART IIB

Monday 28 April 2014   2 to 3.30

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Supplementary page: one extra copy of Fig. 1 (Question 1).
Engineering Data Book

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Outline briefly the advantages and disadvantages of complementary metal oxide semiconductor (CMOS) technology, and explain why silicon-based technology dominates over other semiconductors. [20%]

(b) Figure 1 shows layouts of two different CMOS gates using n-well technology and a p-type substrate, with power supply V_{DD} labelled A, and power supply V_{SS} labelled B.

(i) Explain the operation of each gate and the logic functions of the connections P, Q, R, S, T and U. [10%]

(ii) On the supplementary copy of Fig. 1, label which regions are implanted with p-type impurities and which regions are implanted n-type. Draw on that copy a possible location for the n-type well, and shade in the active regions of all of the n-channel transistors. [10%]

(iii) Taking measurements from Fig. 1, calculate the ratio r_{NP} of the widths of the n-channel to the p-channel transistors in each of the logic gates in Fig. 1. [10%]

(c) Taking the electron mobility in silicon to be twice as large as the hole mobility, comment on the switching performance of each of the logic gates in Fig. 1. For incorporation into a general purpose logic circuit, calculate the optimum design value ratio for r_{NP} to maximize the switching speed. [20%]

(d) Outline why the performance of CMOS circuits improves when the minimum lithographic linewidth is reduced. With reference to Fig. 1, explain which dimensions are most important in determining circuit performance. Comment briefly on possible limitations in CMOS circuit performance as the available fabrication technology is projected to improve over the next decade. [30%]

An additional copy of Fig. 1 is attached to the back of this paper. It should be detached and handed in with your answers.

(cont.

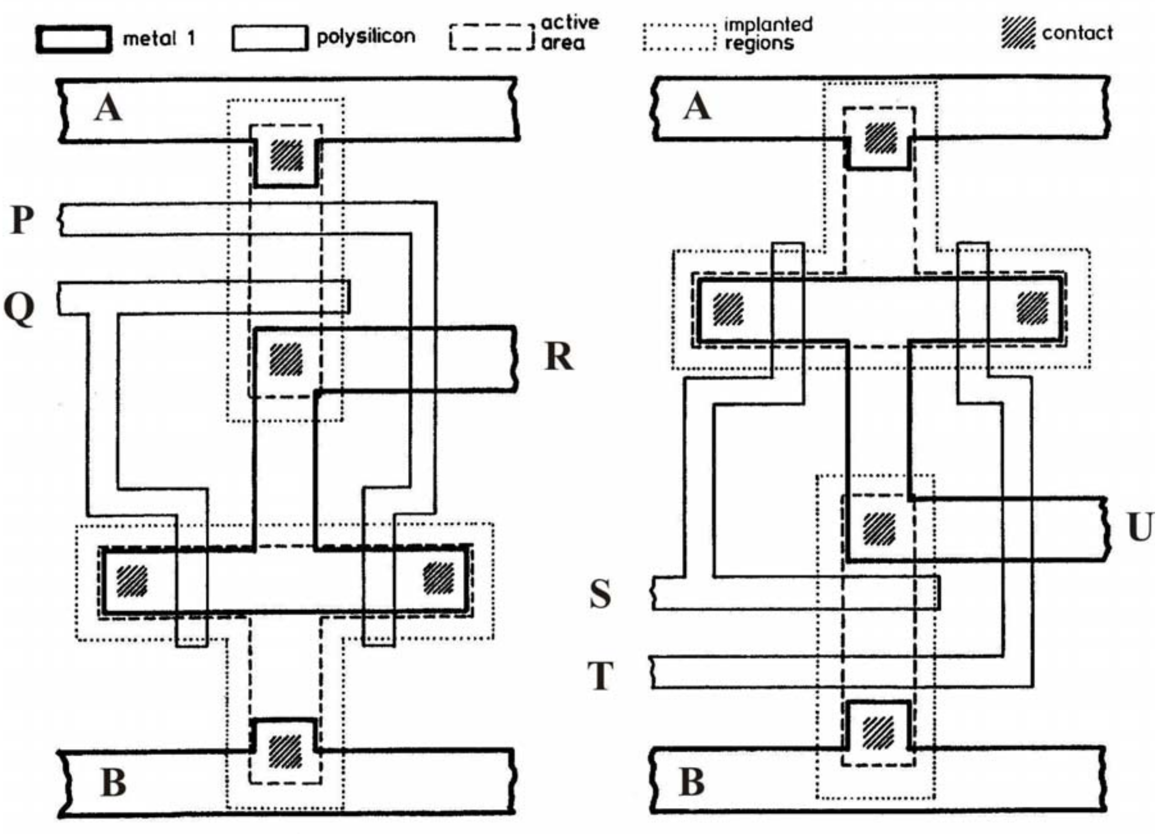
metal 1
polysilicon
active area
implanted regions
contact
A
P
Q
R
B
A
U
S
T
B

Fig. 1

2 (a) Give two main advantages and two disadvantages of the Silicon-On-Insulator (SOI) technology compared to bulk silicon technology. [20%]

(b) Describe schematically the process steps involved in producing:

(i) wafer bonded;

(ii) Smart-Cut (Unibond) SOI wafers.

Use drawings to exemplify the steps. What are the advantages and drawbacks of the two technological approaches against each other? [30%]

(c) Describe two main failure mechanisms associated with dielectrics in IC technology. Explain ways to differentiate between them. [20%]

(d) Draw a diagram of the bath-tub curve that describes the three parts of the failure rate curve of typical VLSI products, and annotate the diagram with:

(i) the nature and distribution of the various failures, and

(ii) two examples of the various failure mechanisms in each part of the overall failure curve. [30%]

3 (a) What is meant by the term *design rule* in CMOS integrated circuit layout? Write a short account of the ways in which design rules constrain the general form and dimensions of interconnect and contact structures in CMOS technologies. [60%]

(b) Show how the following structures and phenomena affect or give rise to specific design rules:

(i) self-aligned process;

(ii) contact cut;

(iii) process-induced gate-oxide damage;

(iv) electromigration. [40%]

In your account indicate the origins of the rules you introduce, making it clear how they arise from physical, electrical or processing constraints. Note: details of specific manufacturers' rules are not required.

(TURN OVER

4 (a) With the aid of a diagram, identify the various contributions to parasitic capacitance observed in a MOS transistor, and describe their origin. Explain how these contributions depend on:

(i) area,

(ii) perimeter, and

(iii) electrical potential

of the gate, drain and source electrodes. [50%]

(b) A simplified plan view (not to scale) showing a CMOS inverter and associated interconnect structures is presented in Fig. 2(a). The polysilicon interconnect and gate electrode are 1 μm wide, and the metal interconnect is 2 μm wide. Interconnect lengths are shown in the figure. The active regions each have dimensions 2 μm × 10 μm.

Figure 2(b) is a table of information abstracted from the manufacturer's data about the process in use, and consists of specific capacitance values per unit area or per unit length. Using the data supplied, determine as accurately as possible the key capacitances at zero bias for this logic inverter at the output terminal, assuming no other devices are connected. You may ignore the effects of contact structures for the purpose of this calculation. [40%]

Indicate qualitatively how these capacitances would be expected to change if normal device operating voltages were applied. State any assumptions made. [10%]

(cont.

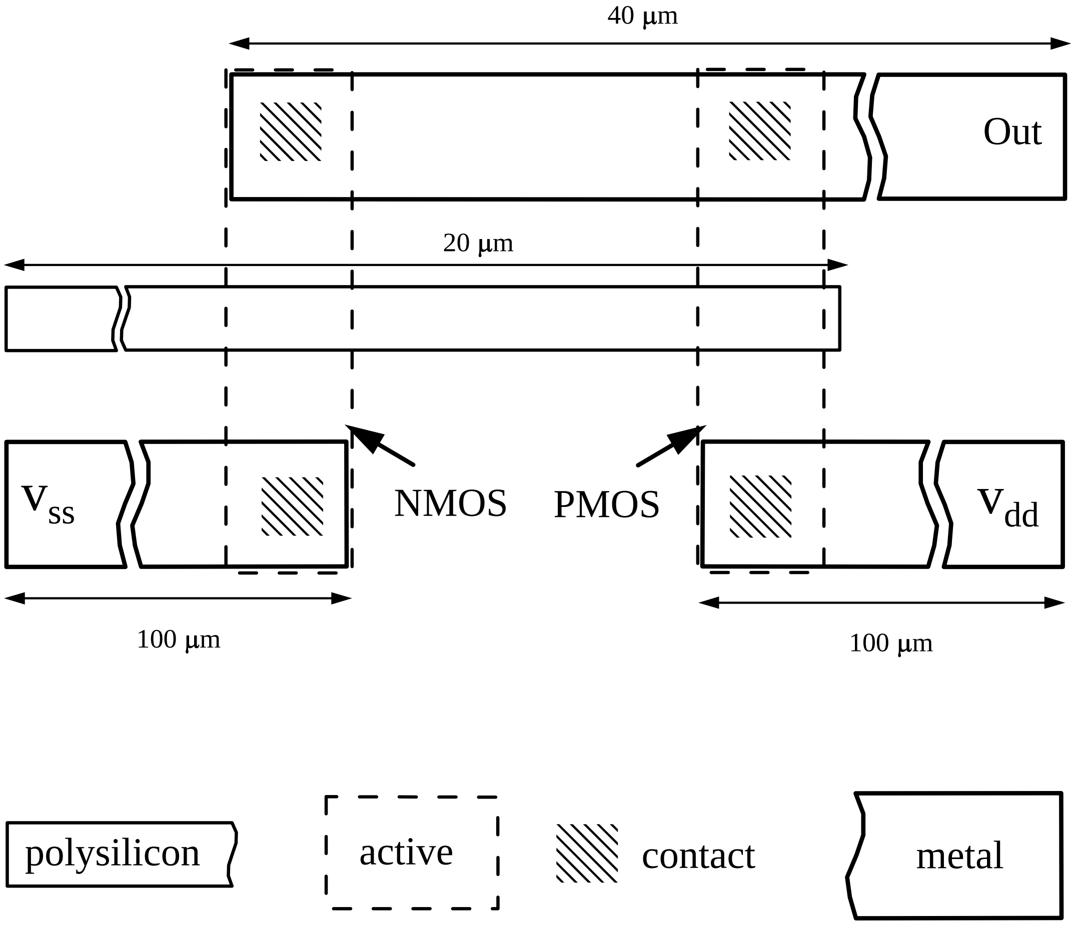

Fig. 2a

Parameter	Value	Unit	Description
C_O	7×10^{-4}	Fm^{-2}	Capacitance associated with gate oxide dielectric
C_{JA0}	1×10^{-4}	Fm^{-2}	Area capacitance to substrate (source or drain)
C_{JP0}	4×10^{-10}	Fm^{-1}	Peripheral capacitance to substrate (source or drain)
C_{GD0}	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with drain
C_{GS0}	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with source
C_{MA}	3×10^{-5}	Fm^{-2}	Area capacitance to substrate of metal over field oxide
C_{MP}	4×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of metal over field oxide
C_{PA}	4×10^{-5}	Fm^{-2}	Area capacitance to substrate of polysilicon over field oxide
C_{PP}	5×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of polysilicon over field oxide

Fig. 2b

 (TURN OVER

5 (a) Describe briefly how *ring oscillator* circuits can be used to measure nanosecond gate delays despite the relatively large time delays associated with bringing signals on- and off-chip. Explain how ring resonances have the potential to give misleading results. Briefly outline any other limitations of this approach to characterisation of logic gate performance. Discuss whether or not a simple ring oscillator design can give a realistic measurement of practical circuit delays. [50%]

(b) Discuss quality, cost, delivery and service as critical factors for the successful manufacture of integrated circuits. [25%]

(c) Describe some of the processes required before a manufacturing line can be approved for the production of quality-assured VLSI products. [25%]

END OF PAPER

Version DMH/4 Candidate Number:

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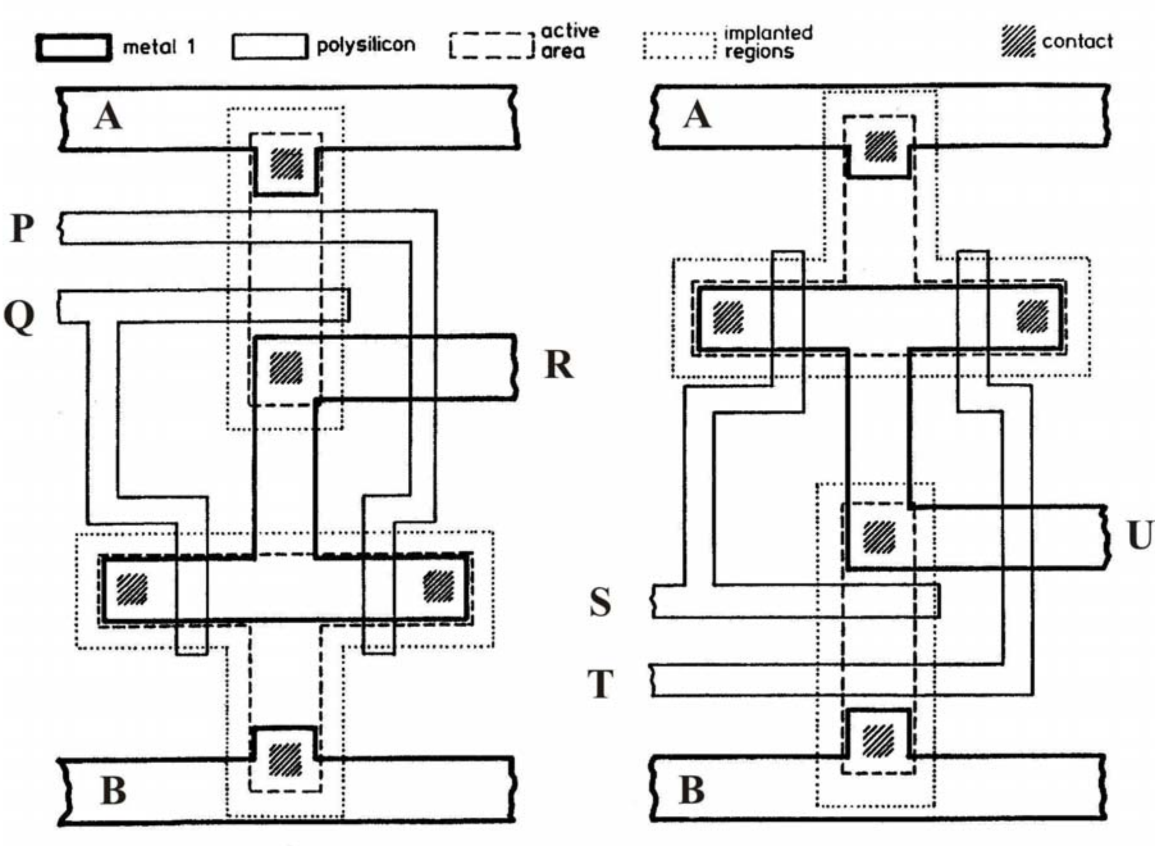
Monday 28 April 2014, Module 4B7, Question 1



Extra copy of Fig. 1, for Question 1
(may be handed in with your script)

4B7 VLSI Design, Technology and CAD - 2014 Numerical Answers

1.

2.

3.

4. Cout = 20 fF

5.