Version AJF/2

EGT3
ENGINEERING TRIPOS PART IIB

Friday 02 May 2014 2 to 3.30

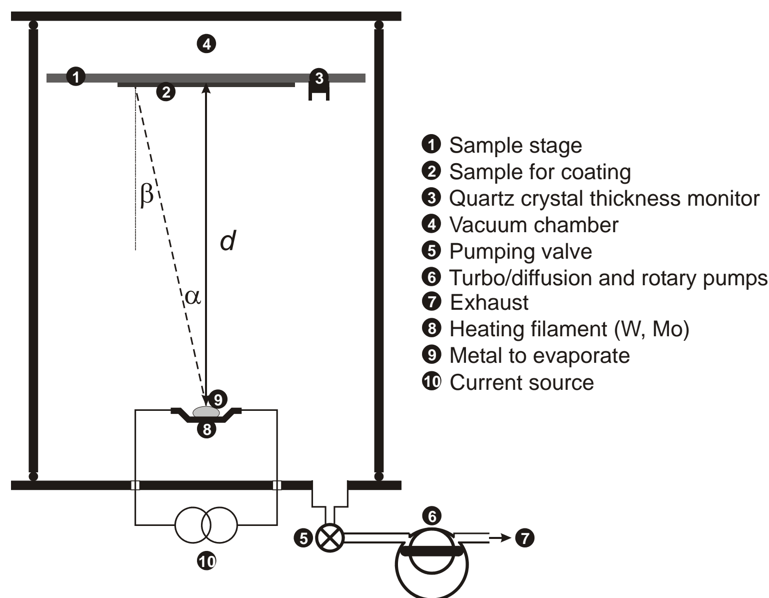
Module 4M6

MATERIALS AND PROCESSES FOR MICROSYSTEMS (MEMS)

ANSWERS

1 (a) Thermal evaporation is a popular method for producing thin metallic layers due to its simplicity. The metal to be deposited is placed on a metal filament (normally W or Mo with a much higher melting point) inside a vacuum chamber which is held at a pressure below 10^{-4} Pa. A current is passed through the filament, which heats up causing the metal to evaporate. The metal condenses in a thin film which is mounted above the metal source.

A high vacuum is required in thermal evaporation to ensure than contamination of the metal layer is minimised. The source to substrate distance should be small compared with the mean free path in the vacuum. The time required for a monolayer of the residual vacuum material to hit the substrate surface should be long compared with the time for a monolayer of material to be evaporated. Evaporation produces generally amorphous metallic layers, frequently with a high surface roughness.



Evaporation results in 'line of sight' deposition from what is essentially a point source of evaporating metal. Evaporation therefore gives very poor step edge coverage, which is an issue with coating patterned layers. The kinetic energy associated with depositing atoms is very low (~0.1 eV) so there is little possibility of damage to a photoresist layer, although thermal damage from the filament should be considered.

(b) (i) We know that the thickness of the evaporated film is non-uniform will decrease towards the edge of the substrate as

$$R \sim \frac{\cos^2 \theta}{d^2}$$

from equation 5.3 of the *4M6 Data Book*. The distance from the filament to the edge of the substrate is

$$d_{max} = \sqrt{d^2 + (\phi/2)^2} = \sqrt{0.4^2 + 0.075^2} = 0.407 \text{ m}$$

where the diameter of the substrate is ϕ. Hence, assuming that deposition is uniform over a hemisphere from the filament, the volume of material being deposited is

$$V = 2\pi d_{max}^2 .t = 2\pi \times 0.407^2 \times 100 \times 10^{-9} = 1.04 \times 10^{-7} \text{ m}^3$$

Therefore, the mass of aluminium required is

$$m = \rho V = 2643 \times 1.04 \times 10^{-7} = \underline{275 \text{ mg}}$$

(ii) If d is the separation of the filament and substrate, then

$$\cos\theta = \frac{d}{d_{max}}$$

and the ratio of the thickness of material at the edge of the substrate to the centre is

$$\frac{t_0}{t_\phi} \sim \frac{1}{d^2} \Big/ \frac{\cos^2\theta}{d_{max}^2} = \frac{1}{d^2} \Big/ \frac{d^2}{d_{max}^4} = \frac{d_{max}^4}{d^4} = \left(\frac{0.407}{0.400}\right)^4 = 1.072$$

Hence

$$t_0 = 1.072 \times 120 = \underline{128.6 \text{ nm}}$$

(iii) Alternative methods include electron beam heating, laser heating (both of which have the advantage of reduced contamination and reduced sample heating as the crucible is not significantly heated) and rf induction heating (which has the advantage of not requiring the heated filament). [15%]

2 (a) The process flow for the production of the SOI wafer is as follows:

1	RCA1	Boil two 6” silicon (100) wafer in RCA Clean 1 ($NH_3(aq):H_2O:H_2O_2$) to remove organic contaminants.
2	RCA2	Boil the two silicon substrates in RCA Clean 2 ($HCl:H_2O:H_2O_2$) to remove metallic ion contaminants.
3	OXI1	Thermally oxidise a 5 μm thick layer of silicon dioxide onto one of the silicon wafers using wet oxidation with oxygen bubbled through boiling DI water at 1250 °C.
4	CMP1	Use chemical mechanical polishing to remove the layer of silicon dioxide from the backside of the oxidised silicon wafer.
5	RCA3	Boil oxidised silicon wafer in RCA Clean 1 ($NH_3(aq):H_2O:H_2O_2$) to remove organic contaminants.
6	RCA4	Boil the oxidised silicon wafer in RCA Clean 2 ($HCl:H_2O:H_2O_2$) to remove metallic ion contaminants.
7	HYD1	Plasma hydrophilise the mating surface of the two silicon wafers.
8	FUS1	Fuse the two wafers together by bringing them into contact.
9	ANN1	Anneal the fused wafers at 1000 °C to strengthen the bond.
10	CMP2	Chemically mechanically polish the exposed surface of the unoxidised wafer down to ~22 μm.
11	RIE1	Reactive ion etching of the polished surface using a CF_4+O_2 plasma down to a 20 μm thick layer.

(b) The maximum length of the cantilever without stiction is given by s*, where *h* is determined by the thickness of the thin silicon layer and *g* is determined by the silicon dioxide thickness. From the 4M6 Data Book, *E* is 190 GPa, so

$$s^* = \sqrt[4]{\frac{3Eh^3g^2}{2\gamma}} = \sqrt[4]{\frac{3\times190\times10^9\times\left(20\times10^{-6}\right)^3\times\left(5\times10^{-6}\right)^2}{2\times0.1}} = \underline{870\,\mu\text{m}}$$

(c) The process flow for the production of the cantilevers is as follows:

1	SIN1	Use LPCVD to grow a 400 nm thick layer of silicon nitride onto the top surface of the thin layer of silicon using a gas mixture of SiH_2Cl_2 and NH_3 at 800 °C and 70 Pa.
2	PHO1	Spin a layer of photoresist onto the top side of the silicon wafer.
3	BAK1	Pre-bake the photoresist.

4	EXP1	Expose the photoresist through a mask to produce a pattern in the photoresist which will protect the cantilevers.
5	DEV1	Develop the photoresist.
6	BAK2	Post-bake the photoresist to harden it.
7	RIE1	Reactive ion etch the silicon nitride layer using a gas mixture of CF_4+CHF_3+He.
8	DRI1	Deep reactive ion etch through the 20 µm silicon layer using a SF_6 and C_4F_8 BOSCH process.
9	BHF1	Etch the silicon dioxide with buffered hydrofluoric acid to undercut the silicon cantilevers.
10	DIW1	Rinse in DI water to rempver any remaining buffered hydrofluoric acid.
11	IPA1	Rinse in isopropanol.
12	ACE1	Ultrasonicate in acetone to remove any residual photoresist.
13	ACE2	Rinse in fresh acetone and blow dry.

(d) A self-assembled monolayer could be coated on the surfaces of the silicon facing into the gap.

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(a) (i) In the absence of any thermal constraints and with the requirement for a low stress, LPCVD should be used as this allows a silicon-rich silicon nitride to be produced with zero stress gradient.

(ii) The aluminium thin film presents a significant thermal constraint, and it will not tolerate the 800 °C that LPCVD requires. Therefore, rf-PECVD would be best employed in this situation.

(iii) There is a very strong thermal constraint from having to deposit on top of the SU8. Therefore, sputtering would have to be used in this scenario, as it does not require any substrate heating.

(b) The difficulty with this process is the need to coat just the inside of channel. The following process could achieve this:

1	STE1	Heat sterilise in an autoclave at 121 °C and 10 psi for 30 minutes.
2	ADH1	Treat the surface of a bare silicon wafer in adhesion reducer.
3	PDM1	Spin a layer of PDMS onto one side of the bare silicon wafer.
4	BAK1	Cure the PDMS at 60 °C for one hour.
5	PEE1	Peel the PDMS away from the substrate.
6	DIP1	Dip coat the PDMS in a thin photoresist.
7	MCP1	Press the PDMS stamp onto the surface of the SU8-coated wafer.
8	BAK2	Bake the photoresist to harden.
9	HYD1	Hydrophilise the surface of the wafer with a short oxygen plasma hydrophilisation.
10	ALK1	Rinse the surface with the biological molecule.
11	ACE1	Wash the surface in acetone to remove the photoresist and any biological molecule on its surface.
12	ACE 2	Wash the surface in fresh acetone to clean.

4 (a) *Anisotropic etching of crystalline materials:* Whilst most wet etches are isotropic, in some cases the wet chemical etch rate varies with crystallographic orientation, resulting in anisotropy. In the case of silicon, the most common anisotropic etchants are strong bases. Orientation dependence is a consequence of the fact that different crystalline surfaces will have varying structures. The (111) surface of c-Si is particularly stable as a silicon atom on the surface will only have one of its four bonds pointing out of the surface with the other three pointing back into the bulk of the material. This results in a stable surface with a high surface density of atoms. As KOH etching, for example, proceeds by the insertion of an OH group into a Si—Si bond, the etch rate of the Si(111) surface is suppressed. The result is that 2.5D structures can be produced from simple 2D surface patterning, such as grooves or pyramids.

(b) *Shape memory effect:* Certain metal alloys, such as NiTi display a shape memory effect. These alloys all undergo a crystalline phase transformation from a weak and easily deformable state at low temperatures to a hard phase at temperatures above a transition temperature, T_{tr}. Initially, the material is held in the desired shape and heated to above T_{tr} to fix this shape 'in memory'. The material is then allowed to cool into its weak state, when it can be deformed easily. However, upon heating the alloy above T_{tr} once more, it reverts to its 'stored' shape, exerting very large forces in the process, making these materials very useful as mechanical actuators in situations where a high frequency response is not required.

(c) *Piezoelectric effect:* Certain materials (such as quartz) have the physical property than a charge is developed on their surface when a mechanical stress is applied to them. Vice versa, it is also true that when a voltage is applied between two surfaces of a piezoelectric, a mechanical stress is generated. We can think of the piezoelectric effect as being due to the movement of anions and cations within the material under the influence of an applied electric field. The presence of both strong and weak ionic bonds in noncentrosymmetric crystals (with a lack of central symmetry) produces a deformation of the lattice. Piezoelectrics are extremely useful for MEMS applications as they provide a direct link between electric and mechanical properties,

$$D = d\sigma + \varepsilon_0 \varepsilon_r \big|_\sigma E \qquad (6.33a)$$

$$D = e\varepsilon + \varepsilon_0 \varepsilon_r \big|_\varepsilon E \qquad (6.33b)$$

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(d) *Piezoresistive effect:* The effect that the resistivity of a material can change when a mechanical stress is applied to a material is known as piezoresistivity. This phenomenon is caused by the change in the atomic spacing in the crystal lattice under

deformation. The periodic potential produced by the atomic lattice has a profound effect on the electrical properties of a material and most notably that of semiconductors. It is therefore perhaps unsurprising that changing this series of potential wells by the application of a stress will change the resistivity. This is particularly useful for MEMS sensors as it provides a useful means of electrically detecting mechanical strains. Assuming piezoresistance to be linearly dependent on stress (which is true for small strains) we can rewrite the Ohm Law as

$$\mathbf{E} = \left[\boldsymbol{\rho}_{\mathbf{e}} + \boldsymbol{\Pi} \cdot \boldsymbol{\sigma}\right] \cdot \mathbf{J} \qquad (6.38)$$

where $\boldsymbol{\rho}_{\mathbf{e}}$, $\boldsymbol{\Pi}$, $\boldsymbol{\sigma}$ and $\mathbf{J}$ are the resistivity, peizoresistive, stress and current density tensors.