4B22 – Flexible electronics
CRIBS Academic Year 2019

1. a)
A generic large-area electronic structure is composed of (1) a substrate, (2) backplane electronics, (3) a frontplane, and (4) encapsulation.

Backplanes provide or collect power and signal to or from front-planes. These may be passive or active. The ideal flexible active-matrix backplane should be rugged, rollable or bendable, capable of CMOS operation, and should lend itself to low-cost manufacturing. Today's TFT backplane technologies are best described by their active semiconductor, which may be amorphous, nanocrystalline, or polycrystalline silicon, a II–VI compound semiconductor, or an organic semiconductor in polymer or molecular form. As thin-film semiconductor technologies develop away from glass substrates and toward flexible substrates, the backplanes differentiate further by the type of substrate. The substrate material defines a region of TFT fabrication conditions in temperature–time space. The maximum tolerable process temperature is set by the type of substrate materials: < 300,< 600, and < 1,000◦C for organic polymer, glass, and steel substrates, respectively.

Frontplanes carry the specific optoelectronic application. The frontplane materials of displays include liquid crystals for transmissive displays, reflective-mode liquid crystals and electrophoretic foils for reflective displays, and OLEDs for emissive displays. The frontplane might also be an X-ray sensor, an image sensor, a pressure sensor, a chemical sensor, an actuator or an artificial muscle in a smart textile.

b)
The device islands are chemically bonded to a pre-strained substrate, while the interconnects are loosely bonded. When the pre-strain in the substrate is released, the interconnects buckle out of the surface and form arc-shaped structures. These wavy layouts can accommodate external deformations through changes in wavelength and amplitude.

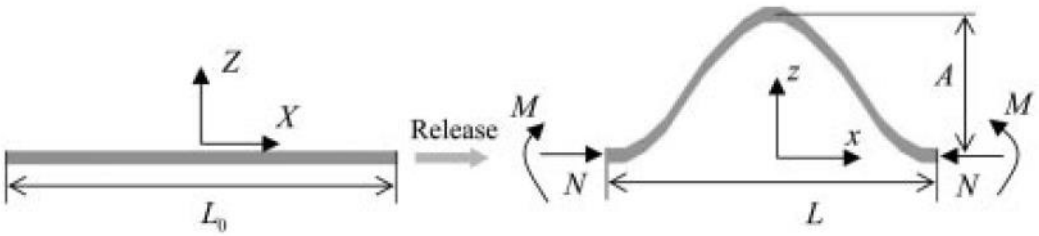


Figure 1: Schematic diagram of buckling mechanics

For a stiff thin film ribbon a wavy profile forms, with the out-of-plane displacement being:

$$w = A/2\left[1 + \cos\left(\frac{2\pi x_1}{L}\right)\right]$$

Where x_1 is the coordinate along the ribbon direction, A and L are the amplitude and the length of the buckled interconnection.

Normally, under full strain

$$w = A/2\left[1 + \cos\left(\frac{2\pi X}{L_0}\right)\right]$$

Where $X = L_0/2$ and $A = 2L0/\pi\sqrt{\varepsilon - \varepsilon_c}$, with ε_c being the critical buckling strain. Of a doubly clamped ribbon.

c)

a) Students can choose the description of two of the following list of conducting materials deposited by low temperature:

- Au evaporation
- Organic conducting polymers
- Nanomaterials (0D, 1D, 2D)

The low temperature deposition approach has several advantages with respect to mechanical transfer and printing:

– wider variety of substrate materials available, including low-cost plastics, paper or tissue;
– lower thermal budget materials can be integrated in the process, such as adhesives, polymers, and biomaterials;
– thermal deformations of the substrate are reduced, and so is mechanical stress occurring due to mismatch between thermal expansion coefficients of the substrate and the films;
– materials science, device physics, fabrication process, and equipment are already well established, for example, in a-Si technology.
For this approach due to the low maximum working temperatures of most low-cost plastics (the glass transition temperatures, T_g, in the range of 80 –150ºC), the thermal budget in the fabrication process is limited within 100 – 150ºC range.

d)

(i) Figure 1a) shows a pseudo-PMOS inverter composed by two p-type TFT transistors, with the load transistor connected as diode, i.e. the gate and drain contacts of the load transistor are short-circuited. Figure 1b) shows a pseudo-PMOS inverter with the a zero-Vgs (or current source) load transistor, i.e. the gate and source contacts of the load transistor are short-circuited. A meaningful operation of the zero-Vgs inverter is obtained only when the load uses a depletion-mode transistor (i.e. $V_T \geq 0$ V for a p-type OTFT). In this case the effective gate-source voltage is nothing but the V_T of the load transistor. As a result, zero-V_{GS} load inverters are greatly influenced by the variations in V_T. On the other hand, zero-V_{GS} load acts as a constant current source that results in a large small-signal output resistance. Consequently, the gain of the inverter that uses a zero-V_{GS} load is significantly larger. The load transistor, acting as a current source, operates in the sub-threshold regime producing a very low current, consequently the energy consumption is lower than in the diode-load configuration, but operates at lower speed.

In both cases the value of V_{PWR} has a negative value ($-V_{DD}$) in order to allow the circuit operating, and the same applies to Vin and Vout.

Key differentiating aspects of the two configurations:
<u>Figure 1a) diode-load configuration.</u>
The key advantages of a diode load inverter are: 1) faster switching speed (attributed to the strong pull-down force of the diode-connected load transistor) and 2) robust to variations in the threshold voltage (V_T).

On the other hand, its key disadvantages are: 1) poor noise margin due to its asymmetric transfer characteristics; 2) greater power consumption as a result of the large pull-down current; 3) low output voltage swing; and 4) low gain.
<u>Figure 1b) Zero-Vgs load configuration</u>

Key advantages of the zero-Vgs load configuration are: 1) large output swing; 2) good noise margin; 3) lower power consumption; and 3) relatively large gain.

On the other hand, its key disadvantages are: 1) slower switching speed; and 2) greater sensitivity to variations in the threshold voltage (V_T).

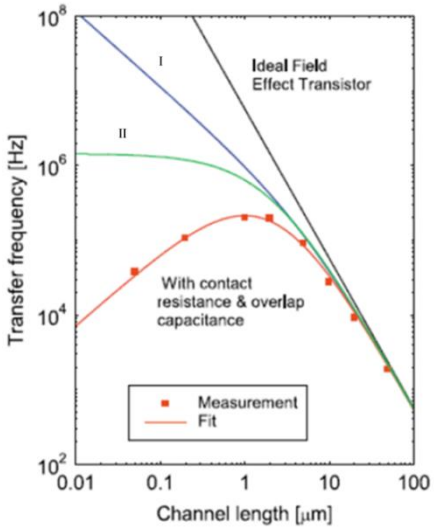
(ii) Overlap capacitances, are parasitic capacitances formed across the interlayer dielectric between the source and drain contacts and the gate areas. The contact resistance is the series parasitic resistance experienced by the charges when flowing in and out of the channel through the source and drain contacts.

Both parasitic parameters limit the switching speed of a thin film transistor, and can be modelled by modifying the effective channel length in the following formula of the cut-off frequency, from the ideal case:

$$f_T = \frac{\mu_0 V_{DS}}{2\pi L^2}$$

where f_T is the cut-off frequency, μ_0 is the field effect mobility, V_{DS} is the drain-source voltage and L is the channel length, to the following one, including the length of the overlap capacitance L_o and the length of the source and drain contact areas L_T.
as represented in the figure below, in the case of a Bottom Gate,
Where f_T is the cut-off frequency, μ_0 is the field effect mobility, V_{DS} is the drain-source voltage and L is the channel length, as represented in the figure below, in the case of a Bottom Gate, Bottom Contact Thin Film Transistor device.
When considering parasitic components in the device, such as contact resistance and overlap capacitance the actual equation assumes the following form:

$$f_T = \frac{\mu_0 V_{DS}}{2\pi L^2} \cdot \frac{L}{L + L_0} \cdot \frac{L^2}{(L + L_T)^2}$$



Where the first correcting term $\frac{L}{L+L_0}$ accounts for the effect of overlap capacitance (curve I in the graph of figure above), while the second term $\frac{L^2}{(L+L_T)^2}$ accounts for the effect of contact resistance (curve II in the graph of figure above).

Assessors comments:

This set of questions did not require any numerical answer. Most of the students could answer the first three questions (standard bookwork) reasonably well. However, (d)i and d(ii) could not be answered correctly by the majority.

2. a)

In this model electrons in a solid behave like a gas. Each atom contributes one electron to the gas, and the electrons obey Fermi-Dirac statistics (i.e. this leads to the Fermi-Dirac electrons velocity distribution as opposite to Maxwell-Boltzmann distribution).

The limitations are that this model cannot model the appearance of band gaps. Because the ions in a perfect crystal are in a regular periodic array, electrons in crystals can be studied by considering the problem of an electron in a periodic potential U(r) with the periodicity of the Bravais lattice, U(r+R)=U(r) for any Bravais lattice vector R.

The Kronig-Penney model considers an additional periodic potential U(x,y,z), to the Schrodinger equation which represents the ionic charges of the crystal lattice. The Schrodinger equation in the 1D form can be then rewritten as

$$\hat{H}\psi(\boldsymbol{r}) = \left(-\frac{\hbar^2}{2m}\nabla^2 + U(\boldsymbol{r})\right)\psi(\boldsymbol{r}) = E\psi(\boldsymbol{r})$$

Where U(**r**) has the periodicity of the Bravais lattice. The solutions to these equations are of the form:

$$\psi_k(\boldsymbol{r}) = u_k(\boldsymbol{r})\exp(i\boldsymbol{k}\cdot\boldsymbol{r})$$

Where $\boldsymbol{k}$ is the wave vector, *r* is a position in the Bravais lattice and $u_k(\mathbf{r})$ is also a function with the periodicity of the Bravais lattice.

Independent electrons obeying to the the general Schrödinger equation in a periodic potential are called Bloch's electrons and follow the property below:

The eigenstates ψ of the one-electron Hamiltonian H = - ħ²/2m + U(r), where U(r+R)=U(r) for all R in the Bravais lattice, can be chosen to have the form of a plane wave times a function with the periodicity of the Bravais lattice:

$$\psi_{nk}(\mathrm{r}) = e^{\mathrm{ik\,r}} \cdot u_{nk}(\mathrm{r})$$

Where $u_{nk}(\mathrm{r} + \mathrm{R}) = u_{nk}(\mathrm{r})$, implying that $\psi_{nk}(\mathrm{r} + \mathrm{R}) = e^{\mathrm{ik\,R}} \cdot \psi_{nk}(\mathrm{r})$

This gives origin to a band-gap in the E vs k energy dispersion relation.

b)

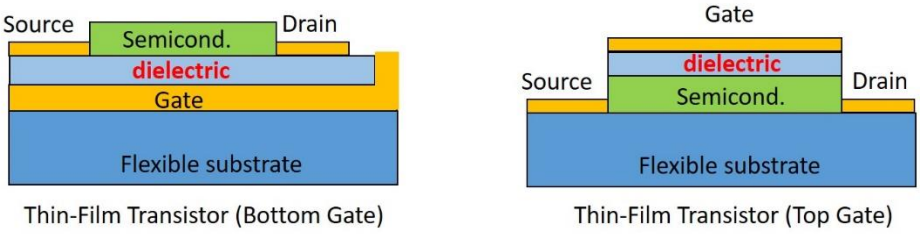
Using the Child's Law we have:

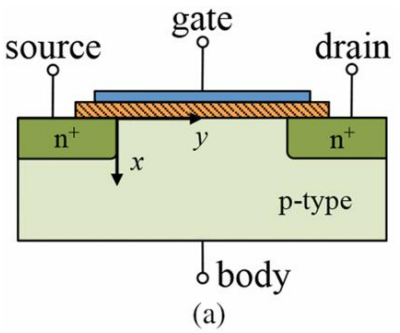
$$J_1 = \frac{9\varepsilon_r\varepsilon_0\mu_{eff1}V^2}{8d^3}$$
$$J_2 = \frac{9\varepsilon_r\varepsilon_0\mu_{eff2}V^2}{8d^3}$$

Where $\mu_{eff1} = \frac{n_1 - n_{trap1}}{n_1}\mu_1$=4.19999x10^{-8} m^2 V^{-1} s^{-1}; and $\mu_{eff2} = \frac{n_2 - n_{trap2}}{n_2}\mu_2$ = 8.68600x10^{-11} m^2 V^{-1} s^{-1}

Substituting the effective mobility in the Child's law equations we get J_1=27.31 kA m^{-2}
And J_2= 56 A m^{-2}.

c)





Metal–oxide–semiconductor field-effect transistor (MOSFETs) are based on a rigid crystalline doped silicon wafer patterned with regions at different doping levels (n or p). MOSFETs generally operate in inversion condition, where a conducting channel is formed under the gate dielectric layer and it is controlled by the Vg. The conductivity of the channel is controlled by the source and drain wells.
A MOSFET device architecture is characterized by: *i)* a p-doped or n-doped semiconducting substrate or well; *ii)* highly doped regions underneath the source and drain electrodes of different polarity than the substrate or well where the device is obtained, *iii)* a thin gate oxide (e.g. SiO2) in the active area between the source and drain electrodes and a gate electrode to generate a transversal electric field across the gate dielectric. This transversal electric field is responsible of the creation of an inversion region underneath the gate oxide which acts as a channel of opposite polarity than the well or substrate semiconductor where the device is obtained. As a consequence, by applying a potential difference between the drain and source, the corresponding electric charges are displaced throughout the channel and their rate is modulated through the potential difference between the gate and the well or the bulk substrate.

A Thin Film Transistor (TFT) is a layered structure on a neutral (plastic or glass) support substrate. A TFT is characterized by: a dielectric or intrinsic substrate where all active layers, including the semiconducting channel are deposited as thin film to form one of four possible staggered device architectures. More in details the following layers are deposited and patterned: i) source and drain contacts; ii) semiconducting channel, iii) gate dielectric, and iv) gate electrode. Their sequence can change according to different architectures of TFTs, e.g. bottom gate/bottom contacts (BGBC), bottom gate/top contacts (BGTC), top gate/bottom contacts (TGBC) or top gate/top contacts (TGTC). The gate dielectric layer is sandwiched between the gate electrode and a (generally amorphous or polycrystalline) thin semiconducting layer. TFTs normally operate in accumulation condition, whereby a concentration of charge carriers is accumulated at the semiconductor-insulator interface, thus determining the conductivity of the TFT channel.
In the standard MOSFETs the drain-current equations, μFE is a proportionality factor that relates the drain current *I*D to the gate and drain voltages *V*GS and *V*DS, the threshold voltage *V*t, the channel width *W* and length *L*, and the gate dielectric capacitance per unit area *C*ox.
However, experimentally, the mobility in amorphous or organic TFTs is found to depend on *V*GS and *V*DS. Therefore, it is more straightforward to view it as a small-signal bias-dependent quantity, analogous to the small-signal gain of an amplifier rather than the large-signal quantity
The Thin film technology is independent of the substrate which plays no role in the determination of the electrical properties of the TFT.

d)

Discussion about dimensionality affecting the electrical properties of electrodes .

d=50um, V_{screen}=0.2 m^3, K_p=0.3, (η) ρ_{max}=300g/l

$d = V_{screen} k_p \phi / \Rightarrow \phi$=0.25

$\eta = 1 + 2.5\,\phi + 6.2\,\phi^2 = 2$

Assessors comments:

A popular question. The majority of the students could correctly answer (a), (b) and (c). In particular, (b) was answered very well. However, many failed to highlight the key differences between TFTs and MOSFETs. The first part of (d) question was poorly done by most. The viscosity calculation part in (d) was correctly answered by the majority of the students.

3. a)
The charge transport in conducting polymers is complex and can be modelled considering the band transport for intra polymer chains and hopping for both intrachain and interchain transport.
If an electric field is applied, the polarons present in the polymer travel through the chain in the direction of the electric field. However, misalignment of the polymeric chain, the absence of pure crystalline polymers and the electric field and the scattering of polarons with phonons limits the band transport in conducting polymers. The latter factor originates a temperature dependence on the mobility which scales as form $\mu \propto T^{-\nu}$ where $1 < \nu < 3$. This dependence can be shown to derive directly from the Einstain relation

$$\mu = \frac{De}{k_B T}$$

where the diffusion coefficient $D=v\lambda_m$ might also be temperature dependant, where v is the drift velocity and λ_m is the mean free path. At higher temperatures more phonon modes are activated and the polarons will have a smaller mean free path. In conjugated polymers, for example, at temperature above the Debye temperature, the number of activated phonons increases linearly with temperature, more scattering is likely to occur, which gives rise to a $D \propto T^{-1}$ and thus μ which scales as T^{-2}.

b)
The starting point of the band model is the Schrodinger equation which can be mathematically treated in different ways. The nearly-free electron model assumes that the ions (positive charges) in the crystal lattice behave as perturbations in the uniform field in which the electrons can move.
.
The vectors in the reciprocal lattice exist in the momentum space (or k-space) which is the set of all momentum vectors a particle can have.

The electron's wavefunction is an oscillating wave with momentum k. The electron energy is proportional to k^2 for free electrons, thus making it intuitive to plot E vs k.

c)
Components:

A Indium Zinc Oxide (IZO) drain electrode;
B Indium Zinc Oxide (IZO) source electrode
C Indium Gallium Zinc Oxide semiconducting channel;
D Aluminium oxide gate dielectric layer;
E Ti/Au gate electrode;
F Ti/Au common source electrode.

On a glass or polymer substrate, neutralised by SiNx or SiOx, an indium gallium zinc oxide precursor solution is coated as a sol-gel form and photo-annealed in a N_2 atmosphere for a controlled time. Alternatively, a vacuum deposition technique (e.g. sputtering) can be used to deposit the metal-oxide layer. However the high temperature of these processes might affect the quality and density of the IGZO deposited layer, thus might not be suitable for low temperature flexible electronic substrates.

d)
$\sigma_{VRH}(T)=\sigma_0 \exp-(T_0/T)^{1/d+1}$, where d=3

$\sigma_{VRH}(T)=\sigma_0 \exp-(T_0/T)$, when d=1

Due to the most difficult hopping path limiting the conductivity in the 1D case, unlike the optimal hopping path between the parallel chains in the 3D case.

Assessor's comments:

Question (a) and (c) were also answered well. In particular, almost everyone could identify the materials and components in the TFT schematic. However, most of the students poorly answered (b) and (d), in particular, the assumptions for electronic band model in (b).

4)

a)

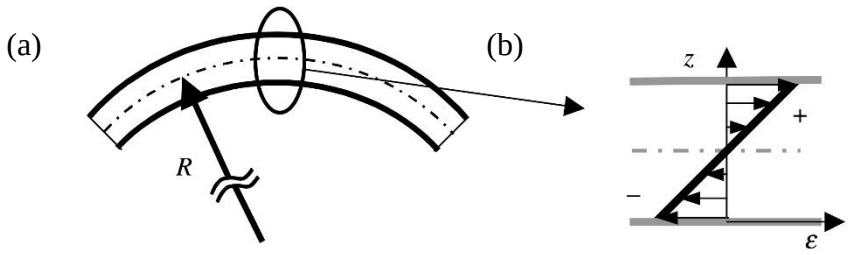


Figure 2: (a) sketch of the bent polymer film. (b) linear strain variation across the thickness of the polymer film.

The neutral plane for a uniaxially bent homogeneous polymer film denotes a plane parallel to its surfaces where the strain is zero. In the bent polymer film sketched in the above fig.1 (a), there will be compressive strain on top surface and tensile strain on the bottom surface. The strain variation across the thickness in a homogeneous polymer film will be linear, as shown in Fig 1(b). The neutral plane, marked by a dotted line in the centre along the thickness will therefore experience minimal strain.

b)

Optimum thickness (considering 90% transparency) is t_{opt} = 1/10 α = 1/(10*100000) cm = 10 nm

FOM, $\Phi = \sigma\, t_{opt} \exp(-10\, \alpha\, t_{opt})$ = 0.37 x 10 x 10 -9/ (1.7 x 10 -8) = 3.7/1.7 = 0.217

c)

Sheet resistance at 90% T (10 nm thickness, topt) = 2 x 0.85 = 1.7 Ω/sq (required value 2 Ω/sq).

Satisfies the requirements.

Plasma carrier frequency $fp = c / \lambda = 3 \times 10^8 / \lambda = (5.66 \times 10^{20})^{1/2} \times 1.602 \times 10^{-19} / 2\pi \times (9.109 \times 10^{-31} \times 8.854 \times 10^{-12})^{1/2} = 2.136 \times 10^{14}$

λ ~ 1400 nm (required value 1500 nm).
Does not satisfy the requirements.

Overall, the material does not satisfy the application requirements.

d)

Percolation of sticks with monodisperse diameter can be written as:

$$N_C L^2 = 5.71$$

where N_C is the critical percolation threshold (minimum number of nanowires required to form a percolated network) and L is the length of the nanowires.

Thus, for sample A (L=100 nm = 1×10^{-5} cm),

$$N_{CA}L^2 = 5.71$$

$$N_{CA} = \frac{5.71}{(1.2 \times 10^{-5})^2} \ /\text{cm}^2$$

$$N_{CA} = 3.96 \times 10^{10} \ /\text{cm}^2$$

i.e. 3.96×10^{10} number of wires will be required per cm^2 to establish a percolated network.

Similarly,

$$N_{CB} = \frac{5.71}{(0.5 \times 10^{-5})^2} = 22.84 \times 10^{10} \ /\text{cm}^2$$

$$N_{CC} = \frac{5.71}{(0.7 \times 10^{-5})^2} = 11.65 \times 10^{10} \ /\text{cm}^2$$

$$N_{CD} = \frac{5.71}{(0.8 \times 10^{-5})^2} = 8.91 \times 10^{10} \ /\text{cm}^2$$

Assessor's comments:

This was a popular question. Most could answer the standard bookwork questions (a) and (b). A few students had difficulties in unit conversion. However, the majority struggled with the equation for plasma frequency as well as the numerical calculation in (c). Almost everyone could answer the straightforward numerical question in (d).