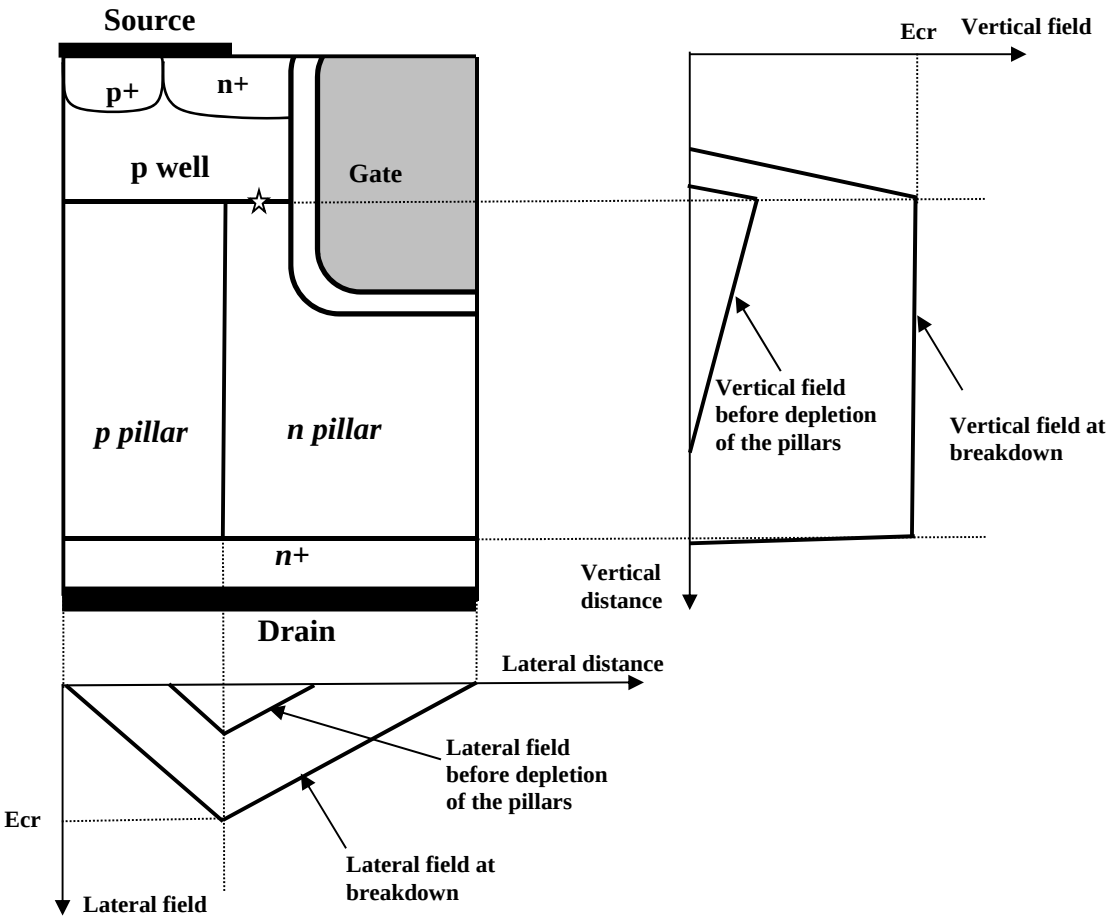
Solutions 4B2 2019

1 (a)



The drift region is comprised on n/p pillars. The vertical field is rectangular at breakdown and triangular before the breakdown. For an optimised superjunction the lateral field is triangular both before the breakdown (when the depletion region is undepleted) and at breakdown [40%]

(b) $f = \frac{1}{T} = 10\text{kHz} \;\; to...100\text{kHz}$, $D = 50\%$, $t_{on} = DT = \frac{D}{f}$

$$P_{\text{ON}} = \frac{1}{T}\int_0^{t_{\text{ON}}} V_{\text{ON}} I_{\text{ON}}\, dt = V_{\text{ON}} I_{\text{ON}} D\,, \qquad P_{\text{ON\_MOS}} = 3\times 5\times 1/2 = 7.5W$$

$$P_{\text{ON\_IGBT}} = 3\times 2\times 1/2 = 3W$$

TURN – OFF

Delay time: $P = V_{\text{ON}} I_{\text{ON}} t_s f$

$P_d = 3\times 5\times 0.1\times 10^{-6} f = 1.5\times 10^{-6} f$ (for both IGBT and MOS)

Growth time:

$$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left(V_{ON} + \frac{V_{dc} - V_{ON}}{t_g} t\right) = t_g f I_{ON}\left[\frac{V_{dc}}{2} + V_{ON}\right]$$

$$P_{g\_MOS} = 0.3\times 10^{-6}\times 3\times 205\times f = 184.5\times f\times 10^{-6}$$

$$P_{g\_IGBT} = 0.3\times 10^{-6}\times 3\times 202\times f = 184.5\times f\times 10^{-6}$$

Fall time :

$$P_f = tf\times f\,\frac{V_{dc}\times I_{ON}}{2}$$

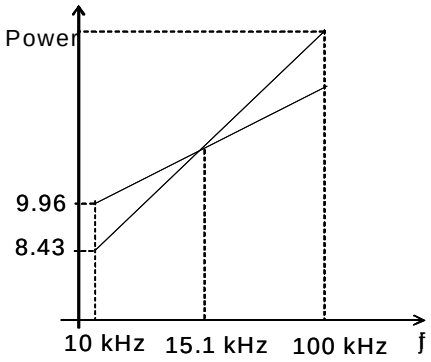
$$P_{f\_MOS} = 0.1\times 600\times 10^{-6} f = 60\times 10^{-6} f$$

$$P_{f\_IGBT} = 0.6\times 600\times 10^{-6} f = 360\times 10^{-6} f$$

Total losses (on-state + turn-off):

$$MOS: 7.5 + 246\times 10^{-6} f$$

$$IGBT: 3 + 543.3\times 10^{-6} f$$



MOS is more efficient at high frequencies (due to lower switching losses) > 15 kHz

IGBT is more efficient at low frequencies (due to lower on-state losses) <15kHz

[40%]

(c) In the MOSFET the on-state resistance (on-state voltage) is expected to increase by 2-3 times from 25 to 150 ºC. The turn-off losses in MOSFET are generally unaffected. In the IGBT, it depends if a positive temperature coefficient (NPT) or negative temperature coefficient (PT) design is employed. In any case the voltage drop can decrease or increase by a very small amount (say 0.1 V – 1V). The turn-off losses are expected to increase slightly in the IGBT as the tail current gets larger and longer at higher temperatures. Overall, the IGBT will perform better at higher temperatures and therefore it will increase slightly the maximum operating frequency beyond which the MOSFET will be more efficient. [20%]

2. (a) The dV/dt effect appears during turn-off when a high forward voltage is re-applied to the structure. There is a maximum *dV/dt* rating above which the displacement current created through the junction capacitance will be greater than the breakover current.

One solution to minimize the effect of the *dV/dt* (or in other words to increase the maximum *dV/dt* rating) is to use cathode shorts. Since a large component of the displacement current is safely absorbed via the cathode shorts, the slope dV_F/dt, can be higher without triggering the parasitic re-turn-on of the thyristor. The smaller the short resistance R_s, the more effective the cathode short is, and the higher the maximum dV_F/dt rating.

The effect of the cathode short can also be seen as an effective reduction in the current gain of the npn transistor (α_2). As a result the thyristor feedback reaction is weaker, making the *dV/dt* rating higher.

There are two more advantages resulting from the use of cathode shorts:

(i) the increase in the breakover point
(ii) a faster turn-off.

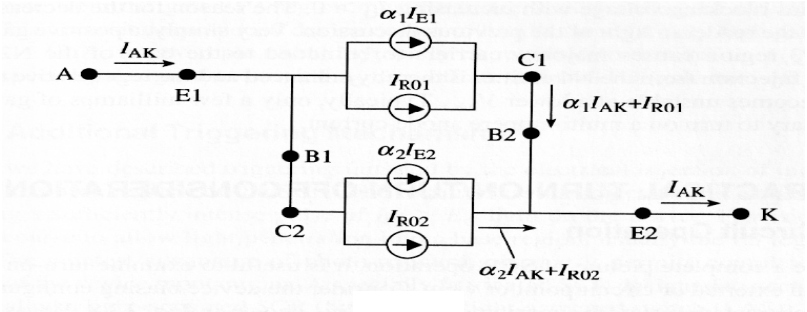
There are however two major drawbacks:

(i) the turn-on is slightly slower.
(ii) The on-state losses are slightly higher.

Another solution to increase *dV/dt* rating as well as the turn-off speed and the breakover voltage is to use anode-shorts. This time the gain of the pnp transistor is lowered (α_1). Anode shorts are slightly more difficult to fabricate as they require a photolithographic process on the backside of the wafer, but they offer good overall trade-off between robustness & turn-off speed on one hand and turn-on and on-state losses on the other hand.

[30%]

(b) (i) The Ebers-Moll equivalent circuit of the thyristor based on the two equivalent circuits for the bipolar transistors is shown below. The gate current was considered to be zero as the thyristor is in the off-state.



From the equivalent circuit above one can obtain the following expression:

$$I_{AK} = \alpha_1 I_{AK} + I_{R01} + \alpha_2 I_{AK} + I_{R02}$$

where I_{AK} is the anode current (same as cathode current) and I_{R01} and I_{R01} are saturation currents (leakage currents) associated with the two transistors.

$$I_{AK} = \frac{I_{R01} + I_{R02}}{1-(\alpha_1 + \alpha_2)}$$

If $\alpha_1 + \alpha_2 < 1$ the thyristor blocks the voltage and the anode-cathode current I_{AK} (i.e. leakage current) is small; of the same order of magnitude as the saturation currents of the bipolar transistors. However when $\alpha_1 + \alpha_2$ approaches one, the leakage current increases and when $\alpha_1 + \alpha_2 = 1$ the device no longer can block the voltage and the device turns on.

[30%]

(ii) Breakover occurs when

$\alpha_1 + \alpha_2 = 1$ or $\alpha_{npn} + \alpha_{pnp} = 1$

$\alpha_{npn} = 0.5 \quad \alpha_{pnp} = 1 - \frac{w_{eff}^2}{2L_p^2}$

$w_{eff} = w_{drift} - w$ (The effective base of the pnp transistor is the undepleted region of the n –drift region – n-base).

$$\Rightarrow \alpha_{pnp} = 1 - \frac{(w_{drift} - w)^2}{2L_p^2} = 0.5$$

$$\Rightarrow (w_{drift} - w) = L_p$$

$$\Rightarrow w = w_{drift} - L_p \Rightarrow \frac{2\varepsilon_0\varepsilon_r V}{q}\frac{1}{N_D} = (w_{drift} - L_p)^2$$

$$\Rightarrow V = \text{BREAKOVER VOLTAGE} = \frac{qN_D(w_{drift} - L_p)^2}{2\varepsilon_0\varepsilon_r}$$

$$V = \frac{1.6\times10^{-19}\times10^{13}\times10^{6}\times150^2\times10^{-12}}{2\times11.9\times8.854\times10^{-12}} = 170.83V \Rightarrow BREAKOVER$$

For 10^{13} cm^{-3}, the avalanche breakdown voltage ~10^3 V, much higher than the breakover voltage.

[30%]

(iii) The break-over voltage is based on the positive feedback of the two bipolar transistors, while the avalanche breakdown refers strictly to the abrupt multiplication of carriers when the electrical field at one location reaches a critical limit. The break-over voltage is in general smaller (and in some cases significantly smaller) than the avalanche breakdown.. Nevertheless if the gains of the npn and pnp transistors are very small (by for example applying heavy lifetime killing), it is possible, in theory that avalanche sets in before break-over. In IGBTs only avalanche is possible as there is no positive feedback. The avalanche is however enhanced by the pnp transitor. [10%]

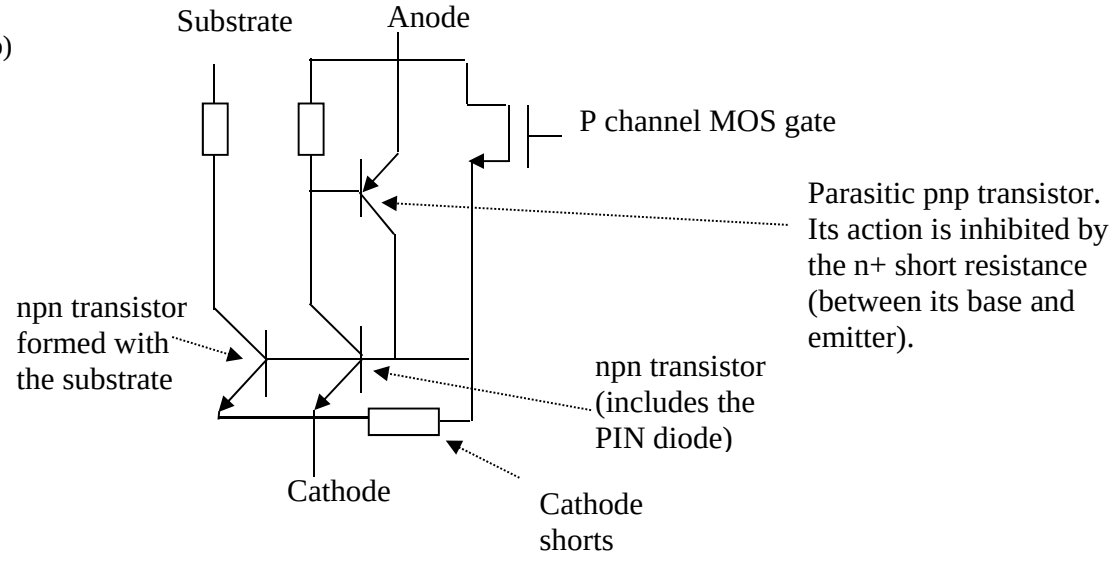
3. (a) The device is a p-channel IGBT with cathode shorts. The structure can be used as a high side device without the need for a level shifter. Thus the gate of the device can be referred to the anode – which in high side is the rail voltage. The Anode sits at the highest potential and the gate is referred to the anode potential. The cathode sits at lower potential than the anode. When the absolute value of the gate voltage is greater than the threshold voltage of the channel formed in the n well, alongside the trench walls, a hole inversion layer is established which connects the p+ source with the p layer. Holes are thus injected from the p+ anode (connected to the anode) into the p layer which acts as drift region. Initially the holes are collected by the p+ short, but when the n+ cathode/p drift layer junction becomes forward biased, the n+ layer starts injecting electrons into the p layer modulating its resistance.

- In the off-state the device behaves similarly to an n-channel IGBT. Most of the voltage is supported across the p layer region (the n well/p layer junction is reverse biased).
- The device is turned on by applying a negative voltage onto the gate, with respect to the anode, thus forming a channel in the n well and an accumulation layer in the p well around the gate. This allows injection of holes into the p layer.

-In the on-state, initially the device behaves as a p-channel Power MOSFET, with the holes collected by the p+ short. The device turns into an IGBT mode, following a snap-back, when the n+ cathode/p layer junction becomes forward biased and electrons are injected into the p layer and the n- substrate via the action of the lateral npn transistor and the vertical npn transistor (with the collector as the n- substrate). As a result heavy conductivity modulation occurs in the p layer and the n- substrate resulting in formation of plasma.

- The turn-off of the device is achieved by bringing the gate voltage to the anode potential. Electrons are extracted during turn-off via the n+ short and the depletion starts building into the p layer and the n- substrate clearing out the plasma. [40%]

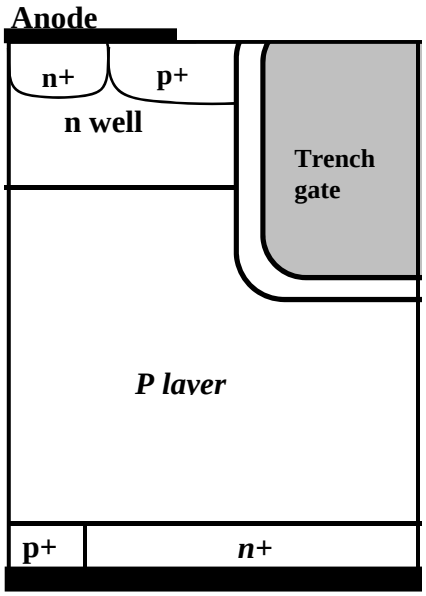
(b)



The substrate needs to be biased at high voltage (e.g. same at anode terminal) to avoid the junction between the substrate and the p layer to become forward biased in the normal on-state operation. [25%]

(c) In the reverse mode, there are two PIN diodes that will become active (forward-biased), from p+ Cathode/pwell/n-substrate and p+cathode/pwell/player/nwell/n+Anode. These diodes act as anti-parallel diodes and could be used for free-wheeling in half bridges. [10%]

The alternative vertical structure with trench technology is shown below.



Advantages of the lateral technology:

(1) Possibility of integrating CMOS circuits for drive, control, protection and processing of the signals.
(2) Possibility of running much lower gate voltages (5 V) than those typical for the vertical devices (15V)
(3) Better tolerances and control due to the CMOS process.

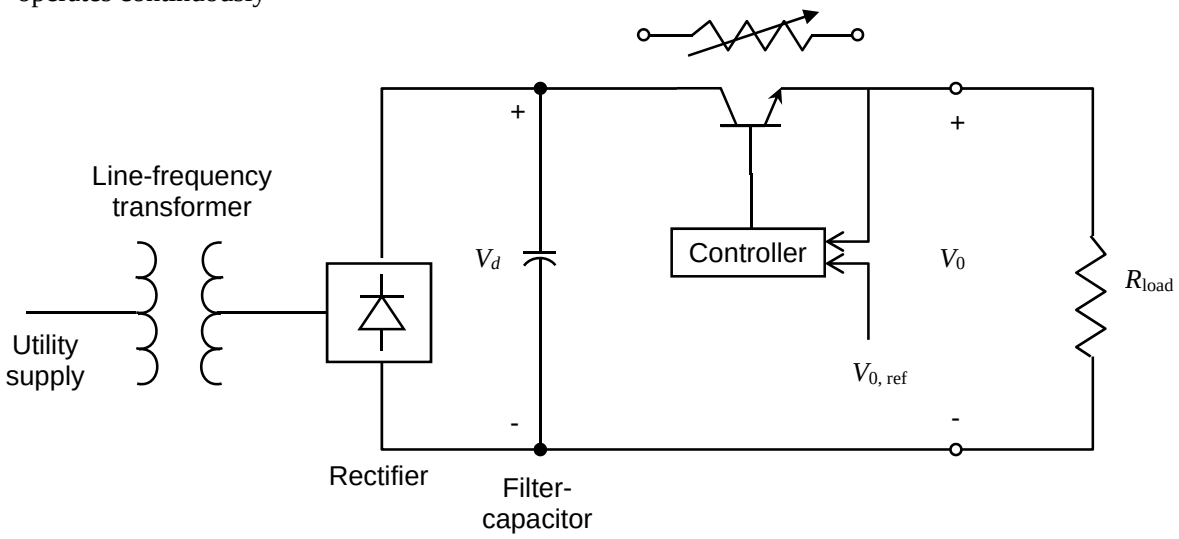
Disadvantages of lateral technology

(1) Poorer on-state performance (because of larger area consumption)
(2) Presence of a second parasitic npn with the substrate – slower speed
(3) The substrate terminal needs to be connected to the highest potential to reverse the n-substrate/p layer junction. [25%]

4.

Linear electronics

The figure below shows a typical linear AC-DC converter and some voltage waveforms (at the transformer secondary and output). . In the linear power supply a line- is used to for stepping down the line voltage to an appropriate level (close to the level of the desired DC output). The voltage at the secondary is then rectified and filtered so that the resultant voltage V_d (which depends on the utility supply magnitude and its variations, typically 10%) is slightly higher than the output voltage V_o. The transistor, used in common base configuration absorbs the voltage difference between V_o and V_d and behaves like a controlled resistor. In this configuration the transistor dissipates a lot of power as the current flowing from collector to emitter is very high (the voltage at the secondary winding is low and therefore the current is high) and the device operates continuously



Disadvantages

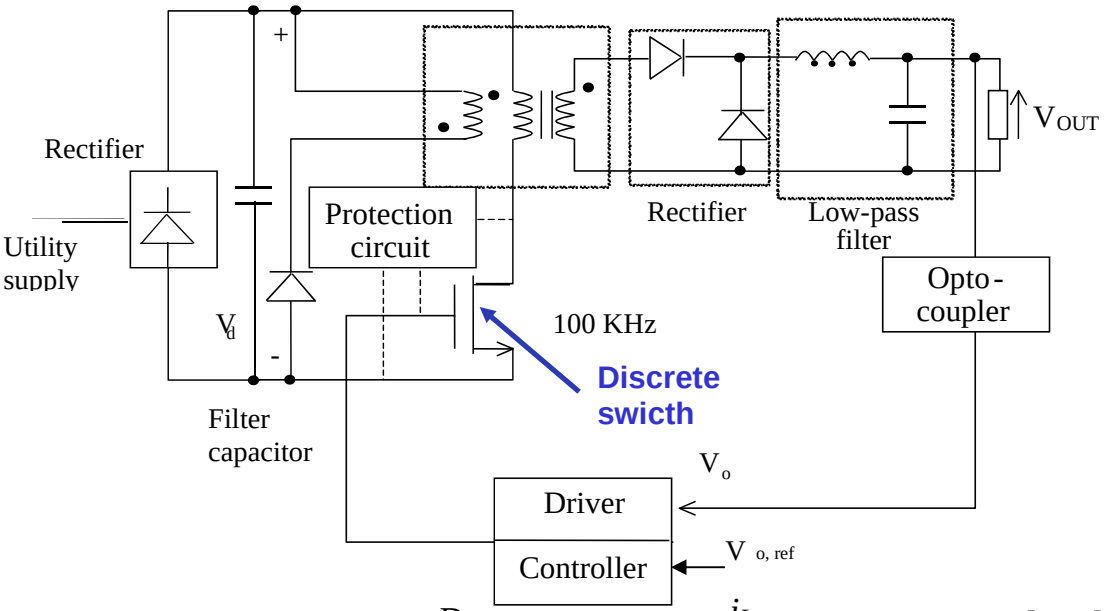
- very low efficiency (typically 30-50% !) (losses are high in the transistor as this operates as an 'adjustable resistor')
- the low frequency line transformer is very heavy and large - remember low ω ⇒ large L (to achieve the same reactance ωL) ⇒ large size and weight
- heating problems (due to excessive power losses) which lead to reliability problems

Advantages

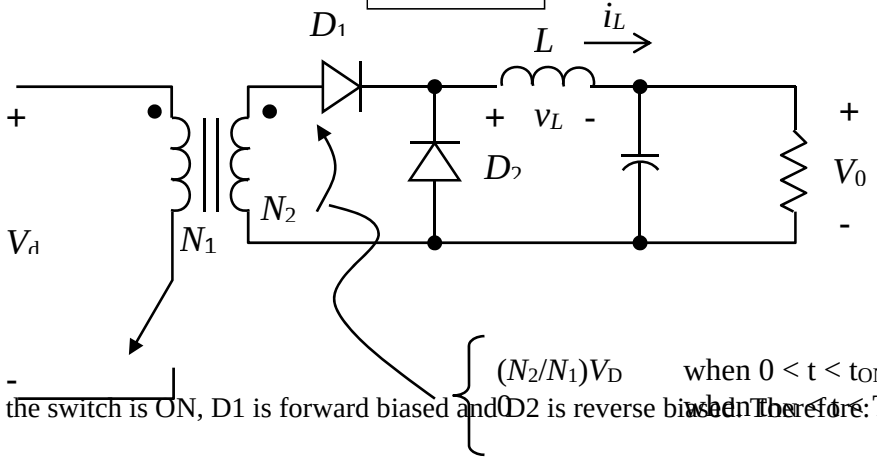
- presently cheaper than switching mode electronics, although the prices in power electronics are decreasing rapidly
- operation at low frequency means the EMI (electro-magnetic interference) is less severe.

Switching mode power electronics

The AC-DC converter is shown below. The signal provided by the utility supply is first rectified and filtered to obtain a high DC voltage V_d. The DC voltage is then converted back into an AC form by switching the transistor ON/OFF at high frequencies (e.g. 100 KHz). The transistor is placed on the primary side of the transformer and therefore sees a high voltage (in the OFF state) and a lower current in the ON state (when compared to the output current).. Since the transistor operates ON/OFF with relatively low losses, the efficiency of the system can be dramatically improved! The ac voltage at the secondary is then rectified by the output diodes and a low-pass filter is used to extract its average DC component so that the load sees a constant DC voltage. A feedback is provided from the output voltage to the gate of the transistors via a controller. This ensures that no matter what the load is, the output voltage remains unchanged. This can be done by finely adjusting the ON to OFF time ratio of the transistor.



[40%]

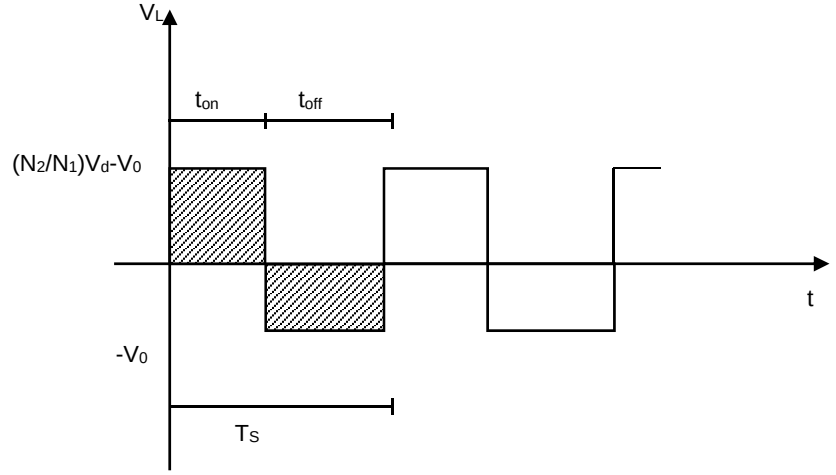


Initially when the switch is ON, D1 is forward biased and D2 is reverse biased. Therefore:

$V_L = \frac{N_2}{N_1} V_d - V_0$ when switch is ON

(ii) When the switch is OFF the inductor current i_L circulates through D2:

$V_L = -V_0$ when switch is OFF



Since the average power dissipated in the inductor is zero, we can equate the integral of the inductor voltage over one period to zero. The result is a DC voltage V_0 across the load:

$V_0 = \frac{N_2}{N_1} V_d \frac{t_{on}}{T_S}$ where $\frac{t_{on}}{T_S}$ is the duty cycle D and $\frac{N_2}{N_1}$ is the transformer turns ratios.

$$t_{ON}\left(\frac{N_2}{N_1} V_d - V_0\right) = V_0\left(T_S - t_{ON}\right) \Rightarrow V_0 = \frac{N_2}{N_1} V_d \frac{t_{ON}}{T_S}$$ [30%]

The feedback helps to maintain a constant DC level at the output with minimum ripple. The feedback provides a negative feedback that can adjust in small steps the duty cycle (via PWM) or the switching frequency (FM) to make sure that the output remains at a constant level. [10%]

The Superjunction has smaller specific on-state resistance than the Power MOSFET. It is therefore possible to have a superjunction device with smaller area and concomitantly lower on-state resistance. This means that the capacitances could be smaller while also reducing the on-state resistance. This means that the superjunction device can deliver both lower on-state and transient losses. Both devices suffer from lower carrier mobility at high temperatures. The superjunction will maintain the higher efficiency advantages at high temperatures.

[20%]

4B2
Examiner's comments:

Question 1, on the SMPS design and calculation of losses for MOSFETYs and IGBTs was attempted by 8 out of 9 candidates with an average of 71.43% for undergraduates. This question was virtually answered by all the candidates to a very high standard. It was pleasing to see that the candidates had good knowledge of SMPS systems and calculation of losses in both MOSFETs and IGBTs. Most of the candidates were able to calculate the instantaneous losses. The first part of the question on plotting lateral and vertical fields for superjunction devices was more difficult but in spite of this it was generally well answered.

Question 2 was split into two parts (a) dV/dt in thyristors (b) break-over and avalanche breakdown in thyristors and IGBTs. The question was attempted by all candidates with an average of 79.29% for undergraduates. The candidates answered very well this question. It was pleasing to see that all candidates understood the difference between the breakover and avalanche type breakdown and virtually all explained correctly the dV/dt effect in thyristors.

Question 3 was a 'blue sky' question where the candidates were asked to look at a p-channel lateral device and explain its operation in different regimes. One sub-question was to derive an equivalent vertical structure This was attempted by 1 undergraduate and 1 graduate. The average mark was 67.5%.

Question 4 was on a comparison between SMPS and linear circuits designs. The question was very well answered by most of the candidates (taken by 8 out of 9) with an average of 88.3%. It was very pleasing to see that most of the candidates were able to understand the benefits of the SMPS power supplies in comparison with the linear electronics and there were good attempts to explain the benefits of superjunction vs MOSFETs in AC to DC converters