WORKED SOLUTIONS

Paper 3

ELECTRICAL & INFORMATION ENGINEERING

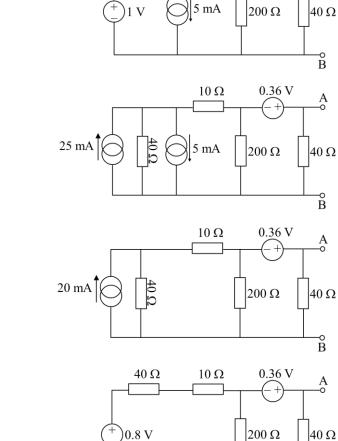
Section A – Joyce Section B – Hasan Section C – Ferrari/Malliaras

SECTION A

Question 1

equivalent:

The numbers are chosen so that (a) there is no need for a calculator



40 Ω

Convert left hand side to Norton

Combine the current sources:

Convert left hand side to Thevenin equivalent:



0.36 V

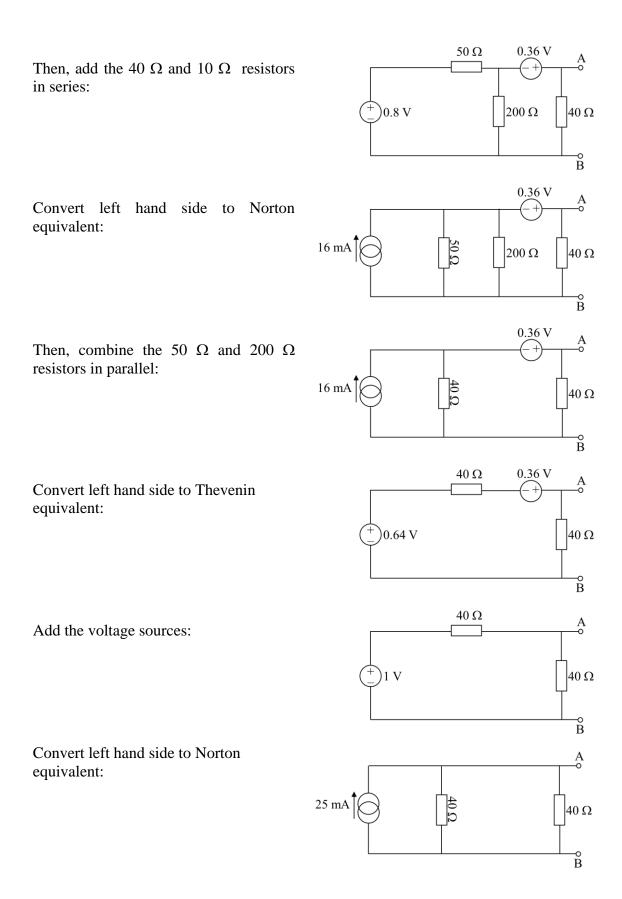
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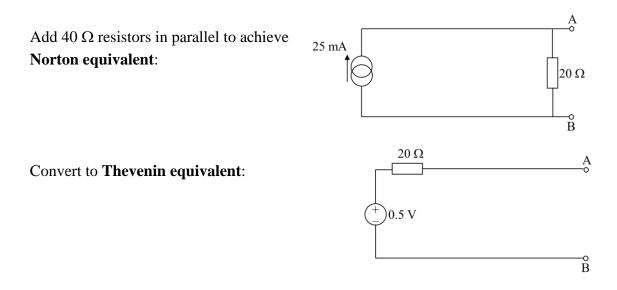
A

A

A 0

 $10 \,\Omega$





Examiner's comment: Most students answered this sub-question capably by doing a sequence of Thevenin and Norton simplifications, but many students made errors as a result of taking shortcuts. Common errors were:

- Neglecting the units (especially ohms)
- Summing currents incorrectly into a node (e.g. adding 25 mA and 5 mA when they should actually be subtracted).
- Adding resistances in series when they should be added in parallel.

A number of students started the process from the right hand side (nearest the terminals), which is always the more difficult approach and was more likely to result in errors.

A small number of students attempted to simplify the circuit through nodal or loop analysis. All these students found themselves lost in a sea of algebra and made errors. It is easier to sequentially perform Thevenin and Norton simplifications.

(b) Power to the load is maximised when $R_L = 20 \Omega$

The current through this load will be $\frac{1}{2} \times 25$ mA.

The voltage across this load will be $\frac{1}{2} \times 0.5$ V.

Power dissipated by load = $VI = I^2 R_L = 0.0125^2 \times 20 = 3.125 \text{ mW}$

Alternatively,

Power dissipated by load = $VI = V^2/R_L = 0.25^2/20 = 3.125 \text{ mW}$

Examiner's comment: Most students correctly identified that maximum power is transferred when the load resistor matches the Thevenin or Norton resistance. A handful tried to derive this from first principles (differentiating), which was actually

unnecessary. A fair number of students miscalculated the power lost across the load and got an answer that was 4 times higher than it should be.

Question 2

(a)

$$i = \frac{v_{in}}{R + j\omega L \|1/j\omega C}$$

Resonance occurs when the impedance of the capacitor negates the impedance of the inductor:

$$\omega L = 1/\omega C$$

$$\therefore C = \frac{1}{\omega^2 L} = \frac{1}{\left(2\pi \times 24 \times 10^3\right)^2 \times 90 \times 10^{-6}} = 489 \text{ nF}$$

(b) At 24 Hz, the impedance of the inductor is:

$$Z_L = j\omega L = j2 \times \pi \times 24 \times 10^3 \times 90 \times 10^{-6} = j13.57 \ \Omega.$$

At 24 Hz, the impedance of the capacitor is:

$$Z_{C} = 1/j\omega C = 1/(j2 \times \pi \times 24 \times 10^{3} \times 100 \times 10^{-9}) = -j66.31 \Omega.$$

Total impedance of the circuit $Z_{total} = R + Z_L \parallel Z_C$:

$$\begin{split} Z_{total} &= 10 + j13.57 \parallel \text{-}j66.31 = 10 + j\ 17.06 = 19.8\ \Omega \measuredangle 59.6^{\circ} \\ I_{rms} &= V_{rms} / Z_{total} = 200 / (19.8\ \Omega \measuredangle 59.6^{\circ}) = 10.1 \measuredangle \text{-}59.6^{\circ} \\ I_{peak} &= \sqrt{2}\ I_{rms} = \ \textbf{14.3}\ \textbf{A} \measuredangle \textbf{-}\textbf{59.6^{\circ}} \end{split}$$

In this case the current lags the voltage, because the load is predominately inductive.

Examiner's comment: A small number of students made errors in calculating the impedance of the circuit, some adding the reactances in series rather than in parallel. Many students only gave the rms current, but not the peak current. The strongest students explicitly stated that the current lags the voltage. Some students gave the phase in radians, which was marked correctly but degrees would be preferable.

Question 3

(a) The impedance of the load referred to the primary is:

 $Z_L' = (N_1/N_2)^2(0.3 + j0.2) = (10)^2(0.3 + j0.2) = \textbf{30} + \textbf{j20}\,\boldsymbol{\Omega}$

(b) The load current referred to the primary, I_L ' is:

I_L' =
$$240/(Z_L' + R_1 + R_2' + X_1 + X_2') = 240/(40 + j30)$$

 $|I_L'| = 4.8A$

The actual load current is:

$$|I_L| = (N_1/N_2) \times 4.8$$

= **48** A

(c) The real power dissipated in the load is:

P =
$$I_L'^2 R_L' = 4.8^2 \times 30$$

= **691.2 W**

Or alternatively:

$$P = I_L^2 R_L = 48^2 \times 0.3$$

= 691.2 W

The reactive power is:

P =
$$I_L^2 X_L = 48^2 \times 0.2$$

= **460.8 VAR**

(d) The power loss
$$P_{loss} = I_L^{2} (R_1 + R_2) = 4.8^2 (6 + 4) = 230.4 \text{ W}$$

$$P_{in, total} = 230.4 + 691.2 = 921.6 W$$

Efficiency = 230.4/921.6

Examiner's comment: Common errors were:

- Misunderstanding that X denotes an imaginary component (reactance).
- In (a), neglecting the units (ohms).

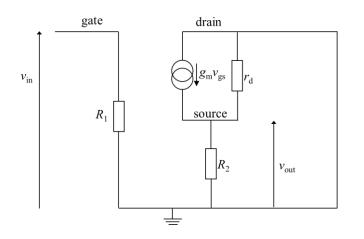
• In (b), only calculating the load current referred to the primary. The full, correct answer is the load current referred to the secondary winding, which is the actual load current.

• In (c), calculating the total real and reactive power dissipated, rather than the power dissipated in the load.

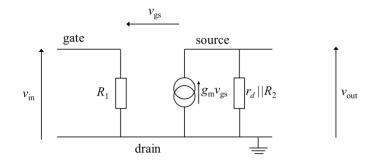
• In (d), misunderstanding the definition of transformer efficiency. Many students calculated efficiency incorrectly as the ratio of apparent power out/in. The correct definition is the ratio of real power out/in.

Question 4

(a)



which can be re-drawn as:



(b) and (c)

Input impedance $R_{in} = R_1 = 10 \text{ M}\Omega$

Gain

$$v_{out} = g_m v_{gs} (R_2 || r_d)$$
 equation 1

$$v_{gs} = v_{in} - v_{out}$$
 equation 2

Using equations 1 and 2 and eliminating v_{gs} gives

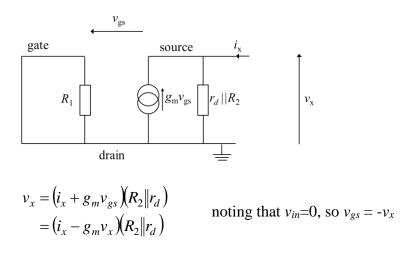
$$v_{in} - v_{out} = \frac{v_{out}}{g_m(R_2 \| r_d)}$$
$$\therefore v_{in} = v_{out} \left(\frac{1}{g_m(R_2 \| r_d)} + 1\right)$$
$$\therefore \frac{v_{out}}{v_{in}} = \frac{1}{\left(\frac{1}{g_m(R_2 \| r_d)} + 1\right)}$$
$$\therefore \frac{v_{out}}{v_{in}} = \frac{g_m(R_2 \| r_d)}{1 + g_m(R_2 \| r_d)}$$

Knowing that $R_2 || r_d = 5k || 20k = 4 k\Omega$, we can calculate the gain as

$$\frac{v_{out}}{v_{in}} = \frac{10 \times 10^{-3} (4 \times 10^3)}{1 + 10 \times 10^{-3} (4 \times 10^3)} = 40/41$$
$$= 0.976$$
$$\approx 1$$

This value (unity!) is expected for a source-follower (also known as a unity gain buffer)

<u>Output impedance</u>: Short circuit the input. Apply a test current i_x and test voltage v_x to the output terminal.



$$\therefore v_{x} + g_{m}v_{x}(R_{2}||r_{d}) = i_{x}(R_{2}||r_{d})$$

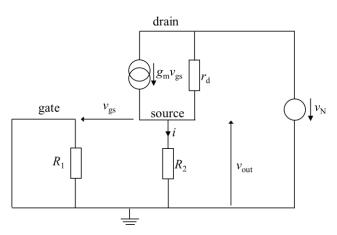
$$R_{out} = \frac{v_{x}}{i_{x}} = \frac{(R_{2}||r_{d})}{1 + g_{m}(R_{2}||r_{d})}$$

$$= \frac{(4 \times 10^{3})}{1 + 10 \times 10^{-3}(4 \times 10^{3})}$$

$$= 97\Omega$$

High input impedance, low output impedance, unity gain.

(d)



$v_{out} = iR_2$	equation 1
$v_{out} = -v_{gs}$	equation 2

 $v_{out} = -v_N + (g_m v_{gs} - i)r_d$ equation 3

Substitute equations 1 and 2 into equation 3:

$$v_{out} = -v_N + \left(-g_m v_{out} - \frac{v_{out}}{R_2}\right) r_d$$

$$\therefore v_{out} \left(1 + g_m r_d + \frac{r_d}{R_2}\right) = -v_N$$

$$\therefore \frac{v_{out}}{v_N} = -\frac{1}{\left(1 + g_m r_d + \frac{r_d}{R_2}\right)}$$

$$\therefore \frac{v_{out}}{v_N} = -\frac{1}{\left(1 + 10 \times 20 + \frac{20}{5}\right)}$$

= **-0.005**

Examiner's comment: This question was answered reasonably well. Common

mistakes in parts (a - c) were:

- Failing to ground the FET drain in the small signal model, leaving it at 10 V.
- Calculating the output impedance as r_d in parallel with R₂. This is incorrect, and the correct impedance is found by applying a test current and test voltage (i_x, v_x).
- Incorrectly drawing $v_{in} = v_{gs}$ in the small signal model.
- Incorrectly assuming $v_{in} = v_{gs}$ in the calculation of gain.

The best students noted that, as a source follower, you would expect unity gain, which agreed with their calculated gain. Some of these students also noted the low output impedance and high input impedance, which are desirable in a buffer.

Common mistakes in part (d) were:

- Drawing v_N across r_d only.
- Combining r_d in parallel with R_2 , which is not correct as they do not share the same two nodes.

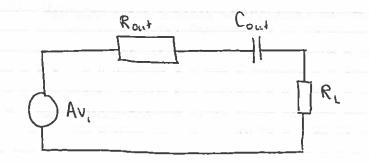
No students noted how little the noise is amplified (gain = 0.005), which is a pity! In part (e), the vast majority of students correctly answered that C_{out} should be placed in series with R_L to create a high pass filter. Some students didn't explain why. In the calculation of C_{out} , some students used the wrong values of resistance. E.g. they added R_L and R_{out} in parallel rather than in series, or they added R_L and r_d . Strangely, some students did not answer part 4(e) but could capably answer question

5(c-ii), which is a closely related question.

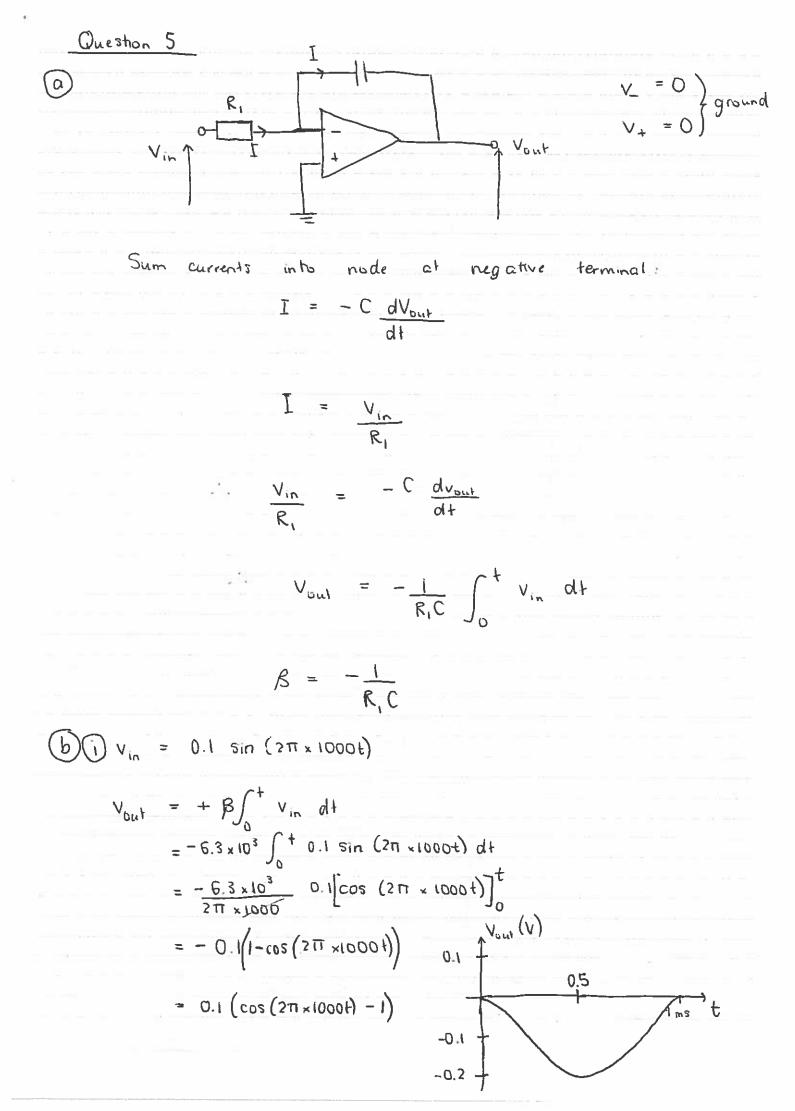
Cout should be placed in series with the load resistor, as the impedance of Cout is $\frac{1}{jWCout}$ which increases

as w decreases

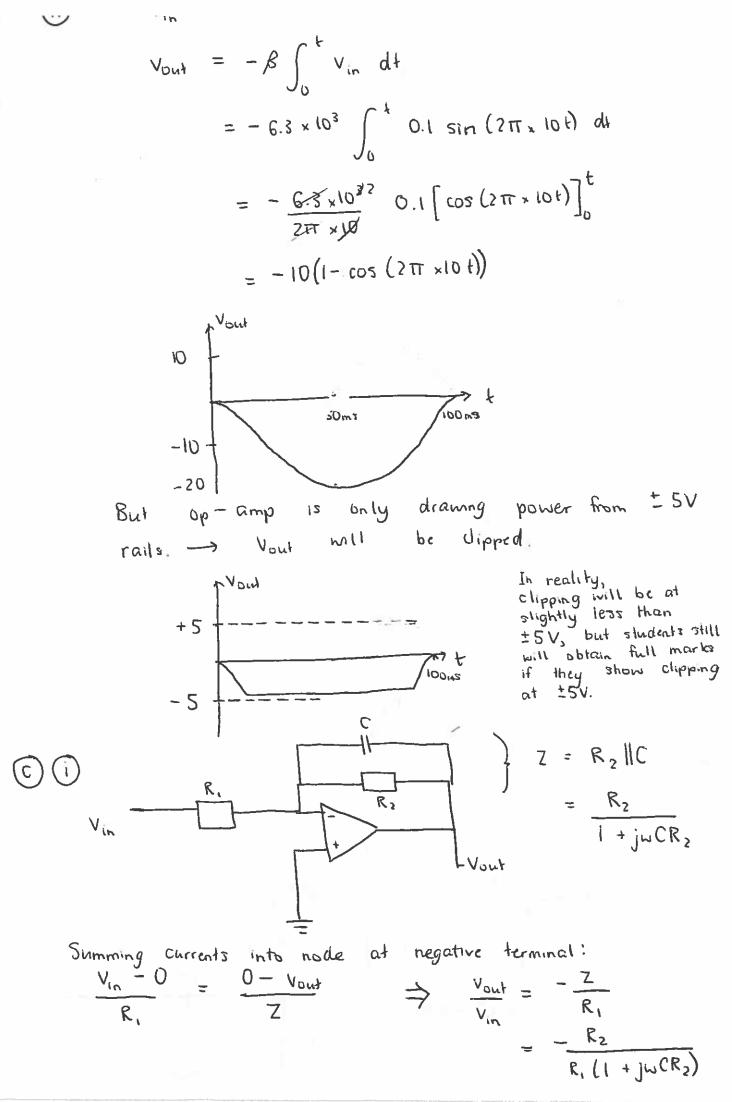
e



$$\begin{aligned}
 & \omega_{3dB} &= \frac{1}{C(R_{L} + R_{out})} \\
 C &= \frac{1}{\omega_{3dB}(R_{L} + R_{out})} \\
 &= \frac{1}{2\pi \times 200 \times (100 + 97)} \\
 &= 4.04 \times 10^{-6} F \\
 &= 4.04 \quad \mu F
 \end{aligned}$$



1.1.1



$$\frac{V_{out}}{V_{in}} = \frac{-R_2}{R_1(1+j\omega R_2C)}$$

(ii)

3 dB cut off when real = imaginary in denominator :

$$R_{2} = \frac{1}{wC}$$

$$= \frac{1}{2x\pi \times 10 \times 10^{3} \times 3.18 \times 10^{-9}}$$

$$= 5 k \Omega$$

6 La) K- Map 0P 00 01 Sum of products 10 Z = MN + OP + PN + MP + NO + MO0---00 0 ٥ 01 0 Z = MN+OP+PN+MP+NO+MO 11-IG Z = MN. OP. PN. MP. NO. MO Z = MN. OP. PN. MP. NO. MO Total mumber of gates required: 6 2 input NAND & 1 6 input NA 00 00 Product of sums 10 11 01 $\overline{z} = \overline{M}\overline{N}\overline{O} + \overline{O}\overline{P}\overline{M} + \overline{O}\overline{P}\overline{N} + \overline{M}\overline{N}\overline{P}$ 00 10 0 0 01 0 $\overline{2} = (M+N+0)+(0+P+M)+(0+P+N)+(M+N)$ ŀ Π Z = (M + N + 0) + (0 + P + M) + (0 + P + N) + (M + N)10 Total number of gates required: 4 3 input NOR & 14 input NOR. 7(a) LSB = MI, MSB = PIInput impedance at NI is 4R = 4kz Input impedance at PI is R = 1 Kr. When all inputs one connected to SV (HIGH), the total $\frac{1}{2} = \frac{3}{8R} + \frac{5}{4R} + \frac{5}{2R} + \frac{5}{2R} + \frac{5}{R}$ $V_{out} = -\frac{R}{2} \cdot I = -\frac{R}{2} \times 5 \left(\frac{1}{8} + \frac{1}{4} + \frac{1}{2} + 1 \right)$

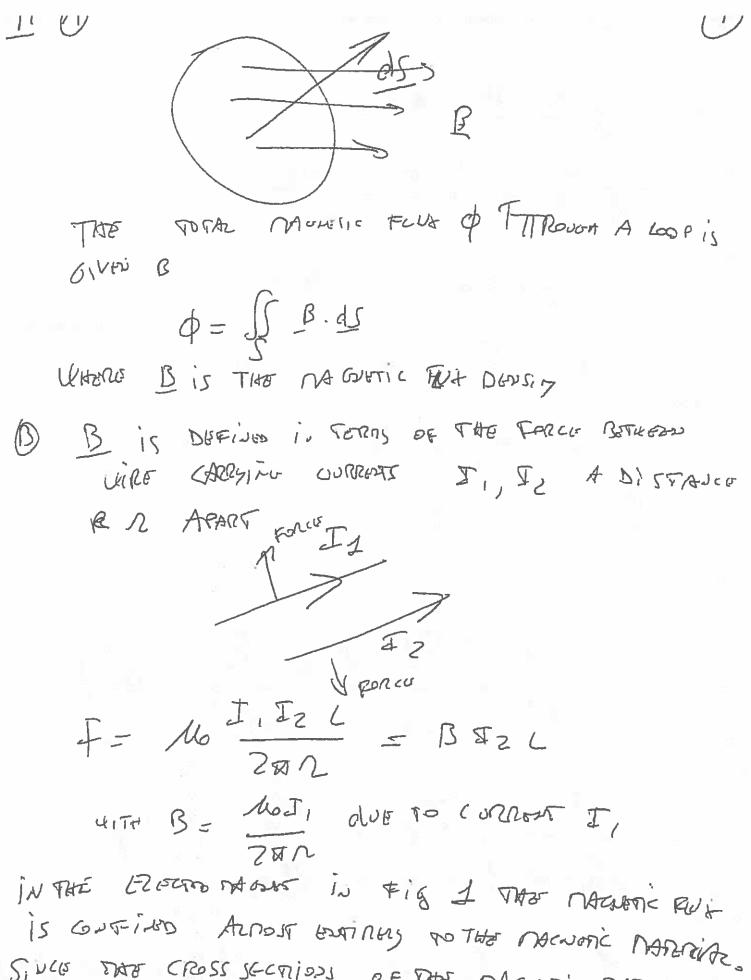
 $= -\frac{5}{2} \times \frac{15}{8} = -\frac{75}{16} = -4.6875 \text{ V}$ (b) Jranbacks of this design: 1) Resistance values are difficult to implement due to physical dimensions for DACs with higher 6its. The range of resistor values is vide. 11) Accuracy of the resistors to difficult to achieve, esp. for DACS with higher 6its 111) Input impedance of each bit is different. An R-2R ladder DAC can be used to avoid the above mentioned prov In this design the values of resistors required are R 2 2R only. 8(a) A static hazand in a combinational digital circuit is when a signal undergoes a momentary transition when it is supposed to remain unchanged. A static hazand can i of O on 1. Static O hazand 0 The signal is expected to stay at 0. Static I hazand 1 The signal is expected to stay at 1.

16 CD 00 01 10 11 $2 = A\bar{c} + \bar{A}D$ 00 To sensue static I hazand, an additional term in 1 01 meded to cover the adjacent but non-overlapping 0 0 11 groups. This is shown in the dotted group in the k-map. D 10 0 0 0 Therefore the function required to avoid static I have and is: $Z = A\overline{C} + \overline{A}D + \overline{C}D.$ AB CD -00 10 0 $\overline{2} = AC + \overline{A}\overline{D}$. 1 00 0 0 To remove static O hazand, an additional term in 01 meded to cover the adjacent but non-overlapping 0 0 11 groups. This is shown in the dotted group D 0 D 10 in the k-map. Therefore the function required to avoid static O hazand is: $Z = AC + \overline{AD} + C\overline{D}.$

9 (a) Truth table for 4 bit synchronous up counter: Present Next J3, K3, J2, K2, J1, K1 Jo, K. 0 0 OX 0 0 0 1 X 0 0 0 X X 1 0 1 0 OX 0-X X X 0 ł 1-0 0 0 0 Χ-0 -0 ł 1 X -Q-X X 0 Ó 0 0 ŀ O χ _]-Ø 1 0 0 X X 0 0 Х ł 0 Ò X X 0 0 Х Х 0 0 0 0 L 0 × ł 0 0 Х 0 0 X -X 0 \bigcirc D 0 0 X X 0 X ſ 1 0 l X \bigcirc 0 Ο X 1 0 0 0 X X l 1 1 X 1 X X Х 0 0 0 0 X 0 D 0 C X Х Ð 1-0 ſ Ð X X --[--1 0 0 D Х D 0 / X X 1 -0-D Ð 1-0 ł X 1 0 X X 0 -1-D X ł ---ŀ X 0 X X X -1--X---1 0 _ -0-0-0-Θ ť 0 X _____ 0 0 0 1 X X X -/-1 0 X X 1 0 X D Ł X 0 D X D χ \mathcal{O} 0 X (b) 0,00 J_3 0,00 Kz 0,02 00 0,02 00 01 11 10 01 10 1/ 0 0 0 Х 00 0 00 X X X X 0 01 0 1 0 01 X X X X -X-X -X-1 0--11-0--11--0--0--0 -0-X -χ-0-X X 10 10

0,0-2 01 1/ 10 00 0 | 00 01 11-0-2-2 0 1 X 00 0 00 0 X X X 0-[-0-1-X X X X Ð 0 0 11 Ô X t. X × X 1 0 0 X X X x 1 D 10 0-0 10-0.00 0,00 Kı J1 0302 10 1/ 1/ 01 10 00 00 01 0-0-2 X 1 00 X 00 0 X Х 0 1 T 01 X X 01 0 X 0 X E × -11x -1-1--X 0 x 1 t 0 X X Х x 10 10 0 0,0. 0-100 J. 030-2 ko 10 1/ 1/ 00 01 -10 01 00 0-2-2 X × 1 X 00 00 × 1 X 1 1 × 01 x X 1 01-X × X 1 11 1 X x x 1 Ì. 10 X 10 t $T_3 = Q_0 Q_1 Q_2$ $J_1 = Q_0$ $k_3 = Q_0 Q_1 Q_2$ $K_1 = Q_0$ $J_2 = Q_1 Q_0$ Jo=1 $k_2 = Q_1 Q_0$ Ko=1

(C) Without carry in & carry out VDD T Oul $\mathcal{T}_{\mathbf{Z}}$ **J**_ 0-0 $\mathcal{I}_{\mathbf{J}}$ \mathcal{J}_{i} 8, θ., a., 52 K.5 k, Cũk With carryin & Carry out i Inspecting Jo, Ko, Ji, Ki, Je, Ke & Js. Kg, previous stages (carry in, should be incorporated with AND gates. Corry V_{DD}-J 02 T, 0.0 *T*, T, 03 0.1 ary k, k, K. 1 CLK (d) UK 0-0 0-1 82 0-3 O-Ipsee = 10-MH2



Sives THE CROSS SECTIONS OF THE MADUUT'S NATION, AL AND THE AIR GAP AND THE SAME, THE MADUUT'S FULL DENS, IT BIS ALSO THE SAME

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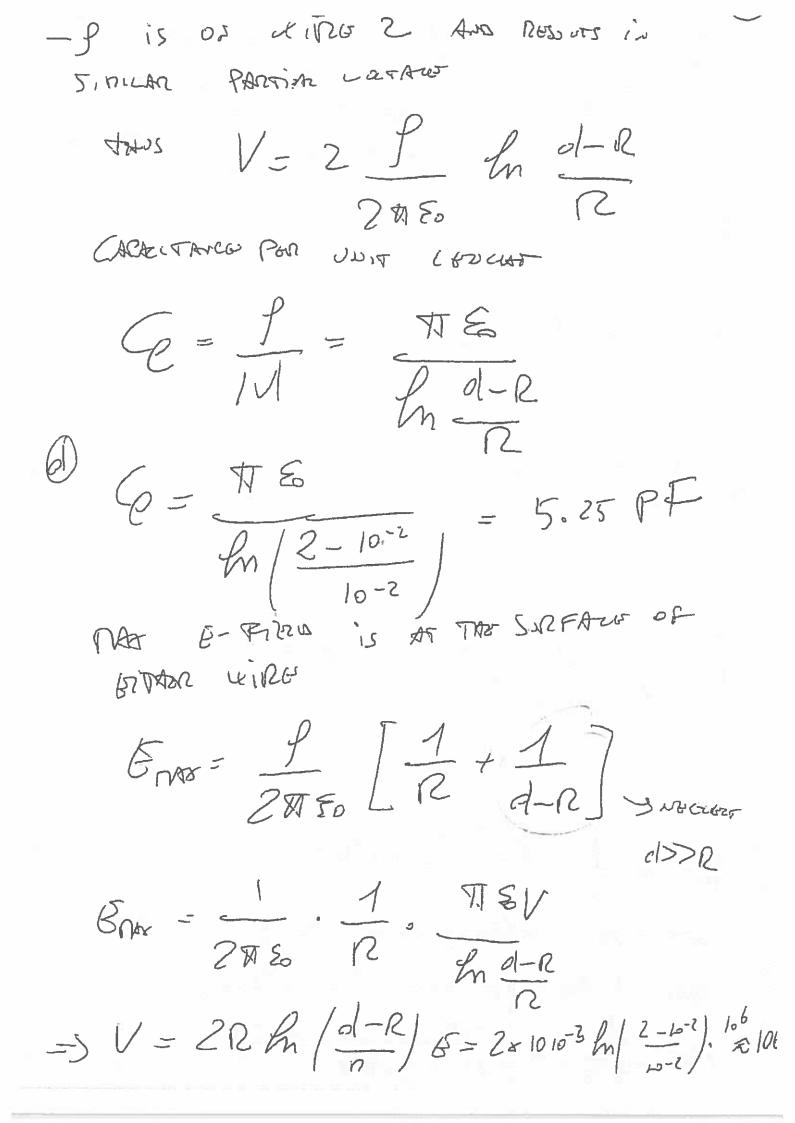
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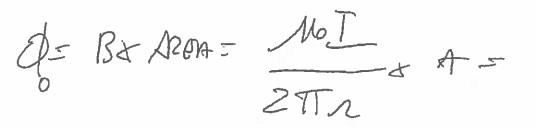
 $V = \int_{R}^{d-R} \frac{\partial}{\partial r} \int_{S} \frac{dn}{\partial r} = \frac{P}{2\pi s_{0}} \frac{h(d-R)}{R}$



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 $V = N d \left[\frac{\Phi_0 \sin \left(2\pi f t \right)}{2} \right]$ olt

V= 1 \$ 277 f Cos (271 f t)

 $i_{1TH} N = MB_{00} \circ P ONDS Brif = 50 H 7$ PEAN VOLTAGE VP 44100 65(200ft) = 1 $N = \frac{VP}{100} \frac{210^{-6}}{50} = 24$