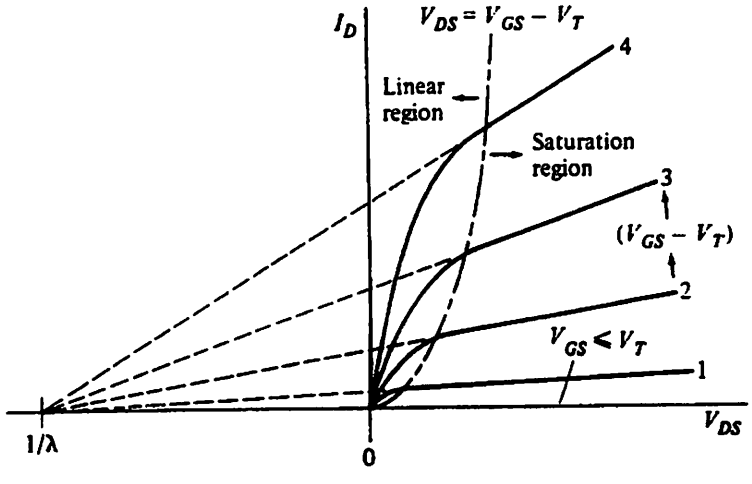
3B2 Crib 2015

Qn 1. For MOS transistors, saturation describes the region of operation where the channel is pinched off near the drain. This typically corresponds to high values of V_{DS}. The necessary condition is (for n-channel) :

$V_{DS} > V_{GS} - V_T$

If $V_{DS} = V_{GS} - V_T$, pinch-off happens right at the drain. As V_{DS} increases, the pinch-off region advances progressively towards the source. To a first approximation, I_D remains unchanged as V_{DS} increases, and the device acts as a constant current source/sink. In fact, as V_{DS} increases, the resultant shortening of the channel (channe length modulation) slightly enhances the conductance, and brings about a gradual increase in I_D.



The near constant current is a useful characteristic in linear circuits.

Also, a FET connected with D and G shorted together is by definition in saturation, and may be used as a load in place of a resistor – it also occupies much less space.

n-channel enhancement mode MOSFET

Vertical scale greatly exaggerated to emphasise channel-length modulation effect

(ii) For bipolar devices, saturation is observed when the base potential V_{BE} causes a large collector current to flow. Assuming a load is connected between collector and supply, V_{CE} falls to a low limiting value V_{CEsat} (typically ~0.2 V), and is definitely less than the value of V_{BE} (under these conditions about 0.7 to 0.8 V).

In this situation $V_{CB} < 0$ (NPN), and the c-b junction becomes forward biased. The collector injects electronic charge into the base, accounting for some excess base current. In bipolar, saturation gives a clearly defined low V_{CE} with a typically higher-than-usual V_{BE} and I_B, and a large I_E. The low V_{CE} can be used to define a logic level (as in saturated-mode bipolar logic). The excess charge stored in the base has to be removed before the device can leave saturation and stop conducting, This takes o(50ns) and limits switching speed available with saturated bipolar logic.

(b) In this circuit, for T2, $V_{DS} \equiv V_{GS}$ since D is shorted to G. Hence by definition $V_{DS} > V_{GS} - V_T$, so T2 is known to be in its saturation mode. We cannot know for certain the state of T1, since Vout is at this point unknown, but we shall assume that, because V_{GS} is high, V_{DS} will likely be low, with that device in its non-saturation state. We must verify this at the end.

Hence we use the first of the given equations for T1, the second for T2
Assuming no current is drawn from the output, we equate I_{DS} for T1 and T2.

$$I_{D1} = \frac{k_1}{2}\left[2(V_{GS_1} - V_T)V_{OUT} - V_{OUT}^2\right] = I_{D_2} = \frac{k_2}{2}(V_{GS_2} - V_T)^2$$

For T1, $V_{GS1} = 6$V. for T2, $V_{GS2} = V_{DD} - V_{OUT} = 12 - V_{OUT}$

$$\frac{120}{2}\left(2(6-1)V_{OUT} - V_{OUT}^2\right) = \frac{20}{2}(12 - V_{OUT} - 1)^2$$

$$60V_{OUT} - 6V_{OUT}^2 = 121 - 22V_{OUT} + V_{OUT}^2$$

$$7V_{OUT}^2 - 82V_{OUT} + 121 = 0$$

Solving,

$$V_{OUT} = \frac{82 \pm \sqrt{82^2 - 4\times 7\times 121}}{14}.$$ Hence V_{OUT} = 5.86 ± 4.13 V

= 1.73 or 9.99 V. The second root is inconsistent with T1 being in its non-saturation region. Hence the first root applies, and V_{OUT} = 1.73 V

(c) σ describes the degree of saturation of the bipolar circuit. σ = 1 means the circuit is not saturated, σ = 0.1 means it is heavily saturated.

σ is defined as $I_C / h_{FE}\, I_B$. If σ = 0.2, then the base current drive is 1/0.2 × that required to sustain collector current I_C, and the circuit is well into saturation, so V_{CE} may be taken as V_{CEsat}.

Hence $I_C = \frac{V_{CC} - 0.1}{R_L} = \frac{5.9}{2000} =$ 2.95 mA

And $I_B = \frac{I_C}{\sigma h_{FE}} = \frac{2.95\times 10^{-3}}{0.2\times 50} =$ 295 μA

If V_{BEsat} = 0.7 V, we may apply KVL to get V_B, which is given by :

$$V_B = I_B R_B + V_{BEsat} = 295 \times 10^{-6} \times 5000 + 0.7 = 1.57\text{ V}$$

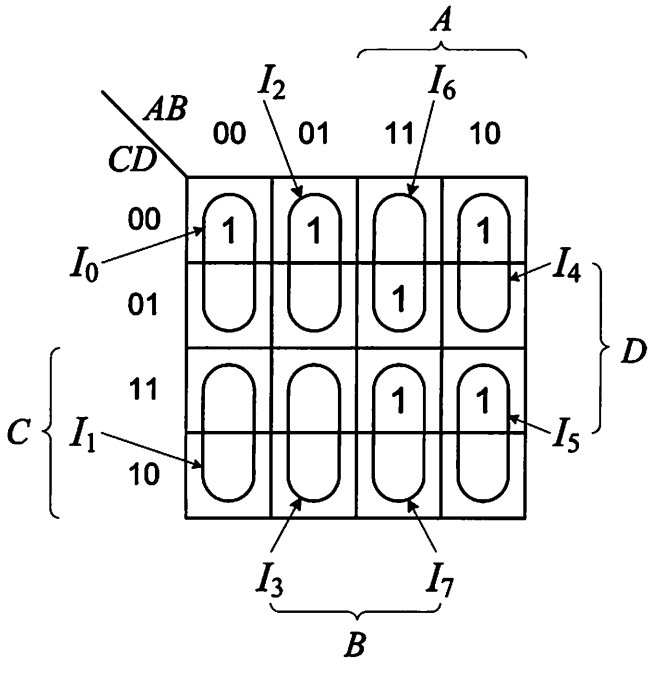
Examiner's note:

Not all candidates could decide which root of the quadratic to use. There was much variation in the answers to the descriptive parts, and many lacked important detail.

2 (a) The Quine-McClusky tabular method is based on building lists with adjacent blocks containing the same number of 'High' variables. By comparing, and if appropriate, combining each term from one block with the block below we build subsequent lists . The terms that did not combine in each list (including the last) are termed 'Prime Implicants' (PIs). The 'Prime Implicant table' is formed of the PIs and the original terms of the logic function. The idea is to select the minimal and the simplest PIs which cover all the original terms. This can be done by visual inspection or by a formalised method.

If the logic function is not in a canonical form (or not brought to a canonical form) it is difficult to deal with terms that have fewer variables. Such terms may be introduced in the second or subsequent lists but this results in missing the chance to combine parts of them (canonical components of such terms) with other terms from the first list (or previous lists) and thus the method does not always deliver an optimal solution.

(b) The implementation using the multipler can be done by using a Mutiplexer specific Karnaugh map.



$I_0 = D_0 = \overline{D}$ $S_0 = A$

$I_1 = 0$ $S_1 = B$

$I_2 = \overline{D}$ $S_2 = C$

$I_3 = 0$

$I_4 = \overline{D}$ $T = D_{out}$

$I_5 = D$

$I_6 = D$

$I_7 = D$

(c)

(i) When power is first applied, the capacitor will charge up to 5V. This acts as power-up reset. When START is pressed Q_D goes ***high*** *and stays* ***high*** *after the button is released. With Q_D* ***high*** *the counter begins to count. This is a usual counter that counts in a decimal sequence 0-1-2-3-4-5. When 5 is reached then the output of the NAND gate goes* ***low*** *turning on the LED (the LED needs a voltage drop across it and a minimum current to be lit). The* ***low*** *output of the NAND gate also appears at the input of the AND gate which will disable the clock input. The counter will then stay at 5 and the LED lit.*

To reset the counter to zero one can press the RESET button so that Q_D goes ***low*** *and will stay* ***low*** *until the start button is pressed again. Without the RESET button, the LED will stay lit.*

(ii) The current that flows through the LED is all sank by the output of the NAND gate (the AND gate will have a high impedance input and therefore will not sink any current). This current is (5 V - 1.7 V)/300 Ω = 11 mA. Therefore the NAND gate should be able to sink 11 mA without burning out !

Most people could do the implementation of a combinational function using a MUX. Some candidates tried using both gates and a 4 to 1 MUX, but the correct and simpler solution was to use a 8 to 1 MUX

3.(c) • Multiplexers are suitable for single output functions, (preferably with few variables).

• ROMs are better for multiple-output functions but they become expensive and less efficient for a very high number of variables

• PLAs are good for multiple-output functions with lots of variables. There are expensive unless the number of variables are too high for a ROM. [20%]

(5) Unique sequences of inputs which lead to releasing the drink.

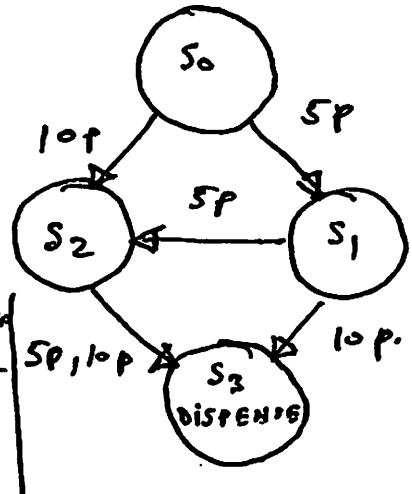
(1) 5p + 5p + 5p

(2) 5p + 5p + 10p (no need given)

(3) 5p + 10p.

(4) 10p + 5p

(5) 10p + 10p.



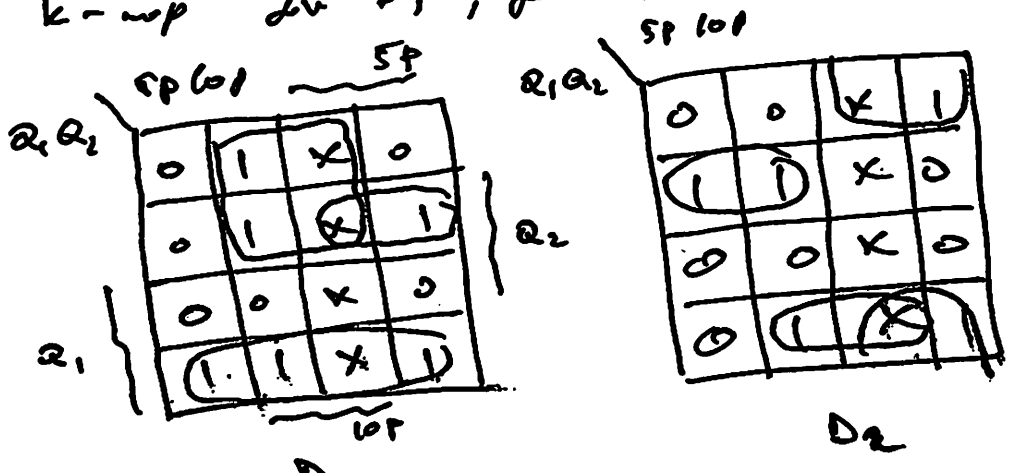
Present state		Next state for input 00	01	11	10	DISPENSE
S_0	00	00	10	–	01	0
S_1	01	01	11	–	10	0
S_2	11	00	00	–	00	1
S_3	10	10	11	–	11	0

Le. output

DISPENSE	INPUTS A	B	OUTPUT
0	—	—	— (NONE)
1	0	0	COFFEE
1	0	1	HOT TEA
1	1	0	CAP
1	1	1	

[30%]

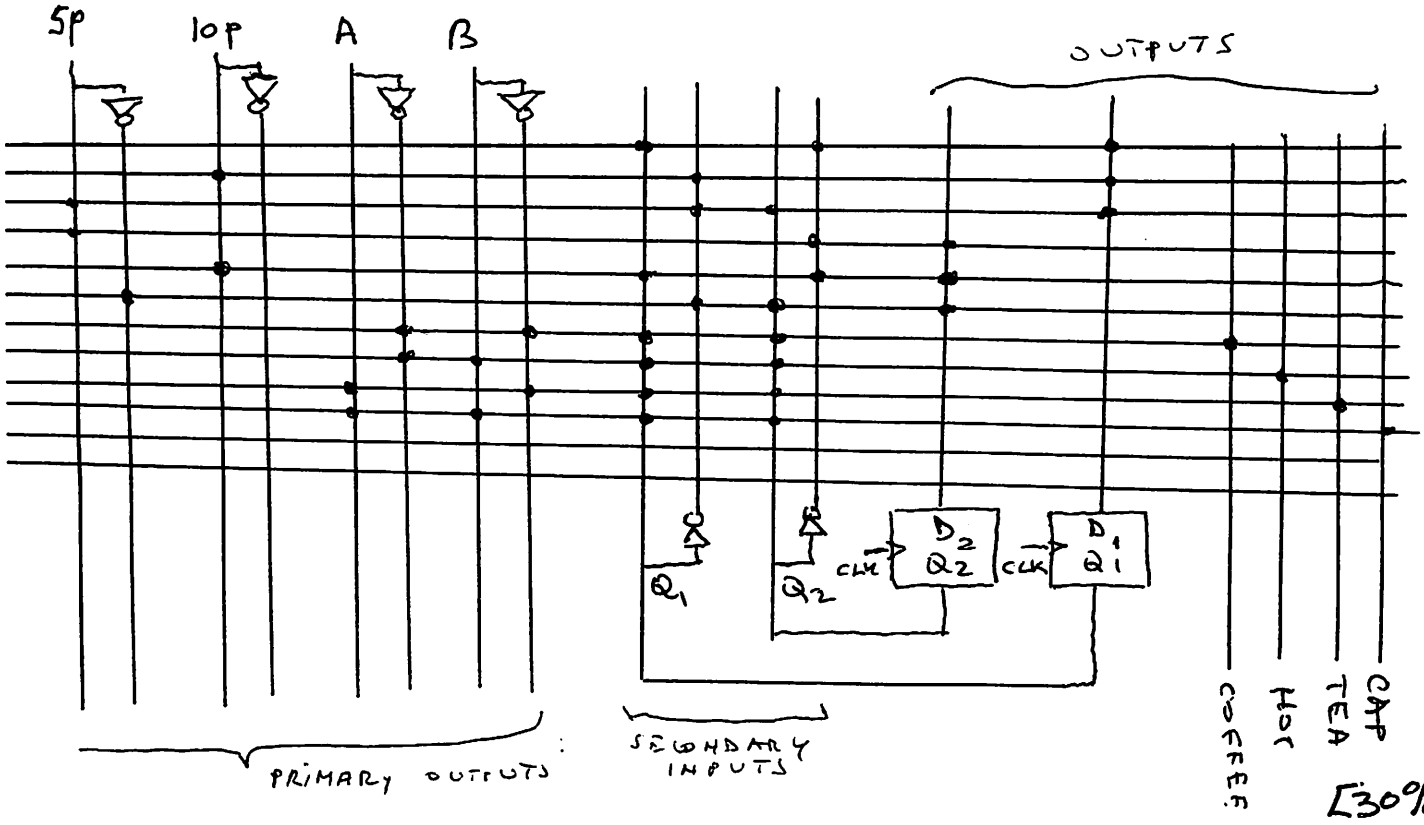
k-map for D_1, for D_2



DISPENSE $= Q_1Q_2$

$$D_1 = Q_1\bar{Q}_2 + lop\,\bar{Q}_1 + 5p\cdot\bar{Q}_1Q_2$$

$$D_2 = 5p\bar{Q}_2 + lop\,Q_1\bar{Q}_2 + \bar{5p}\,\bar{Q}_1Q_2$$



[30%]

There are no essential hazards. 5p, 10p, A, B are inputted sequentially by hand. These inputs cannot move as fast as the outputs. The time for the decoding inputs (Q_1, Q_2 and Displ. To be available at the input is order of tens of nanoseconds. Inputs must change so quickly [20?]

Examiners note Q3

Some candidates did the complete design and implementation. Not all the candidates were able to understand what essential hazards are

Qn 4 (a) Historically logic circuit development began with bipolar devices operating between saturation and cut-off. Available process technologies encouraged this development in an evolutionary rather than revolutionary way. For saturating bipolar technology:

Advantages:

- superiority over passive (e.g. diode-based) logics
- technological simplicity
- adequately suited to integration
- some scope for enhancement (e.g. use of schottky diode technology)

Disadvantages:

- high device count per function
- high power consumption
- low input resistance
- long propagation times
- limited enhancement potential via scaling

The main problem to be surmounted was the undesirable switching delay as devices exit saturation. This was partly resolved by use of Schottky transistors. TTL, S/LS TTL, ALS TTL were the primary technology on which the emergence of digital computing depended. Fastest logics ran at c. 100 MHz and required a fixed 5V supply. Limited switching speed was circumvented with the introduction of current-mode or non-saturating logic e.g. ECL.

Advantages

- very high speed, to > 1GHz in recent forms
- constant power consumption (approx) leading to:
- good overall noise characteristics

Disadvantages

- very high consumption
- poorly suited to large-scale integration

The introduction of ion implantation facilitated the full development of complementary MOS technology, allowing accurate positioning of n dopants in p substrates and v.v. For CMOS:

Advantages

- very low consumption for LF applications
- very good noise immunity (up to 0.4 VDD for inverter)
- fully restored logic outputs, 0V and VDD
- operable over range of supply voltages
- gate inputs draw no current, easy to drive
- highly suited to integration
- scales well (consumption & speed improve as devices shrink)
- usable up to about 60GHz

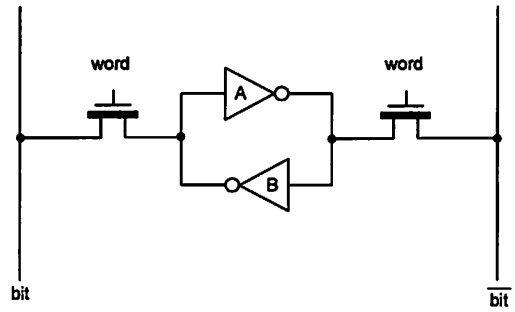
Disadvantages

- comparatively poor drive capability
- not as fast as best bipolar forms for significant loads
- sensitivity to static breakdown
- consumption increases with operating frequency > 1GHz
- liability to destructive latch-up (poor design or peripheral failures)

With CMOS the dominant mode of energy loss is dynamic dissipation as nodal capacitances are charged/discharged. Straightforward design approaches involve multiple devices and significant nodal capacitances; much effort has gone into circuit abstraction. The excellent drive capability

of bipolar is utilised in BiCMOS which has superior performance driving large. Recent emergence of Ge-doped Si semiconductors offers still greater speed improvements up to about 100 GHz. Use of III/V semiconductors, e.g. GaAs MESFETS offers delays o(1 ps) but large scale integration is not yet practicable.

(b) The RAM cell consists of a pair of cross-coupled inverters whose inputs may be accessed by means of switching transistors controlled by the **word** signal.



The cell can be in either of two stable states, corresponding to a stored logic '0' or logic '1'.

If inverter B is generating logic '1' that will cause A to output logic '0', which will cause B to output logic '1', so maintaining the original value.

The same argument hold is inverter B is generating logic '0', giving '1' at A's output, so maintaining this continuous set.

Hence the RAM cell may assume only two states and if isolated from external influences it will retain its state while power is applied. This state may be changed, i.e. data *written*, by driving the vertical **bit** and **bit** lines to new complementary values, and operating the switching transistors by setting the word lines high. The RAM cell inverters must be sufficiently weak (by design) that the bit-line signals can override the signals currently being output by the inverters and switch them into a new state when necessary. It follows also that the driver stages from which the input data is taken must have much greater drive capability, to obtain quick and decisive switching to the new state. Once this has been achieved, the word lines are reset to low, disengaging the switching transistors.

To read out data, both bit-lines are preset to precisely the same voltage, typically the mean of V_{low} and V_{high}. The lines are connected to sensitive comparators, which will initially indicate the equivalence of the signals on the lines. The switching transistors are then enabled. One inverter will drive its corresponding bit-line low, the other high – by a few millivolts. This is because the inverters are designed deliberately with low drive power ('weak'), and the bit-lines represent a substantial capacitive load whose charge is only slightly modified by the influence of the new incremental charges delivered by the two inverters.

The comparator output will then indicate logic '0' or logic '1', according to the sense of the perturbations introduced to the bit-lines by the RAM cell.

To achieve the necessary 'weak' inverters, these are typically implemented using CMOS devices with low values of W/L, leading to low device conductances.

(Block diagram to be inserted)

The additional circuit elements required are:

- Address decoder to select a specific horizontal row of cells to be manipulated
- Bank of sensitive comparators (alternatively called sense amplifiers). Design of these is a challenge since they must combine sub-mV sensitivity with high slew rate to read out the data fast.
- Column decoder, to select the output from a specific sense amplifier from the bank, and connect it to the output pin/s; also (for *write* operations) to connect the input data to the chosen set of bit lines.

Read/write control circuitry, which may allow the multiplexed use of a single pin for both input and output.

Examiners note Q4

Many missed key points, for example, noise margins. Some accounts were very poorly structured. The section on the static RAM was quite well done, and the majority could explain the function of the signals and how to write data into the device. Reading data and the explanation of the use of weak inverters were less well covered. Very few had much idea of what interface circuitry would be required