Qn 1.

(a) **Main reasons for popularity of CMOS**:

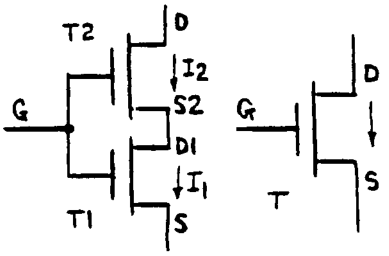
- Gate inputs are effectively open-circuit, very high impedance, easy to drive
- Power supply current for static/low frequency apps is very low, ideal for battery-powered portable devices
- Very good noise immunity, ~0.4 V_{DD} for inverter both low and high states (not quite so high for multi-input gates)
- Fully restored logic levels V_{DD} and 0V
- Can operate over wide range of supply voltages
- Creates little electrical noise
- Easily integrated with linear circuitry for complex mixed-signal designs

Main disadvantages:

- Not as fast as GaAs or some forms of bipolar
- Comparatively sensitive to static breakdown
- Liable to destructive latch-up as compound doped layers form thyristor-like structures

(b) As all devices are operating in non-saturation, we can write for I_2 in T_2:

$$I_2 = \frac{k'}{2}\frac{W}{L_2}\left[2(V_{GS2} - V_T)V_{DS2} - V_{DS2}^2\right]$$



Hence $I_2\frac{2L_2}{k'W} = \left[2(V_{GS2} - V_T)V_{DS2} - V_{DS2}^2\right]$

(1)

Similarly for I1 in T1

$$I_1\frac{2L1}{k'W} = \left[2(V_{GS} - V_T)V_{D1S} - V_{D1S}^2\right]$$

(2)

Note that: $V_{GS2} = V_{GS} - V_{D1S}$ and $V_{DS2} = V_{DS} - V_{D1S}$; substitute (2) into (1)

$$I_2\frac{2L_2}{k'W} = \left[2(V_{GS} - V_{D1S} - V_T)(V_{DS} - V_{D1S}) - (V_{DS} - V_{D1S})^2\right]$$

$$= [2(V_{GS} - V_T)V_{DS} - 2(V_{GS} - V_T)V_{D1S} - 2V_{D1S}V_{DS} + 2V_{D1S}^2 + V_{DS}^2 + 2V_{DS}V_{D1S} + V_{D1S}^2]$$

$$= [(2(V_{GS} - V_T)V_{DS} + V_{DS}^2) - (2(V_{GS} - V_T)V_{D1S} - V_{D1S}^2)]$$

By inspection, the second term inside the [] square brackets is equivalent to the RHS of (2). So substituting:

$$I_2\frac{2L_2}{k'W} = \left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right] - I_1\frac{2L_1}{k'W}$$

But by Kirchhoff $I_2 = I_1 = I$, say. Hence,

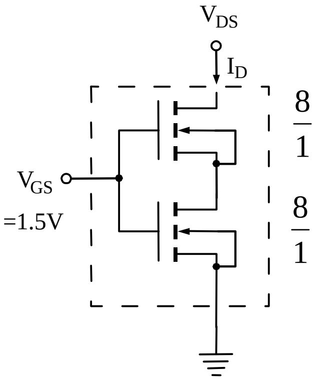
$$\frac{2I(L_1 + L_2)}{k'W} = \left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right], \text{which gives}$$

$$I = \frac{k'}{2}\frac{W}{L_1 + L_2}\left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right]$$

By inspection, this is the current that would flow in a single device T of width W and length $L_2 + L_1$, and whose electrode voltages are V_{GS}, V_{DS} as shown.

(c) The NAND gate with shorted inputs contains two parallel-connected p-type devices of aspect ratio 4 / 1, and two series-connected n-channel devices of aspect ratio 8 / 1. The parallel devices are equivalent to a single p-channel device of aspect ratio (4 + 4) / 1 or 8 / 1. The n-type devices are governed by the relation derived in part (b).

From (b), the equivalent circuit for the n-type devices is:



For the n-type, (from above) $k_n = \dfrac{k_n'W}{L} = \dfrac{8 \times 8}{1+1}$ = 32 μA/V^2

(two series-connected devices)

For the p-type, $k_p = \dfrac{k_p'W}{L} = \dfrac{(4+4) \times 4}{1}$ = 32 μA/V^2

(two parallel-connected devices)

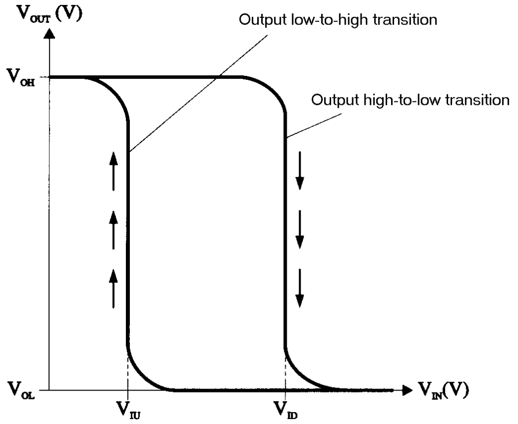
Hence, by symmetry, $V_{out} = V_{DS} = V_{DD}/2 = 1.5$ V, since for each transistor, $V_{DS} > V_{GS} - V_T$, and $|V_{GS}|$ is the same for the equivalent p- and n- devices.

Thus $I_D = \dfrac{k_n}{2}(V_{GS} - V_T)^2 = \dfrac{32}{2}(1.5 - 0.5)^2$ = 16 μA

This question comprised a descriptive section followed by straightforward application of the MOS equations to serial and parallel-connected devices, but the answers seen spanned a wide range. Most candidates knew some of the advantages and disadvantages of CMOS, but several overlooked key factors e.g. noise margins, static sensitivity, latch-up. The analysis based on the Schichmann-Hodges equations was not on the whole well done, but a number of candidates were able to complete it fully. Section (c) on the NAND gate was made easier by application of the result of section (b) to the series devices, but several candidates had difficulty dealing with the parallel-connected pair.

Qn 2 (a) In the conventional CMOS logic inverter, the low-to-high and high-to-low transitions occur at the same input voltages. In the Schmitt gate the phenomenon of HYSTERESIS is exhibited, where the L-H and H-L transitions occur at different input voltages.

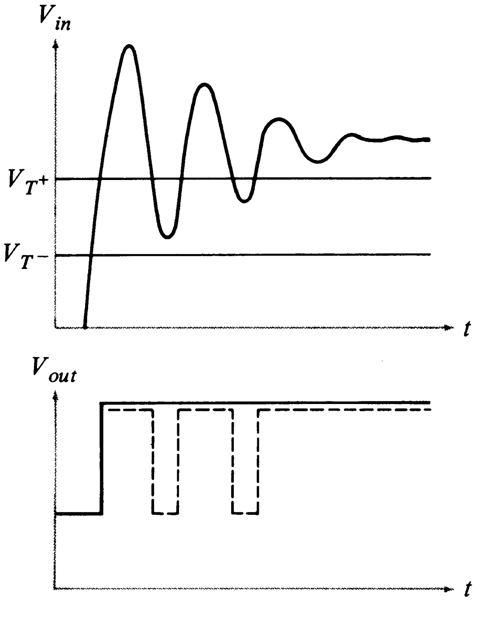
The voltage transfer characteristic exhibits a hysteresis loop as shown in the Schmitt inverter characteristic.



- V_{OUT} makes its H-L transition when the *rising* input voltage exceeds
- V_{OUT} makes its L-H transition when the *falling* input voltage drops below
- The condition $V_{ID} > V_{IU}$ must hold.
- $V_{ID}–V_{IU}$ is referred to as the *hysteresis* of the gate.

[30%]

(b) If the input V_{IN} exhibits noise, the hysteresis characteristic is helpful in cleaning up and conditioning the signal for digital processing. This may be used to advantage in line receiver applications. Because of the fast transition times in high speed digital systems, and the intrinsic parasitic series inductance and parallel capacitance of a signal wire, the voltage pulse seen at the end of a long line might be as below (characteristic ringing).



The output of a simple inverter with switch level V_{ID} would exhibit additional spurious pulses.

Setting the switching level to V_{IU} would not necessarily solve the problem as it might cause triggering on other noise events.

The output of a Schmitt inverter with thresholds V_{ID}, V_{IU}, as described would alleviate this effect in a single step, as required.

The Schmitt inverter can also be used for converting non-digital signals (e.g. sine waves) to a digital pulse train.

[20%]

(c) The circuit shown resembles a CMOS inverter in that it comprises a stack of two series-connected PMOS devices (PI, PO) and two series-connected NMOS devices (NI, NO), with the inputs common. The output is taken from the centre of the stack. As so far described the function would be that of a simple inverter. The provision of additional devices (NF, PF) provides a form of positive feedback.

With V_{IN} at ground, NI is cut off, hence no current path is available in the stack. However, PI is highly conductive (in the non-saturated mode), and its drain is therefore at a virtual V_{DD} potential. Hence V_{GS} for PO is sufficient to bring it into its non-saturation region. There is thus a conductive pull-up to V_{DD}, and since the drain current in the NMOS devices is zero, there is negligible voltage drop across PI and PO. Hence the output voltage is:

$$V_{OH} = V_{DD}$$

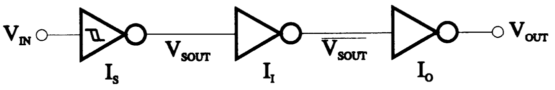
This would remain for V_{IN} between 0V and V_{TN}. By symmetry, if V_{IN} lay between V_{DD} and $V_{DD} - |V_{TP}|$, the output would lie at a low level, with conductive pull-down to 0V such that:

$$V_{OL} = 0$$ [30%]

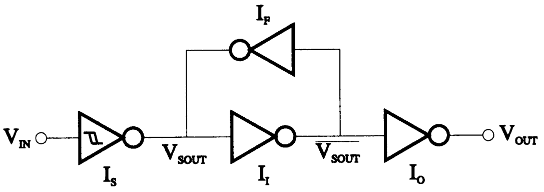
(d) The purpose of the circuit is functionally an inverter. Comparing the input circuitry with that of a standard inverter, we see the input drives 4 gate electrodes (cf 2 in the inverter proper). For unit current comparability, the W/L ratio for the Schmitt transistors (being in series) must be twice those of the standard inverter. Assuming both designs use the same L value, it follows that in the Schmitt gate there are twice as many transistors, each of twice the area, so that the previous stage must drive about 4 times the capacitance of an inverter of equivalent drive strength.

Increasing the size of the Schmitt transistors to increase the drive capability could increase the input capacitance to an unmanageable level.

Hence, if a CMOS Schmitt inverter with large current drive is required, it is best to use the smallest practicable transistors in the Schmitt stage itself, but to follow it with a further inverter (or pair of inverters to achieve the correct polarity).



Buffered Schmitt Inverter



Buffered Schmitt inverter with feedback

The dimensions of all devices in the buffers I_I and I_O may each be made greater than those of the preceding gate to achieve still greater drive capacity. A figure of 3× is commonly used. Optionally, the feedback inverter I_F may be incorporated. This applies positive feedback to the input of the first stage, improving the transient response when the input is extremely noisy. I_F must be made from transistors with lower current capability than I_S, so that its output can always be overruled by the output of I_S, V_{SOUT}. Typically their conductance might be 1/3 of the corresponding parameter for PO, NO, and the structure is sometimes referred to as a 'trickle' inverter. [20%]

On the whole, this question was quite well done. Most candidates understood the basics of Schmitt trigger operation and could ***produce*** *a labelled voltage transfer characteristic. The majority showed awareness of the use of the Schmitt trigger as a line receiver, but accounts differed widely in the amount of detail given. A number had difficulty determining the expected values of* V_{OH} *and* V_{OL}*. Rather few understood the need for buffering or how to apply it.*

3. (a) The terms 0, 2, 16, 18, 24, 26, 28, 30 are put into list 1 in order of how many variable of ‘1’ they contain.

LIST 1

0	00000	√
2	00010	√
16	10000	√
18	10010	√
24	11000	√
26	11010	√
28	11100	√
30	11110	√

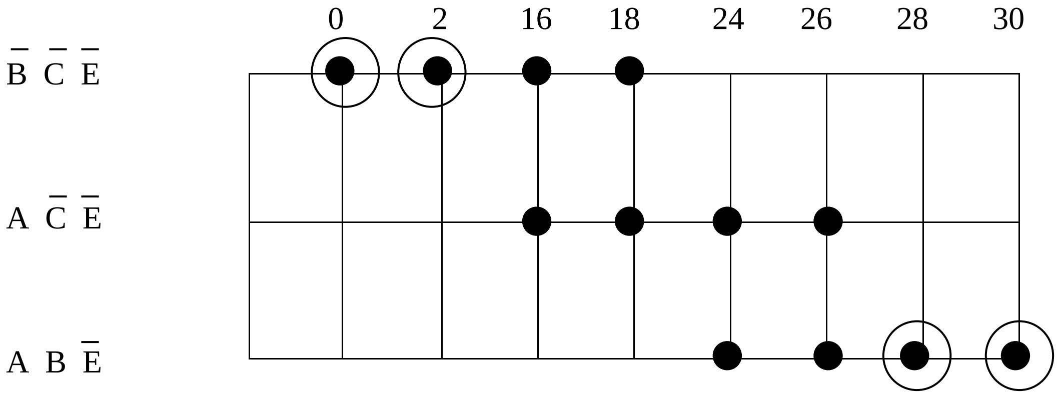
LIST2

0,2	000x0	√
0,16	x0000	√
2,18	x0010	√
16,18	100x0	√
16,24	1x000	√
18,26	1x010	√
24,26	110x0	√
24,28	11x00	√
26,30	11x10	√
28,30	111x0	√

LIST 3

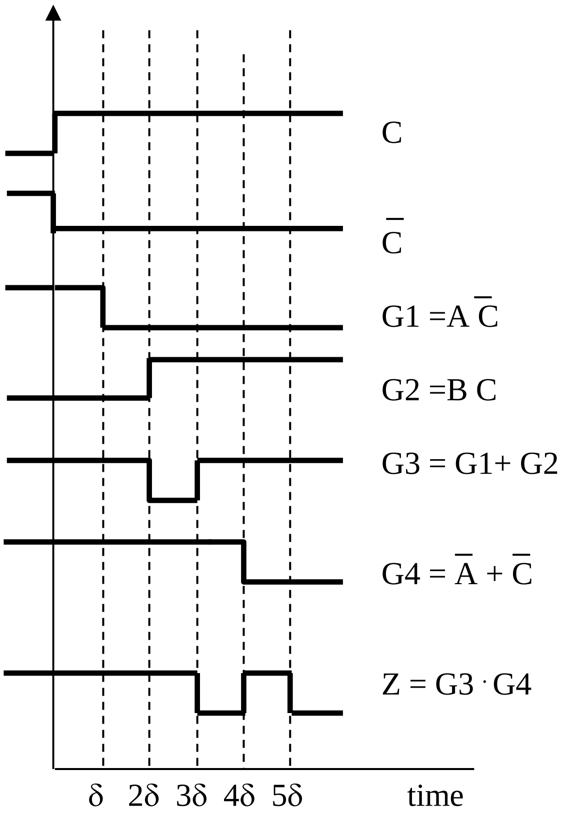
0,2,16,18 0,16,2,18	x00x0	$\overline{B}\ \overline{C}\ \overline{E}$
16,18,24,26 16,24,18,26	1x0x0	$A\ \overline{C}\ \overline{E}$
24,26,28,30 24,28,26,30	11xx0	$A\ B\ \overline{E}$

All the terms from lists 1 and 2 have combined according to $PQ + P\overline{Q} = P$. The list 3 contains all the Principal implicants (PIs) that can be put in a PI table.



Top and bottom PIs are essential. They also recognise all the original terms. So the simplest expression is $\overline{B}\ \overline{C}\ \overline{E} + A\ B\ \overline{E}$ [40%]

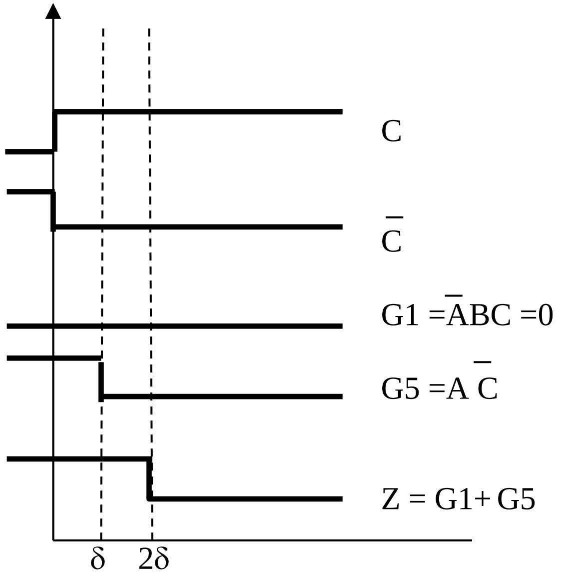
(b) The input C is used in three different paths. A dynamic hazard is possible.

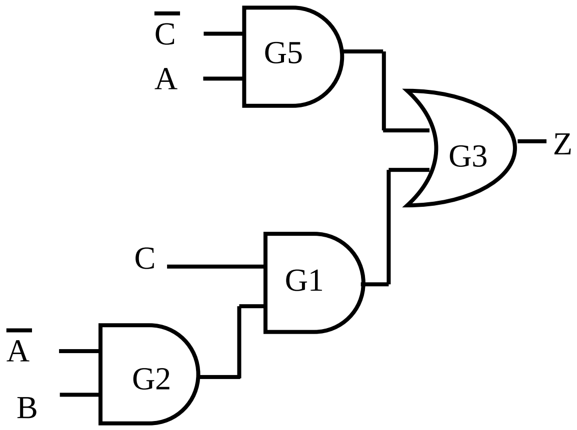


There is a **dynamic** hazard as the output changes from 1 to 0 to 1 to 0 before it settles down after 5 δ.

[30%]

The expression is Z = (AC’ + BC) (A’ +C’) = AA’C’ + A’BC + AC’ + BCC’. The last term gives the hazard. The expression is equivalent to A’BC+ AC’ = (A’B)C + AC’





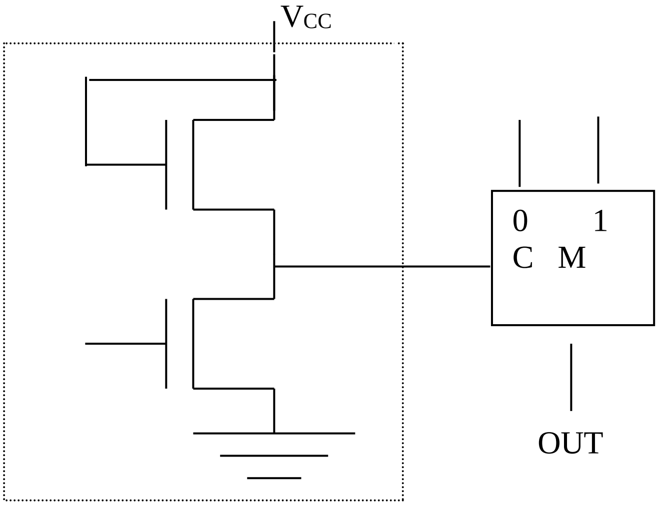
The minimal delay in the output when C changes from 0 to 1 for A=B=1 can be obtained as 2δ. This is because G2 does not switch. [20%]

For better overall speed (when A and B also change, one can swap G2 and G5 given a total delay of 3δ. From the time diagram one can see that the hazard is removed. [10%]

The question was very popular and very well answered. Not all the candidates were able to solve the dynamic hazard but almost all were able to draw timing diagram and spot it. It was very pleasing to see that most of the candidates were able to understand the tabular method and the occurrence of hazards which is related to different time delays in a series of gates.

4. (a) The control circuits connected to M_1 and M_2 are NMOS inverters.

G = 0 ⇒ C = 1
G = 1 ⇒ C = 0



NMOS INVERTER

- **If $G_1 = 1$** ⇒ $C_1 = 0$ ⇒ I/O_2 is configured as input, $I/O_2 = I$. The input I is selected at the M_1 multiplexer and becomes (or not) an input in the PAL function of the signal G2.
  - **$G_2 = 1$** ⇒ $C_2 = 0$, B3 is open circuit and therefore
    $O_1 = \overline{X}\,\overline{Y} + \overline{X}Y + \overline{Y}X + XY = 1$
  - **$G_2 = 1$** ⇒ $C_2 = 1$ In this case the macro-cell behaves as a single output combinational circuit with 3 inputs X, Y, I. The logic function implemented is that of binary adder (with no carry):
    $O_1 = \overline{X}\,\overline{Y}I + \overline{X}\,\overline{I}Y + \overline{I}\,\overline{Y}X + XYI = X \oplus Y \oplus I$

- **If $G_1 = 0$ and $G_2 = 1$** ⇒ $C_1 = 1$, $C_2 = 0$

B_2 and B_3 are inactive (open circuit) and $I/O_2 = O_2$.
The bistable is bypassed and the macro-cell behaves as a two output combinational network with two inputs.

$$\begin{cases} O_1 = \overline{X}\,\overline{Y} + \overline{X}Y + \overline{Y}X + XY = 1 \\ O_2 = XY \end{cases}$$

- **If $G_1 = 0$ and $G_2 = 0$** ⇒ $C_1 = 1$, $C_2 = 1$

B_1, B_2 and B_3 are shortcircuits, M_1 and M_2 select the input “1”. The cell behaves as a MEALY sequential circuit (as the output depends on both the present state and the primary inputs). There are two outputs O_1 and O_2. The inputs to the bistable JK are:

J = XY

$K = \overline{X}\,\overline{Y}$ [40%]

(b) Using the JQ bistable equation and the reverse method we can work out Q^+ and the inputs to the bistable, J and K.

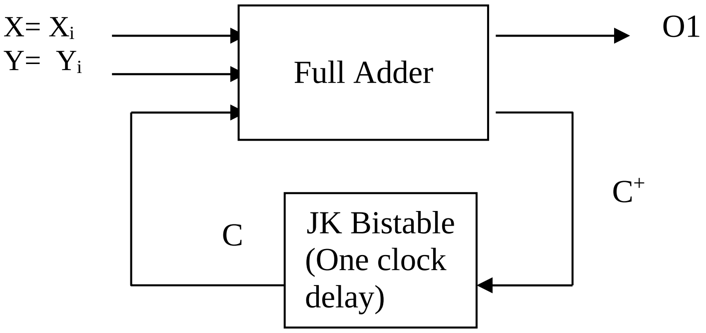
$$Q+ = \overline{Q}J + Q\overline{K} = \overline{Q}XY + Q(X + Y)$$

$$O1 = X \oplus Y \oplus Q$$

XY	**Q**	Output O1	Next state Q^+	JK
00	0	0	0	0x
00	1	1	0	x1
01	0	1	0	0x
01	1	0	1	x0
10	0	1	0	0x
10	1	0	1	x0
11	0	0	1	1x
11	1	1	1	x0

[30%]

(c) This is a serial binary adder. The XY are the inputs Xi Yi (serially entered). Q is the Carry. Q+ is the C+ and O1 is the output (the sum)



C = carry bit (present state)
C^+ = next carry bit (next state)

[30%]

This question was attempted by 30 candidates and was answered to a good standard. The majority were able to identify different modes of operation for the macro-cell (state-machine and combinational). Few have been able to work out that as a state-machine this particular macro cell played the role of a sequential full adder.