1 (a) **Main reasons for popularity of CMOS:**

- Easy-to-drive gate inputs thanks to very high impedance
- Very low power supply current for static/low frequency apps (ideal for battery-powered portable devices)
- Ability to operate with a wide range of supply voltages
- Creates little electrical noise
- High noise immunity, ~0.4 V_{DD} for inverter both low and high states

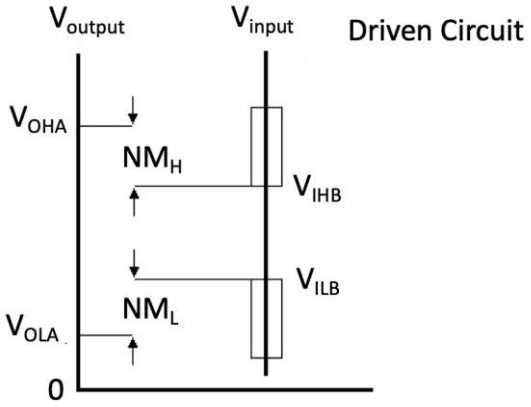
  (not quite so high for multi-input gates)
- Fully restored logic levels V_{DD} and 0V
- Easily integrated with linear circuitry for complex mixed-signal designs

Main disadvantages:

- Sensitive to electrostatic discharge
- Higher cost compared to the bipolar devices

[20%]

(b)



- V_{OHA}: The lowest voltage supplied by logic circuit A delivering High logic.
- V_{OLA}: The highest voltage supplied by an output delivering low Logic.
- V_{IHB} : The lowest input to B acceptable as High logic.
- V_{ILB} : The highest input to B acceptable as Low logic.

In a cascaded circuit, where the output of A is connected to the input of B, the noise margins observed in the High and Low states can be calculated as:

$NM_H = V_{OHA} – V_{IHB}$ and $NM_L = V_{ILB} – V_{OLA}$

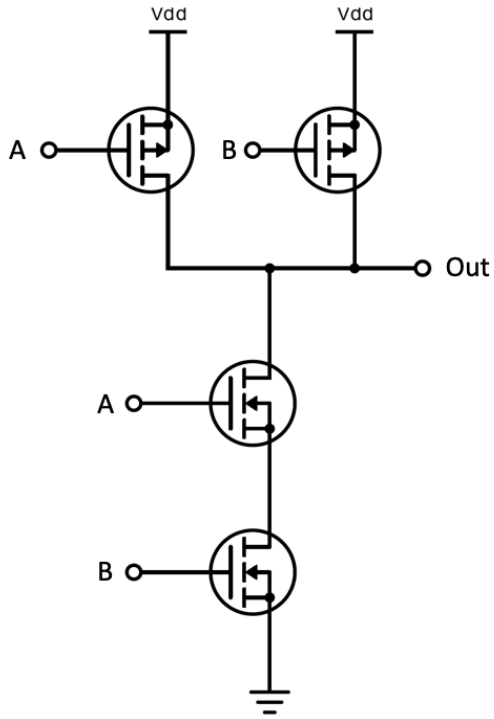
Both noise margins must be positive if the pair of circuits is to operate consistently.

The magnitudes of the noise margins must be δ or greater if superimposed noise of voltage magnitude up to δ is to be rejected.

Note that the voltages V_{OH} and V_{OL} are liable to depend on the magnitude of the current flowing in the corresponding output devices – i.e. they depend on fan-out.

[20%]

(c)



[20%]

(d) (i) As defined, V_{SP} is the point, at which V_O and V_I are equal. At this point both MOSFETs are in the saturation region, and hence $V_{DS} > V_{GS} - V_{T.}$ By using this we can write

$$\frac{k_N}{2}(V_{SP} - V_1 - V_{TN})^2 = \frac{k_P}{2}(V_{DD} - V_{SP} - |V_{TP}|)^2$$

$$\frac{k_N}{2}(V_{SP} - 2)^2 = \frac{k_P}{2}(4 - V_{SP})^2$$

$$\sqrt{\frac{k_N}{k_P}}|V_{SP} - 2| = |4 - V_{SP}|$$

Hence, the switching point is calculated as

$V_{SP} = \frac{4+2\sqrt{k_N/k_P}}{1+\sqrt{k_N/k_P}}$, for $V_{SP} \geq 2$

$V_{SP} = \frac{4-2\sqrt{k_N/k_P}}{1-\sqrt{k_N/k_P}}$, for $V_{SP} < 2$

(ii) For the switching point of $V_{SP=}\ V_{DD}/2=2.5\ V$, the k_n/k_p ratio can be determined as

$$2.5 = \frac{4 + 2\sqrt{k_N/k_P}}{1 + \sqrt{k_N/k_P}} \rightarrow \frac{k_N}{k_P} = 9$$

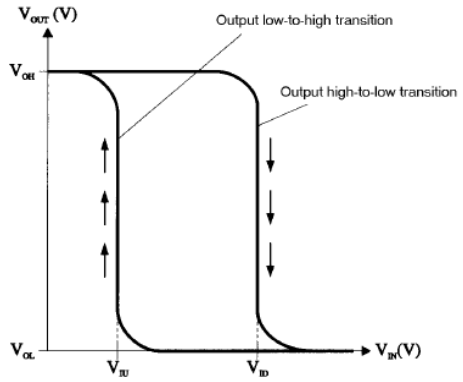
Therefore, the relationship between W/L ratios is calculated as

$$\frac{(C_{ox}\mu)_N W_N/L_N}{(C_{ox}\mu)_P W_P/L_P} = 9 \rightarrow \frac{W_N/L_N}{W_P/L_P} = 3 \rightarrow \frac{W_N}{L_N} = \frac{3W_P}{L_P}$$

and the minimum sizes for the transistor parameters are $W_N=3\ um$, $L_N=1\ um$, $W_P=1\ um$ and $L_P=1\ um$.

[10%]

2 (a) In the conventional CMOS logic inverter, the low-to-high and high-to-low transitions occur at the same input voltages. In the Schmitt gate the phenomenon of hysteresis is exhibited, where the L-H and H-L transitions occur at different input voltages. The voltage transfer characteristic exhibits a hysteresis loop as shown in the Schmitt inverter characteristic.



- V_{OUT} makes its H-L transition when the rising input voltage exceeds V_{ID}.
- V_{OUT} makes its L-H transition when the falling input voltage drops below V_{IU}.
- The condition $V_{ID} > V_{IU}$ must hold.
- $V_{ID} - V_{IU}$ is referred to as the hysteresis of the gate.

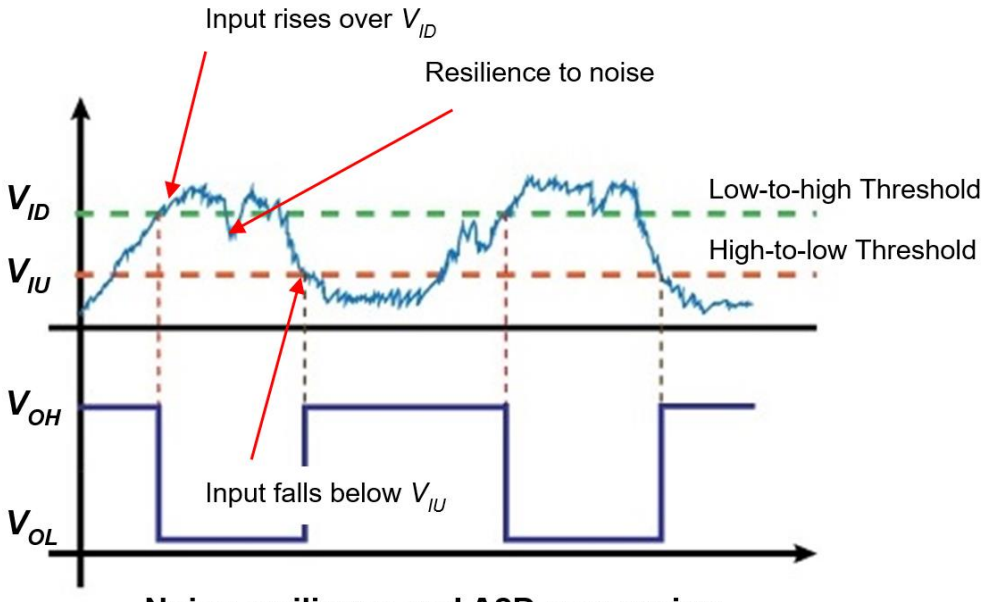
[30%]

(b) If the input V_{IN} exhibits noise, the hysteresis characteristic is helpful in cleaning up and conditioning the signal for digital processing. This may be used to advantage in line receiver applications. Because of the fast transition times in high speed digital systems, and the intrinsic parasitic series inductance and parallel capacitance of a signal wire, the voltage pulse seen at the end of a long line might be noisy (see figure below).

The output of a simple inverter with switch level V_{ID} would exhibit additional spurious pulses. Setting the switching level to V_{IU} would not necessarily solve the problem as it might cause triggering on other noise events.

The output of a Schmitt inverter with thresholds V_{ID}, V_{IU}, as described would alleviate this effect in a single step, as required.

The Schmitt inverter can also be used for converting non-digital signals (e.g. sine waves) to a digital pulse train.



Noise resilience and A2D conversion

[20%]

(c) The RAM cell consists of a pair of cross-coupled inverters whose inputs may be accessed by means of switching transistors controlled by the **word** signal. The cell can be in either one of two stable states, corresponding to a stored logic '0' or logic '1'.

If inverter B is generating logic '1' that will cause A to output logic '0', which will cause B to output logic '1', maintaining the original value. The same argument holds when inverter B is generating logic '0', giving '1' at A's output.

This state may be changed, i.e. data *written*, by driving the vertical **bit** and $\overline{\textbf{bit}}$ lines to new values, and operating the switching transistors by setting the word lines high. The bit-line signals override the signals held by the inverters and switch them into a new state when necessary. It follows that the driver stages from which the input data is taken must have much greater drive capability, to obtain quick and decisive switching to the new state. Once this has been achieved, the word lines are reset to low, disengaging the switching transistors.

To read out data, both bit-lines are preset to precisely the same voltage, typically the mean of V_{low} and V_{high}. The lines are connected to sensitive comparators, which will initially indicate the equivalence of the signals on the lines. The switching transistors are then enabled. One inverter will drive its corresponding bit-line low, the other high, by a few millivolts. This is because the inverters are designed deliberately with low drive power ('weak'), and the bit-lines represent a substantial capacitive load whose charge is only slightly modified by the influence of the new incremental charges delivered by the two inverters.

The comparator output will then indicate logic '0' or logic '1', according to the sense of the perturbations introduced to the bit-lines by the RAM cell.

[25%]

(i) As implied, the RAM cell inverters must be sufficiently weak (by design) that the bit-line signals can override the signals currently being output by the inverters and switch them into a new state when necessary. If the driver stages from which the input is taken have much greater drive capability, quick and decisive switching will result.

To achieve the necessary 'weak' inverters, these are typically implemented using CMOS devices with low values of W/L, leading to low device conductances.

[10%]

(ii) The additional circuit elements required are:

- Address decoder to select a specific horizontal row of cells to be manipulated.
- Bank of sensitive comparators (alternatively called sense amplifiers). Design of these is a challenge since they must combine sub-mV sensitivity with high slew rate to read out the data fast.
- Column decoder, to select the output from a specific sense amplifier from the bank, and connect it to the output pin/s; also (for *write* operations) to connect the input data to the chosen set of bit lines.
- *Read*/*write* control circuitry, which may allow the multiplexed use of a single pin for both input and output.

[15%]

3 (a) In a Mealy network, the primary outputs, Z=f(x,Q), are a function of primary inputs, x, and present states, Q, while in a Moore network, Z=f(Q) is a function of the present states only. A main difference compared to the Mealy network is that when a set of inputs is applied to the Moore network, the resulting outputs do not appear until after the clock pulse causes the flip-flops to change state.

Mealy – traffic light controller
Moore – counter (no input)

[20%]

(b) When both flip-flops are cleared, their outputs are $Q_0 = Q_1 = 0$. After the Clear input goes high, each pulse on the *x* input will cause a change in the flip-flops. Note that the figure shows the state of the signals after the changes caused by the rising edge of a pulse have taken place.

In consecutive time intervals the values of Q_1Q_0 are 00, 01, 10, 00, 01, and so on. Therefore, the circuit generates the counting sequence: 0, 1, 2, 0, 1, and so on. Hence, the circuit is a modulo-3 counter.

Time interval	Q_0			Q_1		
	J_0	K_0	Q_0	J_1	K_1	Q_1
Clear	1	1	0	0	1	0
t_1	1	1	1	1	1	0
t_2	0	1	0	0	1	1
t_3	1	1	0	0	1	0
t_4	1	1	1	1	1	0

[30%]

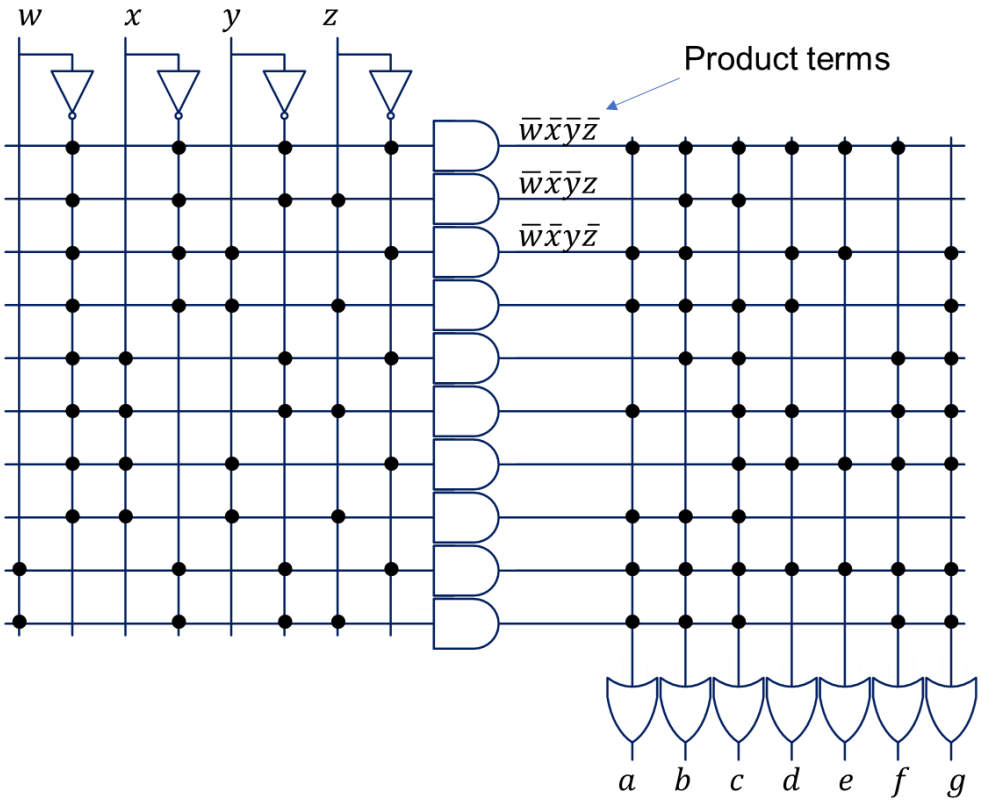
(c) (i) From Lecture 3

w x y z	*a b c d e f g*	Decimal number
0 0 0 0	1 1 1 1 1 1 0	0
0 0 0 1	0 1 1 0 0 0 0	1
0 0 1 0	1 1 0 1 1 0 1	2
0 0 1 1	1 1 1 1 0 0 1	3
0 1 0 0	0 1 1 0 0 1 1	4
0 1 0 1	1 0 1 1 0 1 1	5
0 1 1 0	0 0 1 1 1 1 1	6
0 1 1 1	1 1 1 0 0 0 0	7
1 0 0 0	1 1 1 1 1 1 1	8
1 0 0 1	1 1 1 0 0 1 1	9
1 0 1 0	X X X X X X X	
1 0 1 1	X X X X X X X	
1 1 0 0	X X X X X X X	
1 1 0 1	X X X X X X X	
1 1 1 0	X X X X X X X	
1 1 1 1	X X X X X X X	

$$a = w + xz + y\bar{x} + \bar{x}\bar{z}$$
$$b = w + \bar{x} + \bar{y}\bar{z} + yz$$

[20%]

(ii) Straightforward PLA implementation



A ROM can also be used. When the number of variables is small, a ROM is generally more economical than a PLA. However, when the number of input variables is large, PLAs often provide a more economical solution than ROMs.

[20%]

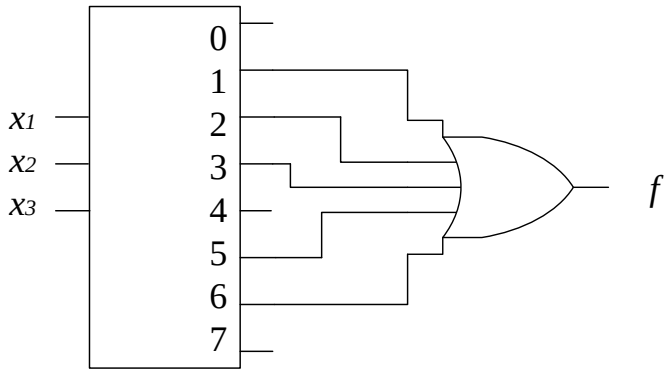
(iii) 0, 8, 6, 9, 2, 2, 2, 1, 0

[10%]

4 (a) Multiplexers and LUTs are suitable for single-output functions. LUT inputs are select lines of cascaded multiplexers, and can produce any function of n-inputs (addresses). ROMs are better for multiple-output functions but they become expensive and less efficient for very high number of variables. PLAs are good for multiple-output functions with lots of variables. They are expensive unless the number of variable is too high for a ROM.

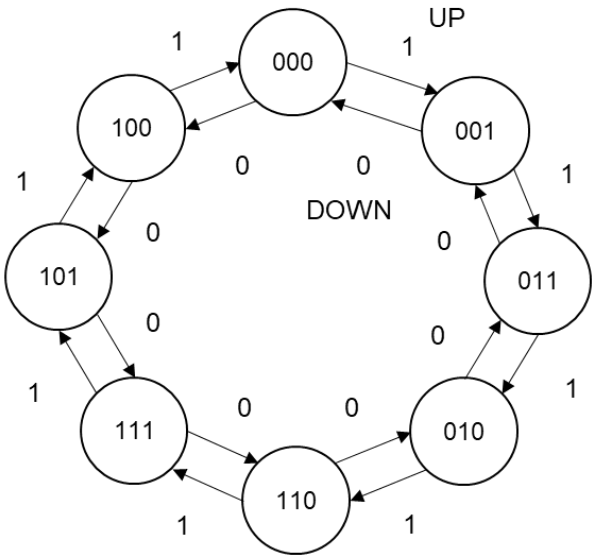
[20%]

(b) The function $f(x_1, x_2, x_3) = \sum(1, 2, 3, 5, 6)$ can be implemented using a 3-to-8 binary decoder and an OR gate.



[30%]

(c) (i)



Present State			Next State					
			DOWN ($Y = 0$)			UP ($Y = 1$)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

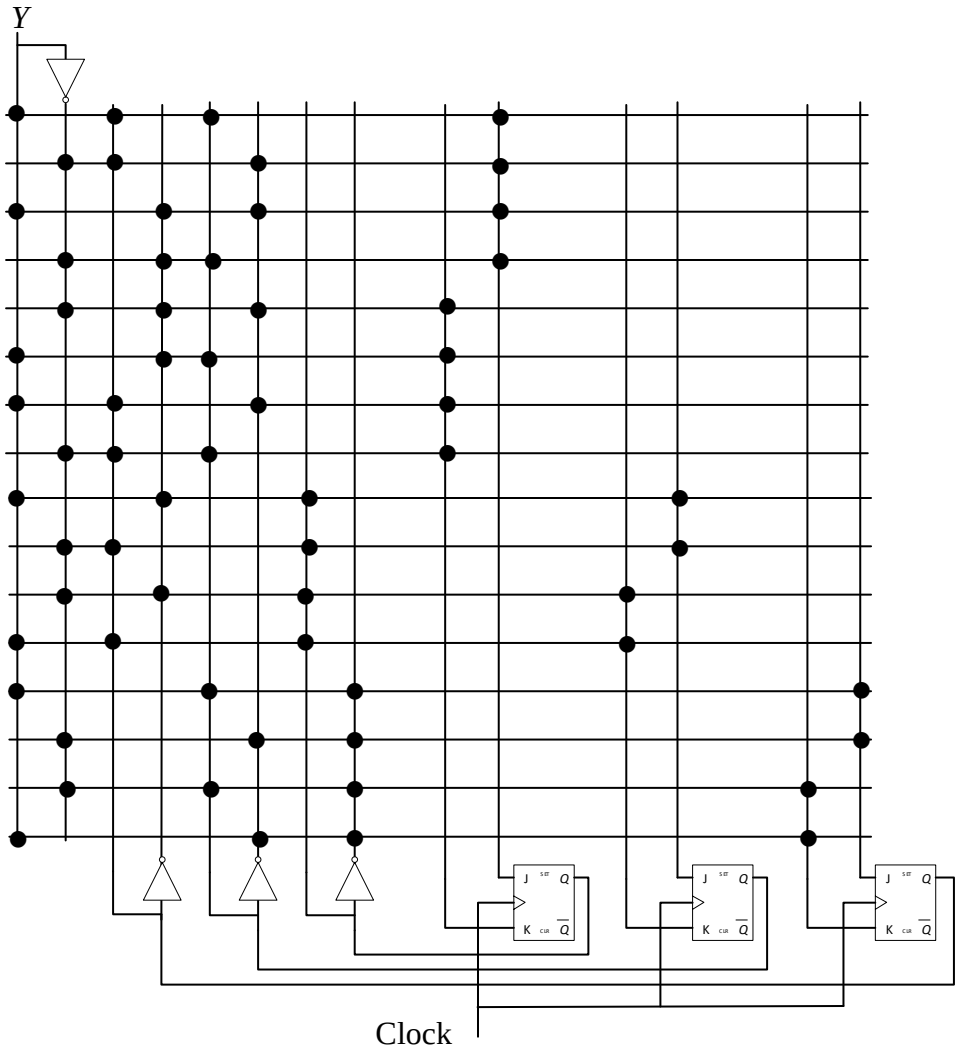
[20%]

(ii)

$J_0 = Q_2Q_1Y + Q_2\overline{Q_1}\overline{Y} + \overline{Q_2}\overline{Q_1}Y + \overline{Q_2}Q_1\overline{Y}$ $\quad K_0 = \overline{Q_2}\overline{Q_1}\overline{Y} + \overline{Q_2}Q_1Y + Q_2\overline{Q_1}Y + Q_2Q_1\overline{Y}$

$J_1 = \overline{Q_2}Q_0Y + Q_2Q_0\overline{Y}$ $\quad K_1 = \overline{Q_2}Q_0\overline{Y} + Q_2Q_0Y$

$J_2 = Q_1\overline{Q_0}Y + \overline{Q_1}Q_0\overline{Y}$ $\quad K_2 = Q_1\overline{Q_0}\overline{Y} + \overline{Q_1}Q_0Y$



[30%]