

3B3 Switch-mode Electronics crib 2015

Q1

a) (i) 20% Ripple. 2 kW, 325 V peak

i.e. $\pm 10\%$ Ripple. $\frac{2000}{325 \times 0.9} \Rightarrow 6.84 \text{ A}$

Linear decay over the full half cycle and constant load current (unlikely at 20%!).

$$\Delta V = \frac{I}{2fC} = \frac{6.84}{2 \times 50 \times C} = 65 \text{ V}$$

$$C = 1.05 \text{ mF}$$

[25%]

Conduction Angle:

Departure angle $C \frac{dV}{dt} = 6.84 \text{ A}$

$$CV\omega \cos \omega t = 1.05 \cdot 10^{-3} \times 325 \times 100\pi \cos \theta = 6.84$$

$$\theta = 86^\circ \text{ or } 94^\circ$$

Intersection angle $325 \times 0.9 - 325 \times 0.1 \frac{\theta}{\pi/2}, \omega t = \theta$

Meets $325 \sin \theta$

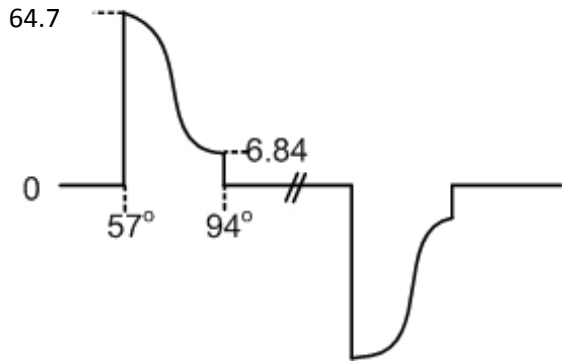
$$\sin \theta = 0.9 - 0.1 \frac{\theta}{\pi/2}$$

θ (rad)	$\sin \theta$	$0.9 - 0.2 \frac{\theta}{\pi}$	
1.1	0.89	0.83	
0.9	0.78	0.84	
1	0.84	0.84	$\theta = 57^\circ$

Conduction angle $33^\circ + 4^\circ = \underline{\underline{37^\circ}}$

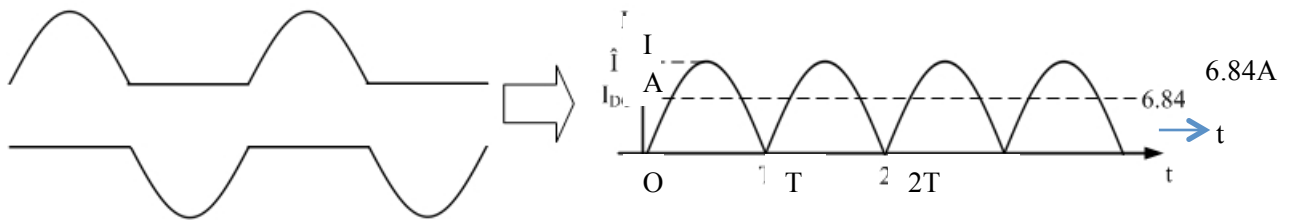
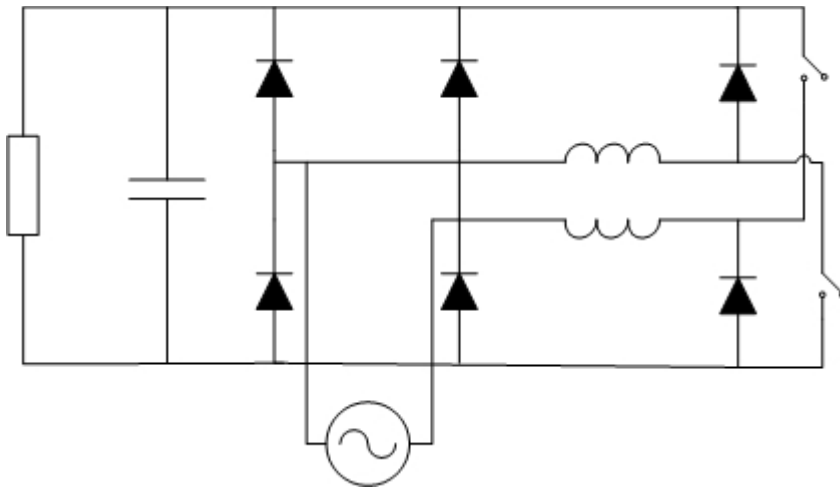
$$I = C \frac{dV}{dt} = CV\omega \cos 57^\circ = 57.9 \text{ A}$$

Total 64.7 A (peak diode current)



[35%]

b) A second design for the induction cooker uses two boost converter stages to draw sinusoidal current from the ac supply so ignore the ripple current at the high switching frequency:



Difference is in and out of the smoothing capacitor. Easily represented by the $n=1$ harmonic.

$$f(t) = \frac{2\hat{I}}{\pi} - \frac{4\hat{I}}{\pi} \cos \frac{\omega_o t}{3} + \dots \text{where } \omega_o = \frac{2\pi}{T}$$

$$325 - 10\% = 292$$

$$I_{DC} \frac{2000}{292} = 6.83 A$$

2nd harmonic? Yes because current is going in and out. Ripple is only given by 2nd harmonic

$$\text{Average} = \frac{2\hat{I}}{\pi} = 6.84 A \quad \omega = \frac{2\pi}{T}$$

$$T = \frac{1}{50 \times 2}$$

$$\omega_o = 4\pi f = 628$$

For the second harmonic $\frac{4\hat{I}}{\pi} \cos \omega_o t = 6.84 \times \frac{2}{3} \cos \omega_o t = 4.56 \cos \omega_o t$

Therefore the peak diode current is $6.84 + 4.56 = 11.4$ A

$4.56 \cos 628t$ is the capacitor current

$$\Delta V = \frac{1}{C} \int 4.56 \cos 628t \, dt$$

20% is *pk - pk* i.e. $2\Delta V \therefore \Delta V = 32.5$ V

$$C = \frac{1}{32.5} 4.56 \int_0^{t=\frac{\pi}{2}/\omega_o} \cos 628t \, dt$$

$$C = \frac{1}{32.5} \times 4.56 \times \frac{1}{628} = \underline{\underline{22mF}}$$

Check $\frac{11.4}{\sqrt{2}} \times 230 = 1.85 \text{ kW} < 10\% \text{ error.}$

$$= 0.6mF$$

[40%]

Q1 The section on a rectifier with capacitor smoothing was well answered. However, analysing the boost converter based power factor correction circuit proved challenging.

Q2.

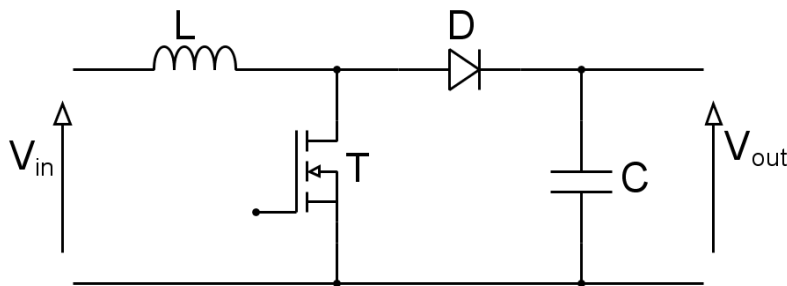
(a) Switch mode power conversion is efficient, so losses are low and so a high power density is possible. As the frequency increases, energy storage components become smaller, again facilitating high power densities. Circuits are available to provide DC to DC conversion, inversion and rectification, with galvanic isolation if needed.

[5%]

(b) (i) A flyback converter is the obvious choice as it is simple and cheap, only using one transistor, provides essential isolation for safety and permits a wide ratio of input to output voltage. [10%]

(ii) A half-bridge is a good solution as it can produce a suitable square wave output and yet only uses two devices. Isolation is not needed here. [10%]

(c) (i) The basic step-up converter is shown below:



The inductor is an energy storage component and energy is stored when the transistor is on as the inductor current grows. When the transistor is turned off, the inductor discharges via the diode into the output capacitor, and hence the load. The diode blocks reverse current flow when the transistor is on. [20%]

(ii) During inductor current build up (transistor on)

$$\Delta I = \frac{1}{L} \int_0^{\rho T} V_{IN} dt = \frac{1}{L} \rho T V_{IN}$$

During inductor current fall (transistor off)

$$-\Delta I \frac{1}{L} \int_{\rho T}^T (V_{IN} - V_{OUT}) dt = \frac{1}{L} (1 - \rho) T (V_{IN} - V_{OUT})$$

Equating

$$\frac{1}{L} \rho T V_{IN} = -\frac{1}{L} (1 - \rho) T (V_{IN} - V_{OUT})$$

Hence

$$V_{OUT} = V_{IN} \left(\frac{1}{1 - \rho} \right)$$

This analysis is based on continuous current in the inductor and assumes perfect components with negligible switching times. [20%]

(iii) Critical condition is that the current can build up enough to supply the load current.

Using power conservation (no losses) gives the current on the DC side to be 40 A. If the mean value of the current in the inductor is 40 A, the peak value is 80 A at the boundary of continuous conduction. This value is reached in 25 μ s. So

$$80 = \frac{1}{L} \rho T V_{DC}$$

$$\text{Or } L = \frac{25 \cdot 10^{-6} \cdot 50}{80} = 62.5 \mu\text{H} \quad [20\%]$$

(iv) The minimum breakdown voltages are both 400 V. [10%]

(v) Obviously simply setting the duty cycle to a particular value does not work in the discontinuous mode and even in the continuous mode the relationship derived in part (ii) will not quite apply because of non-idealities. The solution is to use a closed loop control circuit which senses the output voltage and adjusts the duty cycle to keep the output voltage constant. [5%]

Q2 The question led to good answers but some candidates did not have a sense of the key requirements for the two applications and some candidates did not realize that power transfer via the boost converter was from the 200 V battery to the 400 V DC link.

Q3

(a) (i) Devices with MOS gates are voltage controlled and need no current (apart from a very small leakage current) in the steady state. When switching, substantial currents may be needed to charge and discharge input capacitances, the faster the switching, the higher the current. [5%]

(ii) Methods include dedicated integrated circuits (e.g. IR2110), opto-isolators and pulse transformers. [10%]

(b) (i) The rise time is the sum of the time it takes for the gate to charge to voltage at which the load current commutates from the diode to the transistor and the time for the drain voltage to fall. The gate voltage at which the current commutates is given by

$$(V_{GS} - 2.8)^2 = 50/30$$

or

$$V_{GS} = 4.09 \text{ V}$$

The gate voltage is given by

$$V_{GS} = 5 \left(1 - e^{-t/RC} \right)$$

The time constant is

$$R_G C_{ISS} = 9.9 \text{ ns}$$

$$= 4.09 = 5 \left(1 - e^{-t/9.9 \cdot 10^{-9}} \right)$$

So the time to commutation is 16.87 ns.

The Miller plateau region is then entered and the current flowing through the gate resistor is balanced by that through the drain-gate capacitance.

$$\frac{5 - 4.09}{2.2} = 18 \cdot 10^{-12} \cdot \frac{28}{\Delta T}$$

The fall time is then

$$\Delta T = 1.22 \text{ ns} \quad \text{Total time is then } 18.09 \text{ ns}$$

In this circuit the dominant contribution to the switching time is the charging of the gate input capacitance to point at which commutation takes place. The relatively low DC link voltage leads to a rapid fall in drain-source voltage. [30%]

(c) (i) The part of the resistance representing the power transferred is 21.1 Ω and the power is given by

$$I^2 = \frac{3000}{21.1} \text{ so } I = 11.9 \text{ A}$$

With this current, the voltage across the resonant circuit at resonance is

$$V = 11.9 \cdot 22.8 = 271.9 \text{ V}$$

This relates to the fundamental component of the square wave output of V_{DC} peak to peak

$$271.9 \cdot \sqrt{2} = \frac{4}{\pi} V_{DC}$$

Therefore a minimum DC link voltage of 302 V is needed. [30%]

(ii) The resonant frequency is given by

$$f = \frac{1}{2\pi} \frac{1}{\sqrt{LC}} = \frac{1}{2\pi} \frac{1}{\sqrt{(380 \cdot 10^{-6}) \cdot (33 \cdot 10^{-9})}}$$

And the reactance of the 33 nF capacitor is 107.4 Ω at this frequency. Therefore the RMS voltage across the capacitor is

$$107.4 \cdot 11.9 = 1278 \text{ V}$$

The peak voltage is $1278\sqrt{2} = 1807 \text{ V}$

Therefore a rating of at least 1278 V (ac) or 1807 V (dc) is needed. The capacitor must be of a non-polar type, must have a low-loss dielectric (e.g polypropylene) and be capable of passing the large current. [10%]

(iii) If the inductance falls, the circuit will go off resonance, with the resonant frequency moving upwards, and the current will have a leading phase angle relative to the voltage. This is not good for the inverter which works better with a lagging current. A solution is to increase the inductance so that the load exhibits a lagging current across the inductance range but it becomes necessary to be able to vary the fundamental voltage applied to the circuit and increase the DC link voltage to accommodate this. The fundamental component of the output voltage can be varied by moving to a three-state waveform - $+V_{DC}$, $-V_{DC}$ and zero. [10%]

Q3 The part on high-side driving was obviously unfamiliar.

Q4

(a) (i) At this power level (presuming operation off rectified mains) MOSFETs are possibly the obvious solution but it is within the capabilities of power integrated circuits. Bipolar transistors could also be used. A supersonic switching frequency should be used to avoid irritating acoustic output - 18 or 20 kHz would be suitable and switching losses will be modest at these frequencies. [10%]

(ii) IGBTs are the obvious choice. A switching frequency of around 10 kHz is acceptable as there will be considerable background noise masking the acoustic output and the switching losses will be acceptable. [10%]

(iv) This is a high power drive but IGBT modules are available at this power level. The switching frequency will be modest to limit losses – 5 kHz is a reasonable figure. [10%]

(b) (i) Consider the line voltage between midpoints 'a' and 'b'. If switches S1 and S6 and switches S4 and S3 are switched as diagonal pairs and the resulting difference between the midpoints (the line voltage) is examined it is seen to be a rectangular wave with peak values of $\pm V_{DC}$ irrespective of the polarity of the modulating signal. This is so-called bipolar switching.

Alternatively S1 and S4 can be switched whilst keeping either S3 or S6 on. Examination of the resulting line voltage shows it to be a rectangular wave of peak values 0 and V_{DC} (S6 on) or 0 and $-V_{DC}$ (S3 on). So, assuming the modulating waveform to be a sinewave, in the positive half-cycle the line voltage only has pulses between 0 and $+V_{DC}$ and in the negative only pulse between 0 and $-V_{DC}$. [15%]

(ii) Adopting the unipolar mode effectively doubles the switching frequency, reducing filtering requirements and currents in the load related to switching frequency harmonics. [5%]

(iii) In motor drives, irrespective of whether the machine is star or delta connected, there is no need for a neutral connection and indeed complications may arise if it connected related to common mode signals added to the modulating waveform. In contrast, in an interruptible power supply intended to supply single phase loads a neutral connection would have to be provided, most easily from the centre point of the DC link. [5%]

(c) (i)

State	'ON' switches	$\frac{V_a}{V_{dc}}$	$\frac{V_b}{V_{dc}}$	$\frac{V_c}{V_{dc}}$
V_1	S ₁ , S ₆ , S ₂	1	0	0
V_2	S ₁ , S ₃ , S ₂	1	1	0
V_3	S ₄ , S ₃ , S ₂	0	1	0
V_4	S ₄ , S ₃ , S ₅	0	1	1
V_5	S ₄ , S ₆ , S ₅	0	0	1
V_6	S ₁ , S ₆ , S ₅	1	0	1
V_7	S ₁ , S ₃ , S ₅	1	1	1
V_8	S ₄ , S ₆ , S ₂	0	0	0

[20%]

(ii) There are two zero states – all high side switches on or all low side switches on – giving zero voltages between all the mid-points. Alternating between the two non-zero states bounding one of the six sectors on the vector diagram representing SVM, for example states 1 and 2, and a zero state allows variation of the output voltage. The choice of zero state depends on the scheme adopted i.e. whether the direct-direct or direct inverse approach is chosen.

[10%]

(i) The maximum line voltage obtainable with sine wave modulating signals is the difference between the outputs of two half-bridges. The output from one bridge has an amplitude of $\frac{V_{DC}}{2}$ and hence an RMS value of $\frac{V_{DC}}{2\sqrt{2}}$. In the case of SVM, the difference

between two phases, i.e. the line voltage is $\frac{\sqrt{3}}{2\sqrt{2}} V_{DC}$. This can be obtained from the hexagon diagram representing SVM by finding the radius of the largest circle which will fit in the hexagon.

However, at the point when a line voltage is at its maximum positive value, the other two are not at their maximum negative values so the DC link voltage is not fully utilized. By judicious choice of modulating function the magnitude of the fundamental can be increased up to a maximum of V_{DC} , i.e. the radius of the circle enclosing the hexagon. This increase is a factor of $\frac{2}{\sqrt{3}} = 1.15$.

Achieving this requires the addition of a suitable common-mode (or zero sequence) signal to the sine wave modulating waveform. The common-mode signal does not appear in the line voltages as it is subtracted out. The increase in fundamental output is valuable; a similar gain

can be achieved with the addition of third harmonic (triplen) components in ordinary sine wave PWM but the implementation in SVM is much easier and standard practice. [15%]

Q4 The section on application was not well answered and there were few really good answers to the final part on comparing space vector and sine PWM.