CRIB 4B21

1 (a) With the aid of one of more circuit schematics, describe the operating principle of a current mirror. State one application of the current mirror in an amplifier circuit. [25%]

With a reference to Fig. 1, the current flowing through Q_1, which is diode connected and hence saturated, results in V_{GS} appearing across Q_2. Providing $V_0 \geq V_{GS} - V_t$, the same current would also flow through Q_2, if Q_2 is matched with Q_1 in terms of aspect ratio (W/L).

The integrated MOS current mirror finds applications as a current source where the value of the current source can be replicated in a circuit such as in a multi-stage amplifier.

(b) The circuit shown in Figure 1 is an integrated MOS current mirror. The transistors in the circuit have the following parameters: $(W/L)_{Q1} = 50\mu m/5\mu m$, $|V_{A2}| = |V_{A1}| = 200$ V, $V_t = 1$ V, and $\mu_n \cdot C_{ox} = 20\ \mu A \cdot V^{-2}$. Assuming that there are no channel length modulation effects,

(i) what is the value of V_{GS}? [10%]

$$I_{DQ2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Q1}(V_{GS} - V_t)^2$$

$$100\mu A = \frac{1}{2} * 20 * 10 * (V_{GS} - V_t)^2$$

$V_{GS} - V_t = \pm 1$, → $V_{GS} = 2V$ or $0V$ (0V is not acceptable)

(ii) what is the lowest possible value of V_o for the mirror to supply a constant current output? [10%]

To make a current source, Q_2 should be in saturation, $V_{DS} \geq 2 - 1 = 1$, $V_{Dmin} = 1V$.

(iii) show that, if $V_o = V_{GS}$, then $\frac{I_o}{I_{REF}} = \frac{(W/L)_{Q2}}{(W/L)_{Q1}}$ [15%]

With $V_o = V_{GS}$, then the V_{DS} of both Q_1 and Q_2 are the same, so we don't have any issues with channel length modulation effects, as this can change the current of Q_1 and Q_2. Also in any case, question says λ can be assumed as zero.

So $I_{DQ1} = I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Q1}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$ and

$I_{DQ1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Q2}(V_{GS} - V_t)^2(1 + \lambda V_{DS})$.

Ratio of the above yields $\frac{I_{REF}}{I_o} = \frac{(W/L)_{Q1}}{(W/L)_{Q2}}$ since

$V_{GS1} = V_{GS2}$ and $V_{DS1} = V_{DS2}$.

(iv) what is the output resistance of the current mirror at I_o = 100 μA?

[15%]

$r_o = |V_{AQ2}|/I_o = |200V|/100\mu A = 2M\Omega$

(c) If the output voltage increases by 20% from its value at I_o = 100 μA, what will be the corresponding change in output current? Discuss the physical implications of your result.

[25%]

$\Delta V_o = 20\%V_o$ @ I_o = 100 μA. We know that $\Delta V_o/\Delta I_o = r_o \rightarrow \Delta I_o = \Delta V_o/r_o$.
At I_o = 100 μA, we have V_o = 2V and ΔV_o = 0.4V
ΔI_o = 0.4V/2MΩ = 0.2μA. Thus $\Delta I_o/I_o$ = 0.2μA/100μA = 0.2%
An ideal current source should source a current regardless of the value of voltage across it. However because of the finite output resistance of the transistors in the current mirror considered, the value of current that is sourced becomes dependent on the voltage across it.

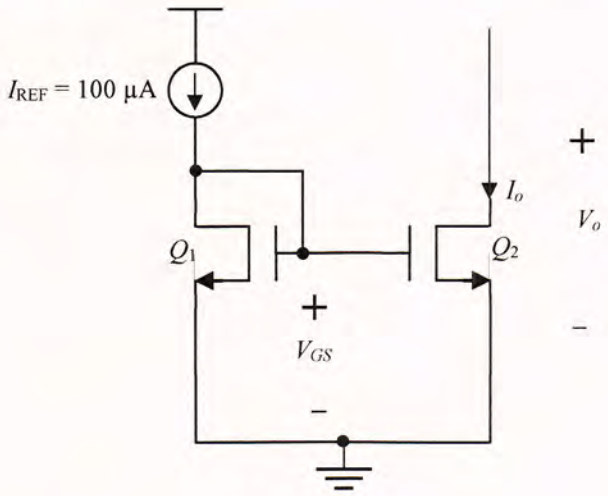


Fig. 1

2 (a) What is a multi-stage amplifier? [10%]

A multistage amplifier has several (single-stage) amplifiers connected in series; for example, the output of first stage becomes input of second stage and its output becomes input of the following stage and so on.

(b) Explain why multistage amplifiers are necessary from the standpoint of circuit characteristics. [10%]

A multistage amplifier has many desirable circuit characteristics that a single stage does not. For example, it provides higher input-output isolation, higher input impedance, lower output impedance, higher gain, and possibly also higher bandwidth.

(c) The two-stage CMOS op amp in Fig. 2 is fabricated in a 0.18 μm technology having $k_n' = 4k_p' = 400\ \mu A/V^2$, $V_{tn} = -V_{tp} = 0.4$ V. With A and B grounded, perform a DC design that will result in each of Q1, Q2, Q3 and Q4 conducting a drain current of 200 uA. Design so that all transistors operate at 0.2 V overdrive voltages.

(i) Specify the W/L ratio in tabular form required for each MOSFET. [15%]

Referring to Fig. 2

$I_{D8} = I_{D1-4} = I_{REF} = 200\ \mu A$

$I_{D5} = 2I_{D1} = 400\ \mu A$

No requirements are given for Q_6 and Q_7, so choose

* $I_{D6} = I_{D7} = 2I_{REF} = 400\ \mu A$

	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
$\left(\frac{W}{L}\right)$	25	25	100	100	50	200	50	25

$I_D = \frac{1}{2}k'(W/L)V_{OV}^2$ so,

$$\left(\frac{W}{L}\right)_{1,2,8} = \frac{2I_{REF}}{k_n'(V_{OV})^2} = \frac{2(200\ \mu A)}{400\ \mu A/V^2(0.2\ V)^2}$$

$= 25$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2I_{REF}}{k_p'(V_{OV})^2} = \frac{2(200\ \mu A)}{400\ \mu A/V^2(0.2\ V)^2}$$

$= 100$

$$\left(\frac{W}{L}\right)_{5,7} = \frac{2(2I_{REF})}{k_n'(V_{OV})^2} = \frac{2(400\ \mu A)}{400\ \mu A/V^2(0.2\ V)^2}$$

$= 50$

$$\left(\frac{W}{L}\right)_{C} = \frac{4I_{REF}}{k_p'(V_{OV})^2} = \frac{4(200\ \mu A)}{100\ \mu A/V^2(0.2\ V)^2}$$

$= 200$

(ii) What is the DC voltage at the output ideally? [15%]

Ideally, V_o (DC) = 0 V.

(iii) Calculate the input common mode range. [15%]

The lower limit is when Q_5 is leaving saturation,

$V_{D5} = -V_{SS} + |V_{OS}| = -1\ V + 0.2\ V = -0.8V$

$V_{in(min)} = V_{GS1} + V_{D5} = V_{tn} + V_{OV} + V_{D5}$

$= 0.4 + 0.2 - 0.8 = -0.2\ V$

The upper input limit is when Q_1 and $Q2$ leave the saturation region:

$V_{D1} = V_{OD} - V_{SD3} = 1 - (0.4 + 0.2) = 0.4\ V$

$V_{DS1} = |V_{OV}| = 0.2\ V$, so

$V_{in(max)} = V_{D1} - V_{OV} + V_{GS1}$

$= V_{D1} + V_{tn} = 0.4\ V = 0.8\ V$

so, the range of input voltage is (-0.2 V to +0.8 V)

(iv) Find the allowable range of the output voltage. [15%]

$V_{O_{(max)}} = V_{DD} - |V_{OV}| = 1 - 0.2 = +0.8\ \text{V}$

$V_{O_{(min)}} = -V_{SS} + |V_{OV}| = -1 + 0.2$

$= -0.8\ \text{V}$

so range is (–0.8 V to +0.8 V)

(d) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of 5V. [20%]

(d) $r_{O2} = r_{O4} = \dfrac{|V_A|}{I_{D2}} = \dfrac{5\ \text{V}}{0.2\ \text{mA}} = 25\ \text{k}\Omega$

$r_{O6} = r_{O7} = \dfrac{|V_A|}{I_{D6}} = \dfrac{5\ \text{V}}{0.4\ \text{mA}} = 12.5\ \text{k}\Omega$

$g_{m1} = g_{m2} = \dfrac{|I_D|}{V_{OV}/2} = \dfrac{0.2\ \text{mA}}{0.2\ \text{V}/2} = 2\ \text{mA/V}$

$g_{m6} = \dfrac{|I_{D6}|}{V_{OV}/2} = \dfrac{0.4\ \text{mA}}{0.2/2} = 4\ \text{mA/V}$

$A_1 = g_{m1}(r_{O2} \| r_{O4}) = (2\ \text{mA/V})(25\ \text{k} \| 25\ \text{k})$

$= 25\ \text{V/V}$

$A_2 = -g_{m2}(r_{O6} \| r_{O7}) = -4\ \text{mA/V}(12.5\ \text{k} \| 12.5\ \text{k})$

$= -25\ \text{V/V}$

$A_O = A_1 \cdot A_2 = 25(-25) = -625\ \text{V/V}$

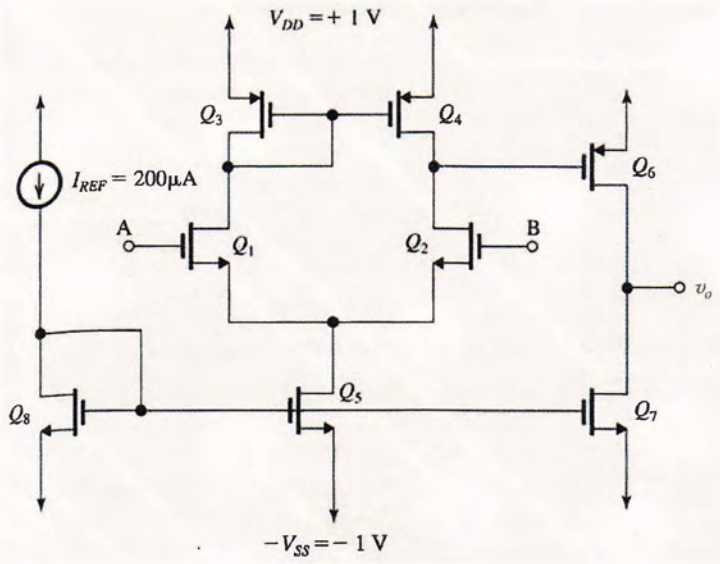


Fig. 2

3 (a) Name three sources of noise that are commonly found in integrated circuit components. [20%]

Given are five types of noise in integrated circuit components – any three would be acceptable.

-- Flicker (or $1/f$) noise – predominates at low frequency.

-- Thermal noise, shot noise – this noise is also referred to as "white" noise since it is present at all frequencies (flat spectrum)

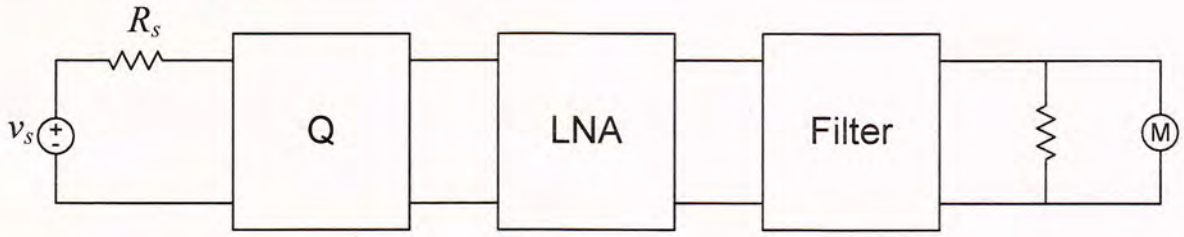
-- G-R noise – has a $1/f^2$ spectrum

-- Popcorn (or burst) noise – at low frequencies.

(b) What is meant by the noise figure of an amplifier and describe how you would measure it. [30%]

Noise Figure is a figure of merit characterizing how noisy an amplifier is wrt an ideal (noiseless) amplifier.

Measurement of Noise Figure



v_s = signal generator

R_s = source resistance

Q = active device (e.g. amplifier)

LNA = low noise amplifier

M = true rms voltameter

Filter to set bandwidth

1. Measure R_s and calculate $N_{vi} \equiv < v_n^2 >^{1/2}$ using $< v_n^2 >= 4kTBR_s$
2. Adjust signal voltage so that $v_s = 10 < v_n^2 >^{1/2}$ or $S_{vi} = 10N_{vi}$
3. Measure output voltage with M

Note: we have (with $v_s = 10 < v_n^2 >^{1/2}$) so $S_{vi}/N_{vi} = 20dB$

The larger the S_{vi}/N_{vi} is, the smaller the measurement error.

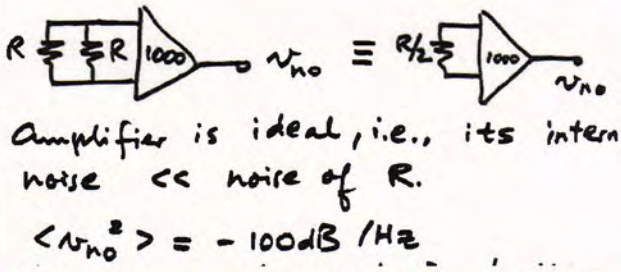
Thus we can neglect the noise and assume that voltmeter gives reading of signal output voltage, S_{vo}.

4. Set $v_s = 0$ and measure $N_{vo}$with M.
5. From the above measurements

$NF = 20 - 20log\frac{S_{vo}}{N_{vo}}$ (the 20 comes from $S_{vi} = 10N_{vi}$)

S_{vo}, N_{vo} are the meter readings from measurements 2 and 3.

(c) A parallel combination of identical resistors are connected between the input and ground terminals of a low noise amplifier. The output of the amplifier has a flat spectrum with value –100 dB/Hz. If the voltage gain of the amplifier is 1000, calculate the resistor value. In your calculations, assume that the amplifier is ideal (i.e., noiseless). [20%]



Amplifier is ideal, i.e., its internal noise << noise of R.

$\langle v_{no}^2 \rangle = -100$ dB/Hz

When referred to the amplifier input, this yields -160 dB/Hz, which is the thermal noise of (R/2). So $\langle v_{ni}^2 \rangle = 4kT(R/2) = 10^{-16} V^2/Hz$. Thus (R/2)=6 kΩ and R=12 kΩ.

(d) A filter or network has an equivalent noise bandwidth B, which can be stated as:

$$B = \frac{1}{|A_o|^2} \int_0^\infty |A(f)|^2 \, df$$

where A_o denotes the transmission (voltage or current) magnitude, $A(f)$ the transfer function, and f the frequency. The above equation yields the same results as the actual non-ideal bandwidth the filter or network has in practice.

For the single-pole filter shown in Fig. 3, show that the noise equivalent bandwidth is

$$B = \frac{\pi}{2} f_o$$

where f_o is the 3 dB bandwidth, $1/(2\pi RC)$. In calculating B, you can use the following relation:

$$B = a^2 \int_0^\infty (a^2 + b^2)^{-1} db = a \int_0^{\frac{\pi}{2}} dq$$

where q is a dummy variable.
[30%]

For the circuit shown in Fig. 3

$$A(f) = \frac{f_0}{f_0 + jf} \quad \text{where } f_0 = \frac{1}{2\pi RC}$$

$$B = \frac{1}{(A_0)^2} \int_0^\infty |A(f)|^2 df$$

$$A_0 = 1 \text{ and } |A(f)|^2 = \frac{f_0^2}{f_0^2 + f}$$

$$B = f_0^2 \int_0^\infty (f_0^2 + f^2)^{-1} df$$

$$B = f_0 \, \pi/2$$

Thus the equivalent noise bandwidth for the filter is $\pi/2$ times the 3-dB bandwidth.

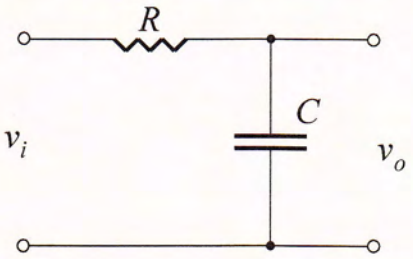


Fig. 3

4 (a) Explain how the design principle of the current steering circuit differs from that of a current mirror. [30%]

A current mirror circuit is particularly useful in integrated circuit design, where one resistor R is used to make multiple current sources. A current steering circuit enables realization of current sources that have different current values without the need to make additional current mirrors. The basis of design is as follows: If each transistor Q_n is identical to Q_{ref}, then each current I_{Dn} will equal reference current I_{ref}. But if the MOSFETS are not made identical, say in which $k_n \neq k_{ref}$ (say $k_1 = 2k_{ref}$), then the currents will be scaled accordingly (i.e. I_{D1} will be twice as large as I_{ref}).

(b) The current-steering circuit shown in Fig. 4 is fabricated in a CMOS technology for which $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 80\ \mu A/V^2$, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, and Early voltages $V_{An}' = 10$ V/μm, $|V_{Ap}'| = |12$ V/μm. If all devices have $L = 0.8$ μm, design the circuit so that $I_{REF} = 20\ \mu A$, $I_2 = 100\ \mu A$, $I_3 = I_4 = 20\ \mu A$ and $I_5 = 50\ \mu A$. Use minimum possible device widths needed to achieve proper operation of the current source Q_2 for voltages at its drain as high as +1.3V and proper operation of the current sink Q_5 with voltages at its drain as low as -1.3V.

(i) Specify the widths of all devices and the value of R. [40%]
(ii) Find the output resistance of the current source Q_2. [15%]
(iii) Find the output resistance of the current sink Q_5. [15%]

(i)

V_{OS2} & $V_{GS2} - V_{tp} \Rightarrow V_{DSmax} = V_{GS2} - V_t$

$(1.3 - 1.5) = V_{GS2} - (-0.6) \Rightarrow V_{GS2}$

$= -0.8\ V = V_{GS1}$

For Q_1:

$$I_{D1} = 20\ \mu A = \frac{1}{2} \times 80 \times \frac{W_L}{0.8} \times (-0.8 + 0.6)^2$$

$\Rightarrow W_1 = 10\ \mu m$

$I_2 = 100\ \mu A = 5I_{REF} \Rightarrow W_2 = 5W_1 = 50\ \mu m$

$I_3 = I_{REF} \Rightarrow W_3 = W_1 = 10\ \mu m$

$$I_3 = I_4 \Rightarrow \frac{W_3}{W_4} = \frac{\mu_n}{\mu_p} \Rightarrow W_4$$

$$= 10 \times \frac{80}{200} = 4\ \mu m$$

(i) contd

For Q_5: $V_{DS5} = V_{GS5} - V_{tn}$ For lowest V_O

$(-1.3 - (-1.5) = V_{GS5} - 0.6 \Rightarrow V_{GS5} = 0.8$ V

$$I_5 = 50\ \mu A = \frac{1}{2} \times 200 \times \frac{W_5}{0.8} \times (0.8 - 0.6)^2$$

$\Rightarrow W_5 = 10\ \mu m$

Now we calculate R:

$V_{GS2} = -0.8\ V \Rightarrow V_{G2} = 1.5 - 0.8 = 0.7$ V

$R = V_{G2} / I_{REF}$

$$R = \frac{0.7}{20\ \mu A} = 35\ k\Omega$$

$R = 35\ k\Omega$

(ii) $r_{o2} = V_{Ap}L/I_2 = 12x0.8/0.1 = 96\ k\Omega$.

(iii) $r_{o5} = V_{An}L/I_5 = 10x0.8/0.05 = 160\ k\Omega$.

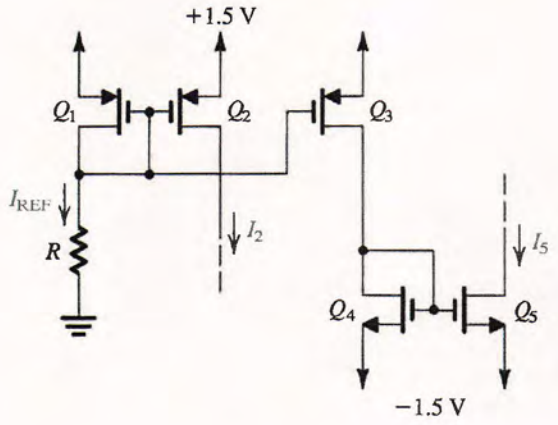


Fig. 4

5 Consider the circuit of Fig. 5, in which an NMOS transistor *M1* is connected in a circuit designed to provide a reference voltage V_{REF}.

(a) Derive an expression relating V_{REF} with the drain current I, transistor parameters and other circuit constants. [20%]

(b) For transistor *M1*, the channel dimensions W and L are chosen as 40 μm and 4 μm respectively; $V_t = +1$ V, and $k' = 20 \times 10^{-6}$ AV^{-2}. V_{DD} and V_{SS} are 6 V and 0 V respectively.

Deduce a suitable value for R if V_{REF} is to be 2 V, and determine the drain current I. [20%]

(c) What is meant by the following terms in the context of the performance of voltage references, and why are they important?

(i) Power supply sensitivity

(ii) Fractional temperature coefficient [20%]

(d) Write a short account of the approaches available to the CMOS IC designer for generating stable reference voltages for use in integrated circuit designs. Your account should mention power consumption, stability, area occupied, and any other factors you consider to be important. [40%]

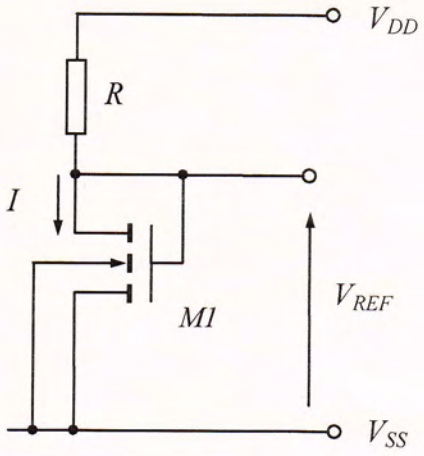
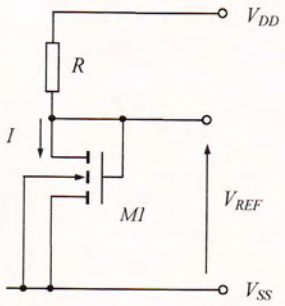


Fig. 5

5.



It can be seen that as G is shorted to D,
$V_{GS} \equiv V_{DS}$ and M1 is always in saturation.

Hence the second of the S-H equations applies.

From Kirchhoff, $V_{ref} = V_{DD} - IR$ (1)

From S-H $I = \frac{k'}{2}\frac{W_1}{L_1}\left(V_{ref} - V_t\right)^2$ (2)

Rearrange (2) $V_{ref} = V_{Tn} + \sqrt{\frac{I}{\frac{W_1}{L_1}\frac{k'}{2}}} = V_{DD} - IR$

Hence $V_{ref} = V_{Tn} + \sqrt{\frac{V_{DD} - V_{ref}}{\frac{RW_1}{L_1} \cdot \frac{k'}{2}}}$ [20%]

(b) Substituting the given values:

$$2 = 1+\sqrt{\frac{6-2}{\frac{R}{2}\cdot\frac{40}{4}\cdot 2\times 10^{-5}}} \text{ and}$$

$$\frac{6-2}{5R\cdot 2\times 10^{-5}} = (2-1)^2 = 1$$

Thus $R = \frac{4}{5\times 2\times 10^{-5}} = 40\ \text{k}\Omega$

and $I = \frac{6-2}{40\times 10^{3}} = 100\ \mu\text{A}$

Using a standard polySi of typically 50Ω/square, this resistor would require L/W of 800, and would occupy a great deal of space. [20%]

(c) An ideal voltage reference is independent of the power supply that services it. Practical references fall short of the ideal and 'PS sensitivity' expresses this in a quantitative way. It is defined:

$$S_X^{V_{REF}} = \frac{\partial V_{REF}}{V_{REF}} \Big/ \frac{\partial X}{X} = \frac{X}{V_{REF}} \times \frac{\partial V_{REF}}{\partial X}$$

where V_{REF} is the voltage reference, X is the parameter under consideration, V_{DD} in this case; if S is unity, a 10% change in V_{DD} will bring about a 10% change in V_{REF}. The objective is to produce a circuit design in which $S_X^{V_{REF}}$ is as small as possible for relevant parameters X, such as V_{DD}.

An ideal voltage reference will also be independent of ambient temperature. Since most electronic components and materials used in electronic circuits have temperature-dependent properties, which may be of different magnitudes and polarities, this is a non-trivial problem. To quantify the effects of components due to temperature change, we define 'fractional temperature coefficient TC_F, defined as follows for a component of value X:

$$TC_F = \frac{1}{X}\cdot\frac{\partial X}{\partial T} = \frac{1}{T}\cdot S_T^X$$

using the notation above. TC_F is typically expressed as parts per million per deg. C, or ppm/deg C. In circuits comprising several components that determine the output, all may contribute to the TC_F of the output itself, and the various contributing values of TC_F must be taken into consideration with the governing equation that determines the output. TC_F may be positive or negative depending on the materials of which the component is made and on its mode of

operation. This opens up the possibility of using devices in combination in circuits such that the temperature-dependent effects cancel to a significant extent.

Achieving minimum $S_{V_{DD}}^{V_{REF}}$ and TC_F simultaneously for a voltage reference is a challenge. [20%]

(d) Some of the techniques available are:

(i) use of a Zener diode where the reverse breakdown voltage characteristic is almost independent of current. Most Zener diodes have a significant temperature coefficient, but this can be minimised by use of devices in which the different physical effects (zener & avalanche effect) wholly or partially cancel. Zener diode may not be compatible with commodity CMOS processes and may have to be provided off-chip.

(ii) use a band-gap reference – an arrangement in which the V_F of a pair of forward biased diodes operated at different current densities are subtracted in an amplifier to give a result almost independent of temperature.

(iii) use an XFET where the difference in pinch-off voltage of two similar FETs is used to provide a stable reference.

Both (ii) and (iii) call for special processing that may not be compatible with commodity CMOS.

(iv) A reference along the lines originally proposed by Kwon et al (covered in lectures) uses only components available in a regular CMOS process. A thermal voltage is developed by use of a pair of MOSFETs operating sub-threshold. This has a positive temperature coefficient. A second voltage is developed from a self-biased β-multiplier circuit, again based on MOS transistors, which has output proportional to V_T: this has a –ve temperature coefficient. When these are scaled appropriately and summed in a suitable amplifier, the result has a near-zero tempco. [40%]

END OF PAPER

FORMULA SHEET

Bipolar Junction Transistors:

$i_C = \alpha i_E \qquad i_C = \beta i_B \qquad i_B = (1-\alpha) i_E \qquad i_E = (\beta+1) i_B$

$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad V_T = \frac{kT}{q} = 25\ mV\ at\ 300K$

$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E} \qquad r_o = \frac{V_A}{I_C}$

MOSFETs:

$i_D = K[2(v_{GS} - V_t)v_{DS} - {v_{DS}}^2] \qquad K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)$

$i_D = K(v_{GS} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad k' = \mu C_{ox}$

$g_m = 2K(v_{GS} - V_t) \qquad r_o = \frac{|V_A|}{I_D}$

Differential Amplifiers:

$v_o = A_d v_d + A_{cm} v_{cm}$

$CMRR = 20\log|A_d / A_{cm}| \qquad A_{cm} = \frac{v_o}{v_{cm}} \qquad A_d = \frac{v_o}{v_d} = g_m R_D$

OR OR

$A_{cm} = \frac{\Delta R_D}{2R} \qquad A_d = \frac{\Sigma R_C}{\Sigma R_E}$

BJT small signal operation: $i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2} \qquad i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$

$R_{id} = 2(\beta+1)(r_e + R_E) \qquad R_E = emitter\ resistance$

FET small signal operation: $i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$ $i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$

Millers Theorem: $C_{eq} = C_{bridge}(1-K)$ $K \equiv \frac{V_2}{V_1}$

Thermal Noise: $< v_n^{\ 2} >= 4kTBR$ $k = 1.38x10^{-23} J/K$

Feedback Architectures and Properties:

	Series-Shunt	**Series-Series**	**Shunt-Series**	**Shunt-Shunt**
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set[1]	V_o=0	I_o=0	I_o=0	V_o=0
To find output loop, set[1]	I_i=0	I_i=0	V_i=0	V_i=0
Signal Source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_v = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1+\beta A$	$1+\beta A_v$	$1+\beta G_M$	$1+\beta A_I$	$1+\beta R_M$
A_f	A_v/D	G_M/D	A_I/D	R_M/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{of}	$R_o/(1+\beta A_v)$	$R_o(1+\beta G_M)$	$R_o(1+\beta A_i)$	$R_o/(1+\beta R_M)$
$R'_{of} = R_{of} \lVert R_L$	R'_o/D	$R'_o(1+\beta G_M)/D$	$R'_o(1+\beta A_i)/D$	R'_o/D

[1]This procedure gives the basic amplifier circuit without feedback but taking the loading of β, R_L, and R_S into account.

4B21 Assessor's comments

Ql Analysis of Current Mirror Circuit

All students attempted this question and did very well. Almost everyone got the design correct taking into account the appropriate biasing conditions and transistor sizing. But many did not calculate the current stability against voltage variations and nor did they address the implications of the result.

Q2 Multistage CMOS Amplifier

All candidates attempted this question; a small number did very well and some had difficulties. The
main difficulty was in calculating the input common mode, which they confused with the allowable
range of the output voltage. There were some issues with the voltage gain calculations.

Q3 Noise in Integrated Circuits

Only four candidates attempted this question with two doing much better than the other. The difficulty for the low performers was evaluating the noise figure and the associated measurement technique. Some had issues with the thermal noise calculation from the amplifier's output noise spectrum.

Q4 Current Steering Circuits

A small number did very well and a small number had difficulties. While almost all students understood the operation of a current steering circuit, the main difficulties were in the calculation of transistor sizes. Virtually all students could calculate the output resistances of the sources and sinks.

Q5 Voltage Reference Circuit

Two candidates attempted this question and one did very well. While the question was straightforward, the difficulty, if any, was describing the approaches available to the CMOS IC designer in designing a stable voltage reference. Not all considered key factors such as power consumption and real estate.