Prof A Nathan

CRIB SHEET

ENGINEERING TRIPOS PART IIB

4B21

1 (a) With the aid of one of more circuit schematics, describe the operating principle of a current mirror and how one would scale the output current? [20%]

Fig. 1 is a common source amplifier in which a current mirror formed by Q2 and Q3 sources the bias current for the amplifying transistor Q_1. The current flowing through Q_3, which is diode connected and hence saturated, results in the same V_{GS} appearing across Q_2. Providing $V_0 \geq V_{GS} - V_t$, the same current would also flow through Q_2, if Q_2 is matched with Q_3 in terms of aspect ratio (W/L). This serves as the biasing current for Q_1. The output current is scaled by sizing the aspect ratio of Q_2.

(b) The circuit shown in Figure 1 is to be designed using a 0.18 μm process. The transistors have the following parameters: $\mu_n \cdot C_{ox}$ = 387 μA·V^{-2}, $\mu_p \cdot C_{ox}$ = 86 μA·V^{-2}, $V_{tn} = -V_{tp}$ = 0.5 V, V_{DD} = 1.8 V, V'_{An} = 5 V/μm, and V'_{Ap} = –6 V/μm. The output voltage is to swing between 0.2 V to 1.6 V and the voltage gain must be at least 10 V/V.

(i) Using the same channel length of transistors, design the circuit for a bias current of 50 μA. [20%]

For an output of 1.6 V,

$V_{SD_{2min}} = |V_{OV}| = 1.8 - 1.6 = 0.2$ V,

$V_{SD_{1min}} = 0.2$ V

Since $I_{D2} = I_{D3} = I_{D1} = 50$ μA,

and $I_D = \frac{1}{2}(\mu_p C_{ox})(W/L)V_{OV}^2$

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \frac{2I_{D2}}{(\mu_p C_{ox})(V_{OV})^2}$$

$$= \frac{2(50\ \mu A)}{(86\ \mu A/V^2)(0.2\ V)^2} = 29.1$$

For Q_1,

$$\left(\frac{W}{L}\right)_1 = \frac{2(50\ \mu A)}{(387\ \mu A/V^2)(0.2\ V)^2} = 6.46$$

A_V must be at least -10 V/V,

and $A_V = -g_{m1}(r_{O1} \| r_{O2})$

If we want to make r_{O1} and r_{O2} equal,

$A_V = -\frac{1}{2}g_{m1}r_O$

so, $r_O = \frac{A_V}{-1/2\ g_{m1}}$

$$g_{m1} \cdot \frac{I_{D1}}{V_{OV/2}} = \frac{50\ \mu A(2)}{0.2\ V} = 0.5\ mA/V$$

$$r_O = \frac{-10\ V/V}{-(1/2)\ (0.5\ mA/V)} = 40\ k\Omega$$

$r_O = \frac{|V'_A|L}{|I_D|}$ so,

for Q_1, $L_1 = \frac{40\ k\Omega(0.05\ mA)}{5\ V/\mu m} = 0.4\ \mu m$

for Q_2 and Q_3,

$L_2 = L_3 = \frac{40\ k\Omega(0.05\ \mu A)}{6V/\mu m} = 0.33\ \mu m$

(ii) If the channel length is an integer multiple of 0.18 μm, what is the needed channel length required? [15%]

If we want the channel lengths to be an integer multiple of 0.18 um, we choose

$L = 3(0.18\ \mu m) = 0.54\ \mu m$

(Note: Choosing 0.36 μm results in slightly less than -10 V/V.)

checking,

$$r_{O1} = \frac{\frac{V_An}{I_D}L}{} = \frac{5\text{V}/\mu\text{m}\ (0.54\ \mu\text{m})}{0.05\ \text{mA}} = 54\ \text{k}\Omega$$

$$r_{O2} = r_{O3} = \frac{6\text{V}/\mu\text{m}\ (0.54\ \mu\text{m})}{0.05\ \text{mA}}$$

$$= 64.8\ \text{k}\Omega$$

$$A_v = -g_{m1}(r_{O1} \parallel r_{O2})$$

$$= -0.5\ \text{mA/V}(54\ \text{K}1164.8\ \text{K})$$

$$= -14.7\ \text{V/V}$$

(iii) If the gain is required to be increased by a factor of 2, what is the required channel length? [20%]

If the gain is to be doubled, and the $\frac{W}{L}$ ratios kept the same, $r_{O1} \parallel r_{O2}$ must double.

If r_{O1} and r_{O2} had been equal, this would have meant doubling L and W, making the area 4 times greater.

For a gain of -20 V/V,

$L_1 = 0.8\ \mu m$

$L_2 = 0.67\ \mu m$

The closest integer multiple that satisfies our requirement is $(0.18\ \mu m)(5) = 0.9\ \mu m$.

so, with $L_1 = L_2 = L_3$,

$$r_{O1} = \frac{5\ \text{V}/\mu\text{m}\ (0.9\ \mu\text{m})}{0.05\ \text{mA}} = 90\ \text{k}\Omega$$

$$r_{O2} = \frac{6\ \text{V}/\mu\text{m}\ (0.9\ \mu\text{m})}{0.05\ \text{mA}} = 133\ \text{k}\Omega$$

This results in a gain of

$$A_v = -(0.5\ \text{mA/V})(90\ \text{k}\Omega \parallel 133\ \text{k}\Omega)$$

$$A_v = -26.8\ \text{V/V}$$

(iv) What is the total increase in total gate area? [15%]

Increase in area = $(0.9/0.54)^2 = 2.78$ (instead of 4)

(c) State one application of the current mirror in a multi-stage amplifier. [10%]

The integrated MOS current mirror finds applications as a current source where the value of the current source can be replicated in a circuit such as in a multi-stage amplifier.

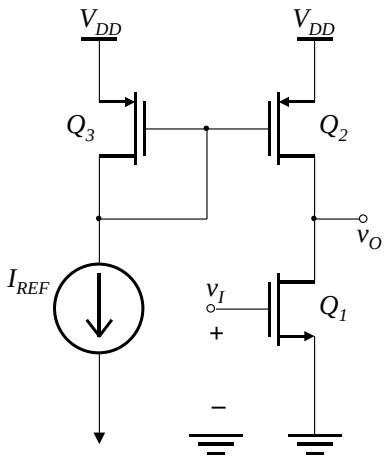


Fig. 1

Q1 Design of Current Mirror Circuit

12 attempts, Average mark 63%, Maximum 100%, Minimum 40%.

Most students attempted this question. A small number did very well and some had difficulties. Very few got the design correct taking into account the appropriate transistor sizing for the specified biasing conditions. Quite a number had problems calculating the needed channel lengths to achieve the required gain. However, most did address the implications of the overall result.

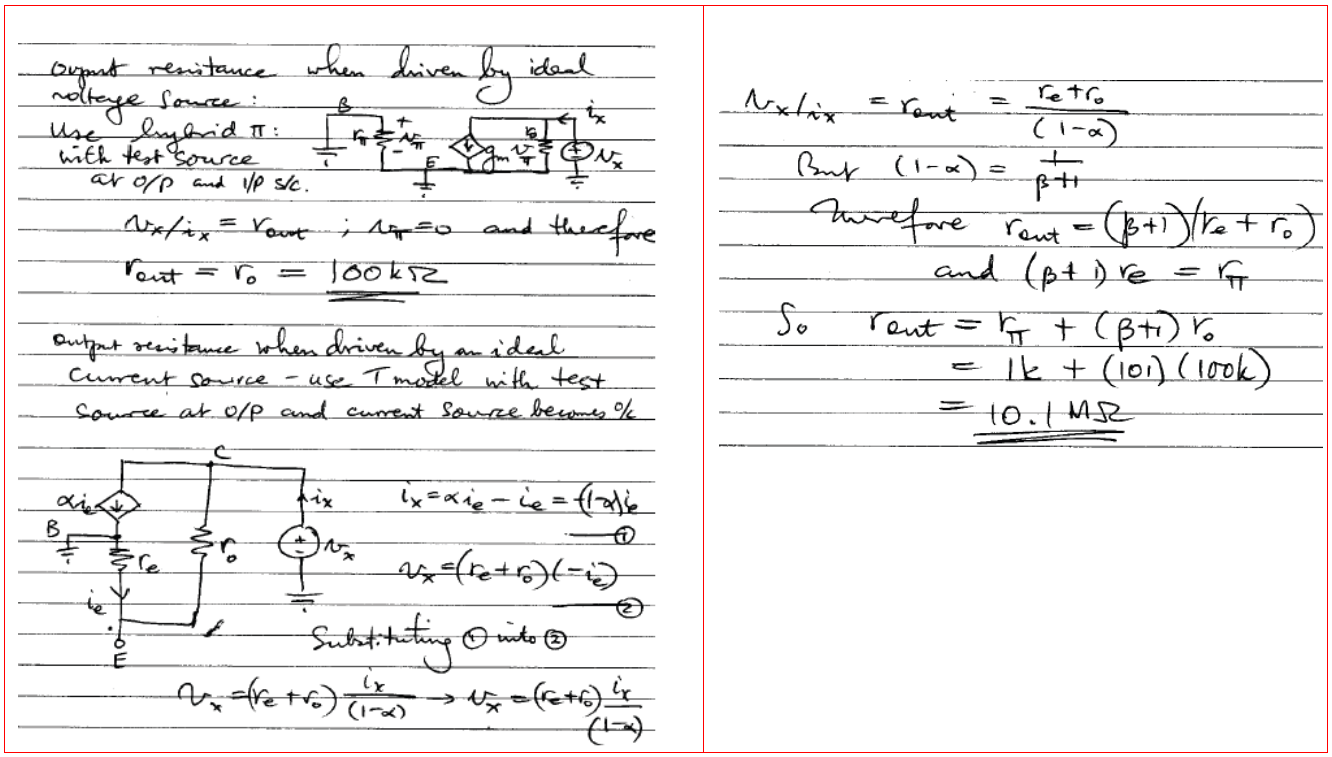
2 (a) Explain what is meant by an ideal voltage source and an ideal current source.

[25%]

Ideal voltage source is one where the voltage across it is independent of the current through it. Ideal current source is one where the current through it is independent of the voltage across it.

(b) Shown in Figure 3 are two common-base (CB) amplifiers, driven by (a) an ideal voltage source and (b) an ideal current source, respectively.

(i) Assuming that each circuit has been properly biased, and that the biasing networks, although not indicated in Fig. 3, do not affect the small-signal analysis, calculate the output resistance, r_{out} for circuits (a) and (b), using the following data: $r_\pi = 1\ k\Omega, r_o = 100\ k\Omega$, and $\beta = 100$. [50%]



Q2 Common Base Amplifiers Driven by Ideal Sources

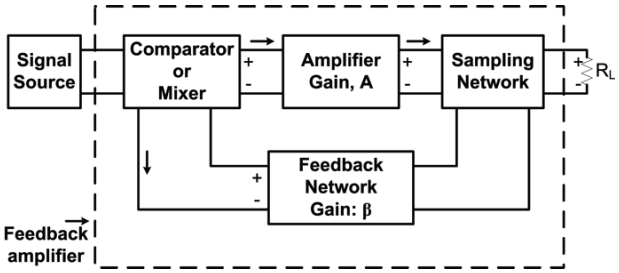
16 attempts, Average mark 83%, Maximum 100%, Minimum 25%.
All candidates attempted this question. Most of them did very well and a small number had difficulties, in which the main difficulty was in calculating the output resistances of the circuits. A few had problems with physical implications of the result and the practical applications.

(ii) Comment on the physical implications of the results for r_{out} for the two configurations. [25%]

The common-base amplifier, when driven by low source resistance, behaves as a voltage amplifier. On the other hand, with high source resistance, it behaves like a current follower. This transition takes place when the source resistance is at the vicinity of the emitter resistance, r_e.

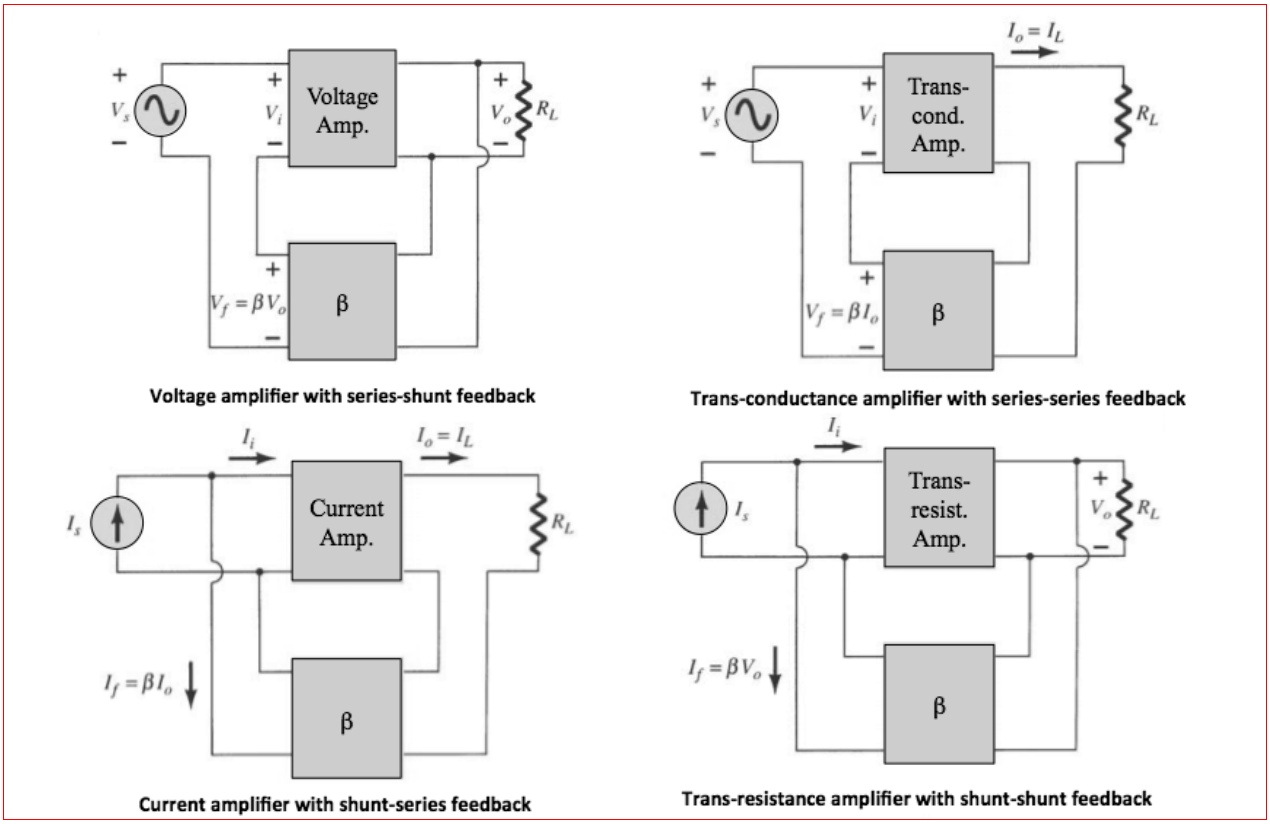
3 (a) With the aid of circuit block diagrams, define negative feedback as applied to electronic circuits describing its effect on circuit characteristics such as gain, linearity, input and output impedances, and bandwidth.
[25%]

Circuits such as amplifiers incorporate negative feedback. This reduces their gain, but improves linearity, input and output impedances, bandwidth and stabilizes all of these parameters, including the closed-loop gain. These parameters also become less dependent on the details of the amplifying device itself, and more dependent on the feedback components, which are less likely to vary with manufacturing tolerance, age and temperature. The difference between positive and negative feedback for AC signals is phase. If the signal is fed back out of phase, the feedback is negative and if it is in phase the feedback is positive.

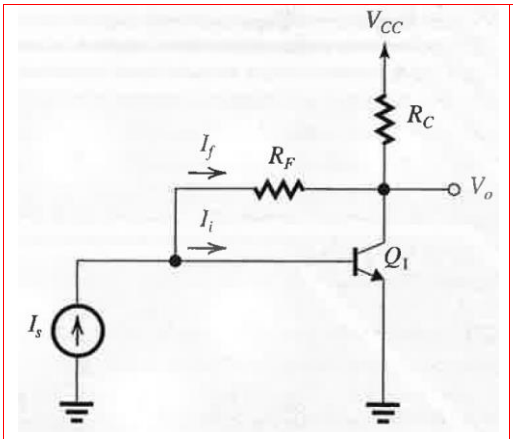


(b) What are the four negative feedback circuit topologies? State clearly if the nature of the sampled and mixing signals is a voltage or current as applied to the different amplifier topologies. [25%]

Series-Shunt (mixing signal is voltage, sampled signal is voltage)
Series-Series (mixing signal is voltage, sampled signal is current)
Shunt-Series (mixing signal is current, sampled signal is current)
Shunt-Shunt (mixing signal is current, sampled signal is voltage)



(c) For the feedback trans-resistance amplifier circuit shown in Fig. 3, assume $R_F >> R_C$ and $r_o >> R_C$ and that the feedback causes the signal voltage at the input node to be nearly zero. [50%]



To obtain A, remove the feedback resistor RF and consider the small-signal response of the resulting common-emitter amplifier.

$$V_O = -\beta I_i \cdot R_C \Rightarrow A = \frac{V_O}{I_i} = -\beta(R_C \parallel r_O)$$

if $r_O >> R_C \Rightarrow A \simeq -\beta R_C$

If the voltage at the input is near to cero volts

$$\Rightarrow I_f = -\frac{V_O}{R_F} \rightarrow \beta_F = \frac{I_C}{V_O} = \frac{-1}{R_F}$$

$$A_f = \frac{A}{1 + \beta_F A} = \frac{-\beta R_C}{1 + \frac{\beta R_C}{R_F}}$$

For $\beta = 100$, $R_C = 10$ K and $R_F = 100$ K

$$A_f = \frac{-100 \times 10\ \text{K}}{1 + (100 \times 10\ \text{K})/100\ \text{K}}$$

$$= -90.9 \times 10^3\ \text{V/A}$$

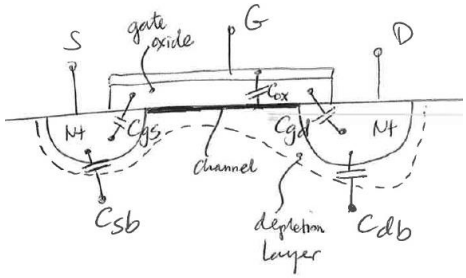
Q3 Feedback Circuit

15 attempts, Average mark 66%, Maximum 95%, Minimum 55%.

Almost all attempted this question. While most, if not all, had no problems with the concept of negative feedback, associated circuit topologies and effect on key performance attributes only very few could carry out systematic analysis to identify the nature of the feedback signal. The difficulty for the low performers was evaluating the feedback transfer functions and the gain.

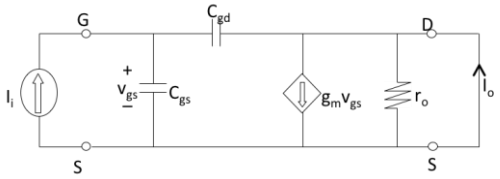
4 (a) Consider a MOSFET fabricated in one-micron CMOS technology. With the aid of a device schematic, describe the main sources of capacitances (along with typical values) that influence high frequency circuit performance. [25%]

Gate-to-channel capacitance: linear region, Cgs = Cdg = (1/2) WLCox; Cox ~ 1fF/μm2
Gate-to-channel capacitance: saturation region, Cgs = (2/3) WLCox = Cdg =0
Overlap capacitance (~1-10 fF): Cgs = Cdg = WL_D where L_D = overlap length
Source and drain junction capacitances C_{sb} and C_{db} (voltage-dependent) due to the depletion layer between S and D, and bulk (substrate)



(b) With the aid of a simplified equivalent circuit, show that the MOSFET's unity gain frequency (ω_T) can be approximated as $\omega_T = g_m /(C_{gs} + C_{gd})$, where g_m is the transconductance, and C_{gs}, C_{gd} the gate-source and gate-drain capacitances, respectively. [15%]

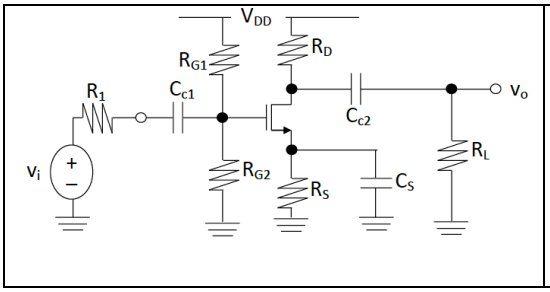
Equivalent circuit with the important C's. Here S is connected to the substrate (B) and C_{sb}, C_{db}, C_{gb} neglected to simplify analysis for unity gain frequency calculation

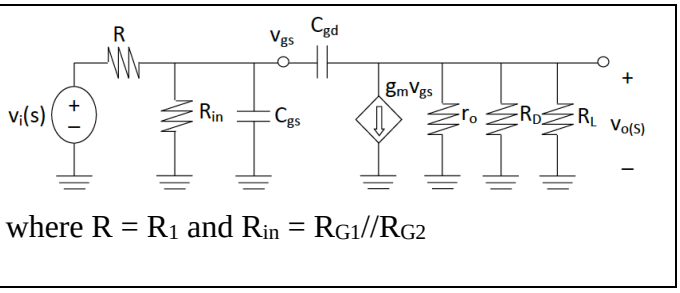


$i_o/i_{in} = g_m /[s(C_{gs} + C_{gd})]$ and current gain becomes unity when $\omega_T = g_m /[C_{gs} + C_{gd})$

(c) The components in the circuit shown in Fig. 4 have the following parameters: $\mu_n C_{ox}$ (W/L) = 2 mAV^{-2}, V_t = 0.5 V, $C_{gs} = C_{gd}$ = 10 fF, R_1 = 100 kΩ, R_{G1} = 600 kΩ, R_{G2} = 1.4 MΩ, R_D = 2 kΩ, R_L = 10 kΩ, R_S = 1 kΩ and $C_{C1} = C_{C2} = C_S = \infty$. The supply voltage V_{DD} = 1.8V and Early voltage V_A = -26V.

(i) Construct the small signal equivalent circuit. [15%]





where R = R_1 and R_{in} = R_{G1}//R_{G2}

(ii) Find the mid band voltage gain v_o/v_i. [15%]

$v_o/v_i = -g_m R_L' = -1.64$ V/V

where

$I_D = K(V_{GS}-V_T)^2$

where $V_{GS} = V_G - V_S$

$V_G = V_{DD} x R_{G2}/(R_{G1}+R_{G2}) = 1.8x1.4/2 = 1.26$ V

$V_S = R_S x I_D$

$K = 0.5x\ \mu_n C_{ox}\ (W/L) = 10^{-3}$ AV^{-2}

→ $I_D = (V_G - V_T - (I_D/K)^{0.5})/R_S$

→ $I_D \approx 0.26$ mA

→ $r_0 = |V_A| / I_D = 26V/0.26mA = 100$ kΩ

→ $V_{GS} = 1.26 - 0.26$ mA x1kΩ ≈ 1V

$g_m = \mu_n C_{ox}\ (W/L)\ (V_{GS}-V_t) = 2x10^{-3}\ (1-0.5) = 10^{-3}$ A/V

$R_L' = r_o//R_D//R_L \approx 100k\Omega//2k\Omega//10k\Omega \approx 1.64$ kΩ

(iii) What is the approximate upper -3dB frequency f_H ?

[20%]

For an approximate analysis, we use Miller's theorem. The total input capacitance is $C_T = C_{gs} + C_{gd}\ (1+g_m R_L') = 10fF+10fFx(1+1.64) = 3.64\ x10^{-14}$ F

$R' = R_1//R_{in} = 100k\Omega//[1.4M\Omega//0.6M\Omega] \approx 80.8$ kΩ

$f_H = (2\pi\ x3.64x10^{-14}\ x\ 80.8x10^3)^{-1} \approx 54$ MHz

(iv) In less than three lines, comment using intuitive-based reasoning, on the circuit's high frequency behaviour in relation to the source follower.

[10%]

In the common source amplifier, due to Miller effect (capacitive feedback), C_{in} is large – this degrades f_H. In the source follower, C_{in} is actually reduced!

Q4 High Frequency Analysis

4 attempts, Average mark 70%, Maximum 83%, Minimum 55%.

Only four candidates attempted this question with a reasonable spread of marks. While the candidates understood the small signal equivalent circuit and calculation of the unity gain frequency, the main difficulties were in estimating the 3-dB frequency. Virtually all of them had the right intuitive reasoning on the impact of parasitic capacitances on high frequency performance.

5 (a) Give a short account of the applications in which integrated *phase-lock loop architectures* are commonly used. [20%]

In a frequency synthesiser design for a computer motherboard, a current-starved Voltage-Controlled Oscillator (VCO) comprising seven identical stages is to be designed, based on the circuit in Figure 5, which shows a single stage (comprising transistors *M1*, *M2*, *M3* and *M4*), enclosed in dashed lines, and the current control circuit (*M5* and *M6*).

5 The use of a phase-locked loop allows synthesis of stable high frequencies given a high quality low-frequency reference. Any system that requires provision of a set of stable high frequency signals can benefit from the PLL technique. Examples of these applications include wireless base stations, wireless handsets, pagers, CATV systems, clock-recovery and clock-generation systems. Other applications of PLLs are found in tone decoding, coherent demodulation, bit synchronization, and symbol synchronization in computer communications. Phase-locked loops can also be used to demodulate frequency-modulated signals. A similar principle underpins the lock-in amplifier for recovery of small signals that otherwise would be lost in noise

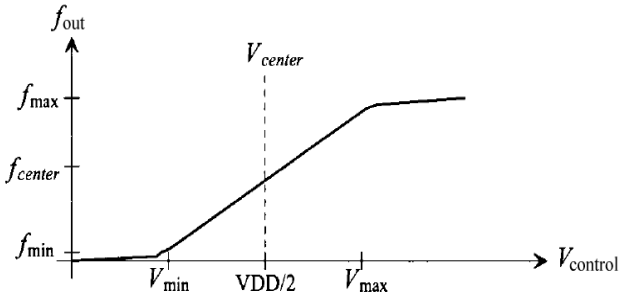
Certain of the elements of a PLL are readily implemented using circuit structures from digital technology. As a result, phase-locked loops integrate well into mixed-signal environments.

(b) Complete the schematic circuit for the VCO, and explain its mode of operation, giving details of what determines the frequency of operation. [20%]

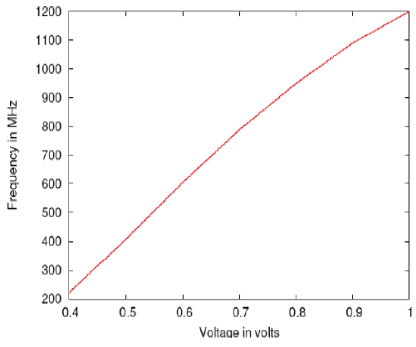
A VCO is a variable frequency oscillator whose frequency is controlled by a voltage according to the following equation:

$$f_{out} = F(V_{control})$$

Ideally, F is a linear function of $V_{control}$. An ideal and a typical characteristic are shown below.

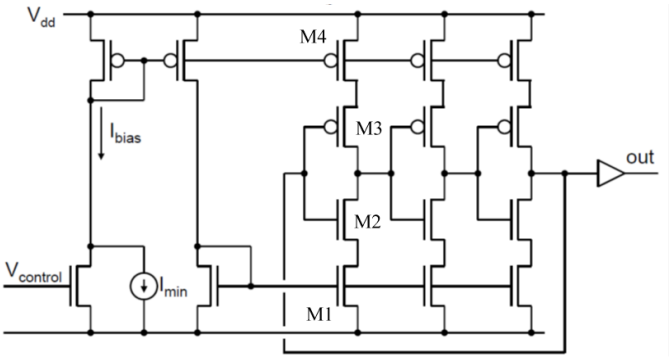


Ideal VCO characteristic

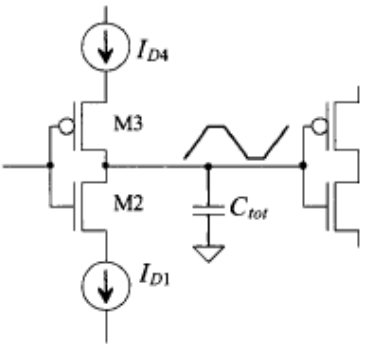


Typical law for $V_{control}$

A typical schematic for a three-stage current-starved VCO is shown below. Its operation is very similar to that of a ring oscillator.



Current-starved VCO



Simplified VCO stage

MOSFETs M2 and M3 act as an inverter, while MOSFETs M1 and M4 operate as current sources, limiting the current available to the inverter and therefore the speed with which parasitic capacitances arising at the output of the stage can be charged or discharged. These capacitances are due to the diode capacitances associated with the drains of M2 and M3, the gate capacitances of the succeeding stage, and any other linked interconnect or other parasitic capacitances. As with a ring oscillator, an odd number of stages is required, and each is identical to the one just described. A bias circuit regulated by *Vcontrol* feeds the current sources of each stage, so that all vary in synchronism.

An important property of the VCO is the need for a high input impedance, determined by the circuitry connected to $V_{control}$. This needs to be as high as possible to avoid adverse interaction with the loop filter that has to drive it.

(c) The total capacitance being driven at the output node of each stage is 2 fF. Assume the minimum value of the control voltage V_{inVCO} is equivalent to the threshold voltage for M5. The threshold voltage for all devices has magnitude 1 V. The supply voltage V_{DD} is 5 V, and the maximum drain current in each stage is to be 100 μA. Stating any other assumptions made,

(i) Estimate the maximum frequency that can be generated; [10%]

To determine design equations for use with the current-starved VCO we consider a simplified single stage (shown in Fig 4b) and estimate the total capacitance C_{tot} being driven at the drains of *M2* and *M3*.

$$C_{tot} = C_{out} + C_{in}.$$

The time take to charge C_{tot} from zero to V_{SP} with the constant current I_{D4} is given by:

$$t_1 = C_{tot}\frac{V_{SP}}{I_{D4}}$$

The time take to discharge C_{tot} from V_{DD} to V_{SP} is

$$t_2 = C_{tot}\frac{V_{DD}-V_{SP}}{I_{D1}}$$

If we set $I_{D1} = I_{D4} = I_D$, then the sum of t_1 and t_2 is just

$$t_1 + t_2 = C_{tot}\frac{V_{DD}}{I_D}$$

Assuming all stages are identical, the oscillation frequency f_{out} of the current-starved VCO for N (odd number > 3) is:

$$f_{out} = \frac{1}{N(t_1+t_2)} = \frac{I_D}{N.C_{tot}.V_{DD}}$$

The maximum VCO oscillation frequency corresponds to the largest value of I_D, which will be obtained when $V_{control} = V_{DD}$. It is possible to deduce the VCO gain, K_V, from these equations. The definition of K_V is:

$$K_V = 2\pi \cdot \frac{f_{max}-f_{min}}{V_{max}-V_{min}} \text{ radians/volt-second}$$

Numerical part: $C_{tot} = 2$ fF

$$f_{max} = \frac{I_D}{N.C_{tot}.V_{DD}} = \frac{100\times10^{-6}}{7\times5\times2\times10^{-15}} = 1.43 \times 10^9 \text{ Hz} = 1.43 \text{ GHz}$$

(ii) Develop an equation for the VCO gain, K_V, and estimate its value. Comment on the linearity that can be achieved. [20%]

$V_{inVCO} = 5$ V corresponds to the maximum value of I_{D1}, which we are told is 100 μA.
$V_{inVCO} = 1$ V corresponds to V_T for the bias control device, at which point I_D falls to zero, and f_{osc} also falls to zero.

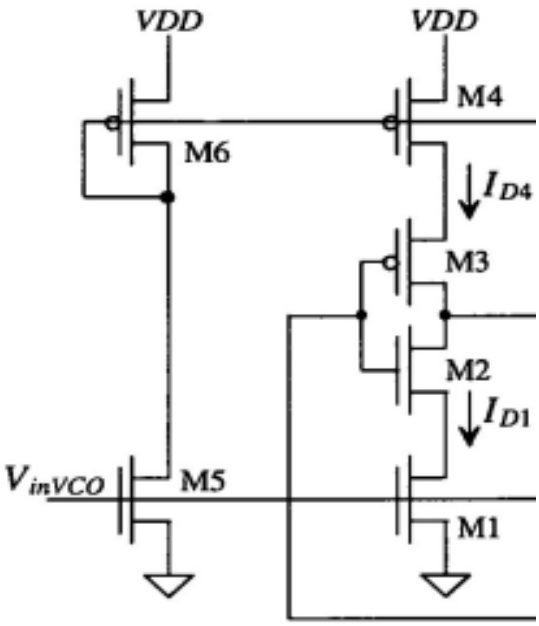
Formally, $K_V = 2\pi \cdot \frac{f_{max}-f_{min}}{V_{max}-V_{min}} = 2\pi \cdot \frac{1430-0}{5-1} = 2.25 \times 10^3$ rad / V-s

Note that the variation of frequency with control voltage is not expected to be a linear relationship.

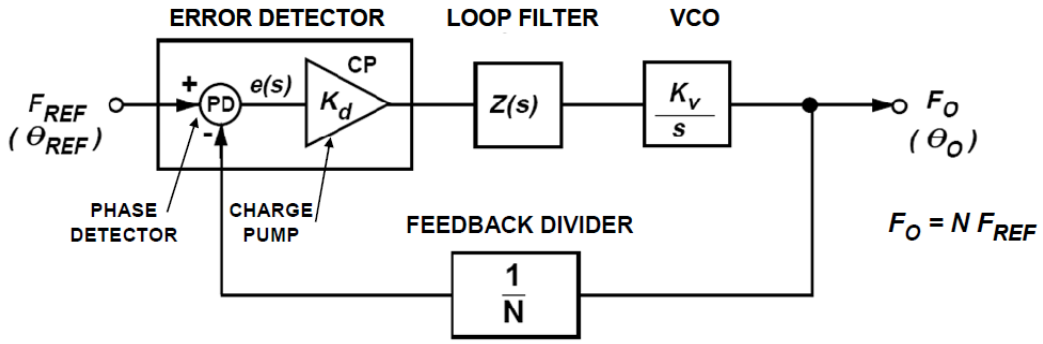
(i) As V_{inVCO} approaches V_T (i.e. small V_{inVCO}), the variation of I_D will become approximately proportional to $(V_{GS} – V_T)^2$ – the device is in saturation mode

(ii) Similarly, as V_{inVCO} approaches VDD, the device leaves saturation mode, and the current falls off slightly. In the mid-range region i.e. V_{inVCO} lying between 2V and 4V good linearity is obtained. In practice, the VCO parameters would be chosen for an appropriate centre frequency with V_{inVCO} set to the mid-point of this range.

(d) With the help of a block diagram, explain how the VCO developed in parts (b) and (c) could be used in combination with other suitably chosen circuit elements to achieve a frequency synthesiser whose output frequency is to be exactly 4 times the frequency of a stable reference. [30%]



(d) The main elements of a phase-locked loop are shown below.



PLL Model

It is a feedback system that combines:

(i) a *voltage controlled oscillator* (VCO) and
(ii) an error detector (comprises a *phase comparator* and a *charge pump*)
(iii)a low-pass *loop filter* (LPF)

so connected that the oscillator maintains a constant phase angle relative to a reference signal. The phase comparator may be based on an analogue multiplier, an XOR gate or a bistable. The loop filter is typically an off-chip RC circuit.

The phase-locked loop can be analysed quite generally as a negative-feedback system with a forward gain term and a feedback term. A simple block diagram of a voltage-based negative-feedback system is shown in Figure 2. Analysis can proceed in the normal way using Laplace Transform theory with a forward gain term, G(s), and a feedback term, H(s). The standard equations for a negative feedback system apply.

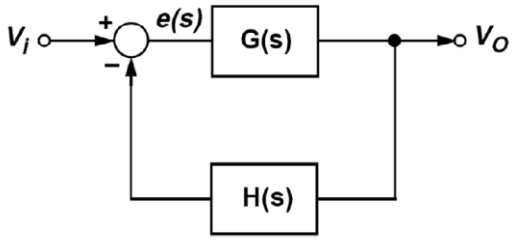


Figure 2 Standard negative-feedback control system model

In practice, phase-locked loops are intrinsically non-linear analogue systems, requiring a proper parametric analysis to cover the wide range of conditions that may arise when out-of-lock. A linear approach is satisfactory in normal operating conditions.

In a PLL-based system required to generate higher frequencies than the input, the VCO oscillates at a frequency of f_0. In a manner akin to that of a feedback network in other linear systems, a portion of this signal is fed back to the error detector, via a frequency divider with a pre-determined ratio 1/N. This divided-down frequency is fed to one input of the error detector. The other input in this example is a fixed reference signal, F_{REF}. The error detector compares the signals at both inputs. Negative feedback forces the error signal, *e(s)*, to approach zero, at which point the feedback divider output and the reference frequency are in phase and frequency lock. When the two signal inputs are equal in phase and frequency, the error will be constant and the loop is said to be in a "locked" condition.

The block diagram above shows a suitable architecture. In the architecture shown, $F_O = N \times F_{REF}$. Hence, if the feedback divider is specified as a 'divide-by-4' counter, the output frequency will be $4 \times F_{REF}$.

Q5 Voltage Controlled Oscillator

0 attempts, Average mark 0%, Maximum 0%, Minimum 0%.

No candidates attempted this question despite the question being reasonably straightforward, although it have many parts to it probably giving the impression that it was a very long question.

FORMULA SHEET

Bipolar Junction Transistors:

$i_C = \alpha i_E \qquad i_C = \beta i_B \qquad i_B = (1-\alpha) i_E \qquad i_E = (\beta+1) i_B$

$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad V_T = \frac{kT}{q} = 25\,mV \; at \; 300K$

$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{V_T}{I_B} \qquad r_e = \frac{V_T}{I_E} \qquad r_o = \frac{V_A}{I_C}$

MOSFETs:

$i_D = K[2(v_{GS} - V_t)v_{DS} - v_{DS}{}^2] \qquad K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)$

$i_D = K(v_{GS} - V_t)^2 = \frac{k'}{2}\left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \qquad k' = \mu C_{ox}$

$g_m = 2K(v_{GS} - V_t) \qquad r_o = \frac{|V_A|}{I_D}$

Differential Amplifiers:

$v_o = A_d v_d + A_{cm} v_{cm}$

$CMRR = 20\log|A_d / A_{cm}| \qquad A_{cm} = \frac{v_o}{v_{cm}} \qquad A_d = \frac{v_o}{v_d} = g_m R_D$

OR OR

$A_{cm} = \frac{\Delta R_D}{2R} \qquad A_d = \frac{\Sigma R_C}{\Sigma R_E}$

BJT small signal operation: $i_{C1} \approx \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2} \qquad i_{C2} \approx \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$

$R_{id} = 2(\beta+1)(r_e + R_E) \qquad R_E = emitter\ resistance$

FET small signal operation: $i_{D1} \approx \frac{I}{2} + \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2} \qquad i_{D2} \approx \frac{I}{2} - \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$

Millers Theorem: $C_{eq} = C_{bridge}(1-K) \qquad K \equiv \frac{V_2}{V_1}$

Thermal Noise: $< v_n{}^2 >= 4kTBR \qquad k = 1.38x10^{-23}\,J/K$

Feedback Architectures and Properties:

	Series-Shunt	**Series-Series**	**Shunt-Series**	**Shunt-Shunt**
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set[1]	$V_o=0$	$I_o=0$	$I_o=0$	$V_o=0$
To find output loop, set[1]	$I_i=0$	$I_i=0$	$V_i=0$	$V_i=0$
Signal Source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_v = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1+\beta A$	$1+\beta A_v$	$1+\beta G_M$	$1+\beta A_I$	$1+\beta R_M$
A_f	A_v/D	G_M/D	A_I/D	R_M/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{of}	$R_o/(1+\beta A_v)$	$R_o(1+\beta G_M)$	$R_o(1+\beta A_i)$	$R_o/(1+\beta R_M)$
$R'_{of} = R_{of} \lVert R_L$	R'_o/D	$R'_o(1+\beta G_M)/D$	$R'_o(1+\beta A_i)/D$	R'_o/D

[1]This procedure gives the basic amplifier circuit without feedback but taking the loading of β, R_L, and R_S into account.