Solutions for 4B21 - (Year 2019).

1) (a) Two advantages : (i) High gain

(ii) Avoids a dominant pole due to Miller multiplication at the input due to the common source amplifier stage seeing a low output impedance ($\sim 1/g_m$) i.e the input impedance of the common gate.

Two disadvantages : (i) High output impedance.

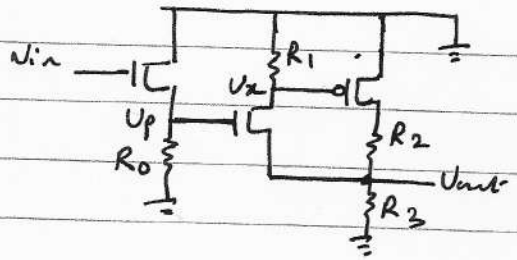
(ii) Requires a larger supply voltage (unless a folded cascode configuration is used) => high power consumption.

NOTE: Points regarding "cost" "complexity" are not considered correct.

Other Ado:- (i) High input impedance

Other disado:- (i) More noise (ii) Signal leakage via common gate. (iii) Layout area.

2.)



(i) At node U_p : $g_{mn}(V_{in} - U_p) = \frac{U_p}{R_0} \Rightarrow U_p = \frac{g_{mn} V_{in}}{g_{mn} + 1/R_0}$.

At node V_x : $\frac{-V_x}{R_1} = g_{mn}(U_p - V_{out})$

$= g_{mn}\left(\frac{g_{mn}}{g_{mn}+1/R_0} V_{in} - V_{out}\right)$.

At node V_{out} : $\underbrace{g_{mn}(U_p - V_{out})}_{= -V_x/R_1} - g_{mp} V_x = V_{out}/R_3$

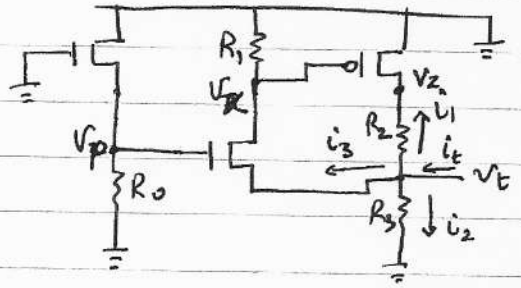
$\Rightarrow -V_x\left[\frac{1}{R_1} + g_{mp}\right] = \frac{V_{out}}{R_3}$

$\Rightarrow -g_{mn} R_1 \left[\frac{g_{mn}}{g_{mn}+1/R_0} V_{in} - V_{out}\right]\left[\frac{1}{R_1} + g_{mp}\right] = V_{out}/R_3$.

$\Rightarrow \frac{V_{out}}{V_{in}} = \left(\frac{g_{mn}}{g_{mn}+1/R_0}\right)\left(\frac{g_{mn} g_{mp} R_1 R_3 + g_{mn} R_3}{g_{mn} g_{mp} R_1 R_3 + g_{mn} R_3 + 1}\right)$.

NOTE: A common mistake observed was that students failed to account for $g_{mn}(V_x - V_{out})$ while writing KCL at node V_{out}.

(ii) Apply a test voltage V_t at the output node. Ground the input.



$$-g_{mn} V_p = \frac{V_p}{R_0} \Rightarrow V_p = 0.$$

$$i_2 = \frac{V_t}{R_3}$$

$$i_3 = +g_{mn} V_t = \frac{V_x}{R_1} \Rightarrow V_x = g_{mn} R_1 V_t.$$

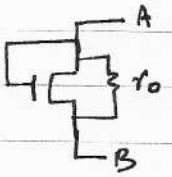
$$i_1 = \frac{V_t - V_2}{R_2} = +g_{mp} V_x = +g_{mp} g_{mn} R_1 V_t.$$

$$i_t = i_1 + i_2 + i_3$$

$$= V_t \left[+g_{mp} g_{mn} R_1 + g_{mn} + \frac{1}{R_3} \right]$$

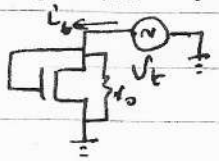
$$\Rightarrow \frac{V_t}{i_t} = R_{out} = \left(g_{mp} g_{mn} R_1 + g_{mn} + 1/R_3 \right)^{-1}.$$

(c.) (i)



Consider the diode connected TFT with channel length modulation resistor r_0. as shown in the figure. We define the two terminals A & B.

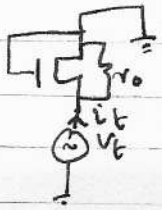
When a test voltage V_t is applied to A w.r.t B.



the current $i_t = g_m V_t + \frac{V_t}{r_0}$

$$\Rightarrow Z_m = (g_m + 1/r_0)^{-1}.$$

When a test voltage V_t is applied to B w.r.t A.



$$i_t = g_m V_t + V_t/r_0.$$

$$\Rightarrow Z_m = (g_m + 1/r_0)^{-1}.$$

$\therefore$ The device can be thought of as a resistor of resistance $(g_m + 1/r_0)^{-1}$.

NOTE: A common mistake observed was that students failed to apply ~~at~~ at calculate the impedance as seen from both terminals (drain and source). This is vital. The circuit can be modelled as a resistor only if these impedances are equal.

(ii), $I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{gs} - V_T)^2$.

$V_{gs} - V_T = 2V$

$I_{DS} = 1mA$.

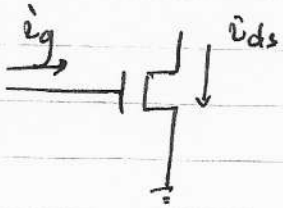
$\therefore \frac{\mu C_{ox}}{2} \frac{W}{L} = \frac{1e-3}{4} A/V^2$.

$g_m = \frac{\partial I_{DS}}{\partial V_{gs}} = \left(\frac{\mu C_{ox}}{2} \frac{W}{L}\right)\left(2(V_{gs} - V_T)\right) = \left(\mu C_{ox} \frac{W}{L}\right)(V_{gs} - V_T)$

$= \left(2 \times \frac{1e-3}{4}\right)(2) = 1e-3 \; A/V$.

2.) (a) (i) The transit frequency of the MOSFET is the small signal frequency which when applied to the gate (i.e the small signal is applied), the gate current equals the drain current. i.e the current gain is 1. Beyond this frequency, there is no current amplification in the transistor.

(ii)



$V_{ino} \sin(\omega t) = V_{gs}$

The gate capacitance $= C_{ox} W L$

Current through the gate = displacement current $= (C_{ox} WL) \frac{dV_{gs}}{dt}$

$i_g = (C_{ox} WL)(V_{ino} \omega) \cos(\omega t)$.

$|i_g| = C_{ox} WL V_{ino} \omega$

$i_{ds} = g_m v_{gs} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) v_{gs}$ (DC Bias)

$= \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{ino} \sin(\omega t)$.

$|i_{ds}| = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{ino}$.

$|i_g| = |i_{ds}|$ at $\omega = \omega_T =$ Transit frequency (angular)

$= 2\pi f_T$, with $f_T =$ Transit frequency.

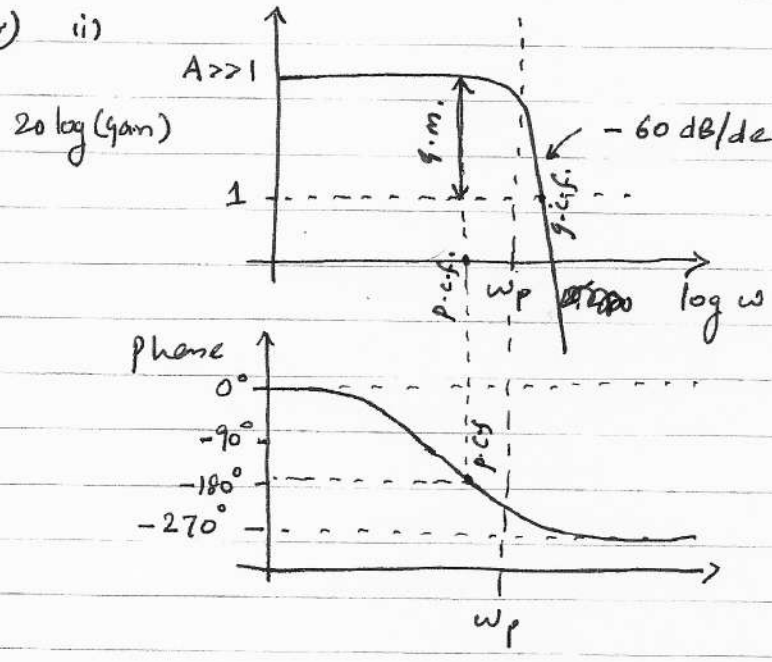
i.e $C_{ox} W L \, v_{in0} (2\pi f_T) = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) v_{in0}$.

$$f_T = \frac{1}{2\pi} \frac{\mu}{L^2} (V_{GS} - V_T)$$

If W is doubled and L halved, f_T increase 4 times.

$\therefore \alpha = 4$.

(b) ii)



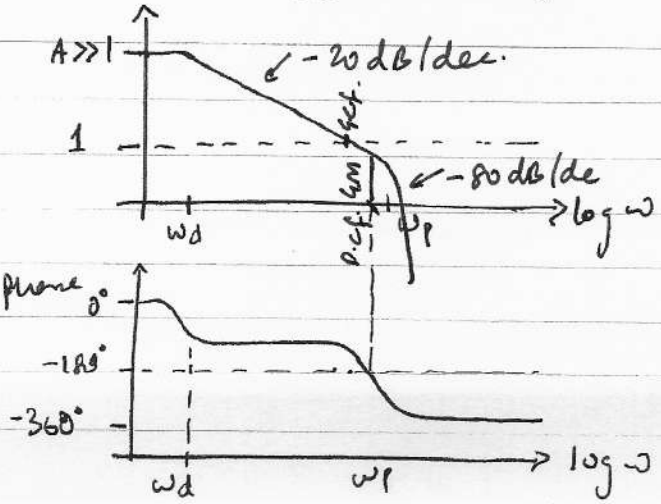
(ii) gain > 1 at Phase = -180°

$\therefore$ System in feedback is unstable. (i.e Closed loop).

(iii) Dominant pole compensation, makes the system tend to a first order system by adding a significant pole, ω_d

$\omega_d << \omega_p$.

$$T(s) = \frac{1}{\left(1 + \frac{s}{\omega_d}\right)\left(1 + s/\omega_p\right)^3}.$$

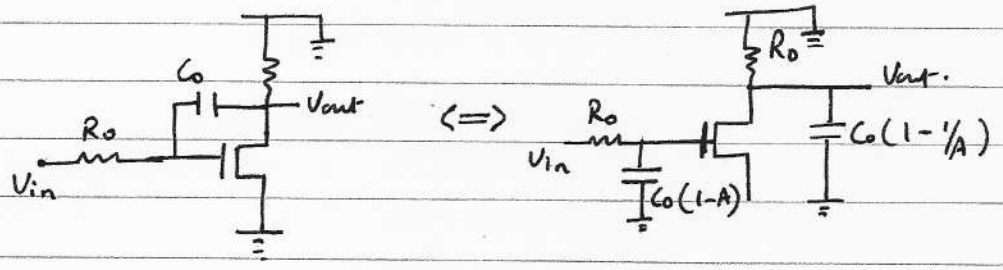


gain < 1 when phase = -180°.

$\therefore$ Closed loop system is stable.

NOTE: Many students labelled their Bode Plots incorrectly.

(c) (i) The Miller Equivalent Circuit is



D.C Gain, $A = -g_m R_o$.

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_o}{\left[1 + sC_o R_o (1+g_m R_o)\right]\left[1 + sR_o C_o \left(1+\frac{1}{g_m R_o}\right)\right]}$$

It is alright to approximate

$sC_o R_o (1+g_m R_o) \simeq sC_o g_m R_o^2$

and $sC_o R_o \left(1 + \frac{1}{g_m R_o}\right) \simeq sC_o R_o C_o / g_m$.

Under the assumption that the low frequency gain $A >> 1$.

(ii) Input time constant $= R_o C_o (1+g_m R_o)$

output time constant $= R_o C_o \left(1 + \frac{1}{g_m R_o}\right)$

$$R_o C_o (1+g_m R_o) = 10\, R_o C_o \left(1 + \frac{1}{g_m R_o}\right)$$

$$\Rightarrow (g_m R_o)^2 - 9(g_m R_o) - 10 = 0$$

$$\Rightarrow g_m R_o = 10.$$

$\therefore$ low frequency gain or the gain without $C_o = -g_m R_o$

$= -10$,

NOTE: If you have made the assumption of $g_m R_o >> 1$ and stated $R_o C_o (g_m R_o) = 10\, R_o C_o$ you will still obtain $g_m R_o = 10$

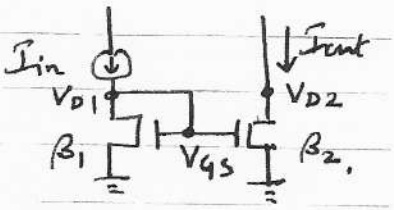
However if you have retained $R_o C_o (g_m R_o + 1)$ and approximated $R_o C_o \left(1 + \frac{1}{g_m R_o}\right) \simeq R_o C_o$ you will clearly not obtain the answer as 10. This is an illogical assumption.

3) (a) (i) An ideal two MOSFET current mirror (as shown in figure (a)) has both MOSFETs operating in saturation mode. Therefore, ideally the drain-source voltage of the MOSFETs do not affect the currents. We therefore have

$$I_{in} = \frac{\beta_1}{2}(V_{GS} - V_T)^2$$

$$I_{out} = \frac{\beta_2}{2}(V_{GS} - V_T)^2.$$

$$I_{out} = \frac{\beta_2}{\beta_1} I_{in}.$$



In the presence of channel length modulation, the drain-source voltage affects the current in the MOSFET via the channel length modulation parameter λ.

$$I_{in} = \frac{\beta_1}{2}(V_{GS} - V_T)^2(1 + \lambda V_{D1})$$

$$I_{out} = \frac{\beta_2}{2}(V_{GS} - V_T)^2(1 + \lambda V_{D2}).$$

$\therefore$ If $V_{D1} \neq V_{D2}$, $I_{out} \neq \frac{\beta_2}{\beta_1} I_{in}$.

(ii). CMOS technology provides the use of a PMOS & NMOS transistor.

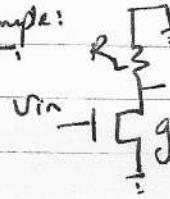
A PMOS acts as an ideal current source (in the absence of channel length modulation) and offers a high output impedance for a NMOS driver.

An NMOS performs a similar role for a PMOS driver.

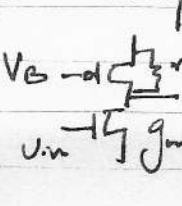
The advantage is that this (ideally infinite) high impedance load still has a finite voltage drop thereby permitting the driver to be in saturation.

$\therefore$ The use of CMOS offers very high gain.

Example:



Gain $= -g_{m1} R_L$



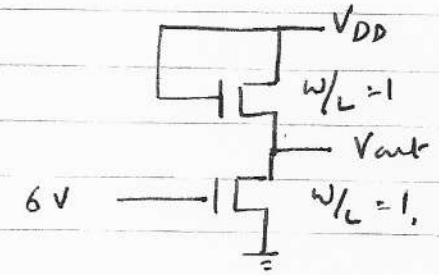
Gain $= -g_{m1} r_o$.

3.)(b) Clearly MOSFETS M1 to M7 are in saturation.
M2-M4 with M1-M3 are a cascode current mirror pair.
M5 - M6 are another current mirror pair.

∴ Current in M3-M4 = 4 mA.
Current in M5 = 4 mA
current in M6 = $(4\text{ mA})\left(\frac{6}{8}\right)$ = 3 mA.

Voltage drop across the resistor = 6 V.

We now consider the last stage of the circuit with MOSFETS M7 & M8.



(i) V_{DD} = 10 V

Assume M7 & M8 are in saturation.

$$\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_{M7}(V_{DD}-V_T-V_{out})^2 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_{M8}(6-V_T)^2.$$

$$\Rightarrow V_{DD}-V_T-V_{out} = 6-V_T$$

V_{DD} = 10 V, V_T = 1 V $\Rightarrow$

$$9 - V_{out} = 5 \Rightarrow V_{out} = 4\text{ V}.$$

Since $V_{out} - V_T < 6$ V, our assumption of M8 being in saturation is wrong. M8 is in linear mode. operation.

$$\therefore \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_{M7}(V_{DD}-V_T-V_{out})^2 = \mu C_{ox}\left(\frac{W}{L}\right)_{M8}\left[6-V_T-\frac{V_{out}}{2}\right] \times V_{out}$$

$$\therefore \frac{(9 - V_{out})^2}{2} = \left(5 - \frac{V_{out}}{2}\right) V_{out}.$$

$$\therefore 81 + V_{out}^2 - 18 V_{out} = 10 V_{out} - V_{out}^2.$$

$$\therefore 2 V_{out}^2 - 28 V_{out} + 81 = 0.$$

$$V_{out} = \frac{28 \pm \sqrt{28^2 - 4 \times 2 \times 81}}{4}$$

$$= 4.085 \text{ V} \quad (+ \text{ not valid}, - \text{ valid}).$$

(ii) If $V_{DD} = 15$ V.

Again assume M8 is in saturation.

$$\therefore \frac{\mu C_{ox}}{2} \left(\frac{W}{L}\right)_7 (V_{DD} - V_T - V_{out})^2 = \frac{\mu C_{ox}}{2} \left(\frac{W}{L}\right)_8 (6 - V_T)^2$$

$$\therefore V_{DD} - V_T - V_{out} = 6 - V_T$$

$$\therefore 14 - V_{out} = 5$$

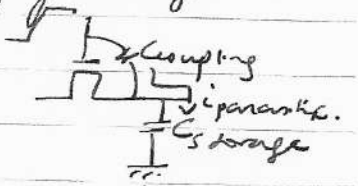
$$V_{out} = 9 \text{ V}$$

Our assumption of M8 being in saturation is alright

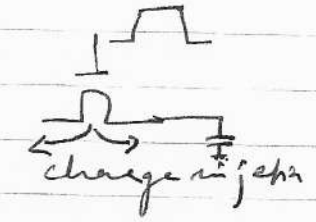
$$\therefore V_{out} = 9 \text{ V}.$$

4)(a)(i) Clock feed through is the error due to charge coupling between the gate - source/drain overlap capacitances. to the storage capacitor.

- It only dependens on the gate high and low levels
- It is independent of the rate of gate voltage variation



(ii) Charge injection is the error due to the channel charge that dissipates / appears by charge transfer from source / drain.

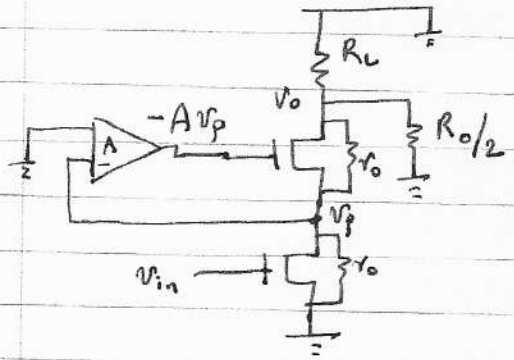


- It depends on the drain voltage (data stored on the capacitor.
- It is dependent on the frequency or ramp rate of the gate voltage.

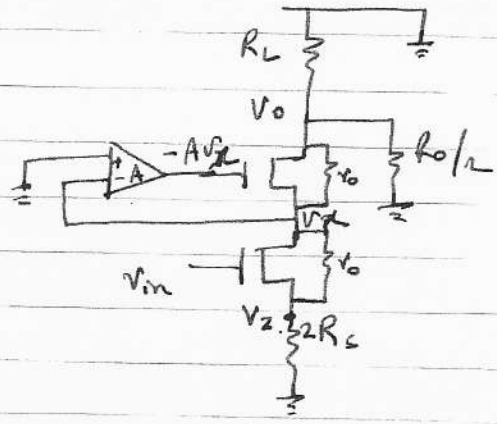
Very high ramp rate (greater than channel-capacitor ~~decrease~~ (R_C time constant)$^{-1}$), the channel charge is split equally between source/ drain.

low ramp rate ($\phi < R_C)^{-1}$), the channel charge distribute more charge to the lower impedance terminal. (larger capacitance).

(b) We use the half circuit method. due to the symmetry.



Differential gain calculation



Common mode gain calculat.

(i) Differential gain calculation.

$$-\frac{V_{od}}{R_L} = \frac{V_{od}}{R_o/2} + \frac{V_{od}-V_p}{r_o} + g_m(-AV_p - V_p) = \frac{V_p}{r_o} + g_m V_{in}.$$

$$\therefore \quad V_{od}\left[\frac{1}{R_L} + \frac{1}{R_o/2} + \frac{1}{r_o}\right] = g_m(A+1)V_p + \frac{V_p}{r_o}$$

$$\Rightarrow V_p = \frac{V_{od}\left[\frac{1}{R_L} + \frac{1}{R_o/2} + \frac{1}{r_o}\right]}{\frac{1}{r_o} + g_m(A+A1)}$$

Also $$-\frac{V_{od}}{R_L} = \frac{V_p}{r_o} + g_m V_{in}$$

$$-\frac{V_{od}}{R_L} = \frac{V_{od}}{r_o}\left[\frac{1/R_L + 1/R_o/2 + 1/r_o}{\frac{1}{r_o} + g_m(A+1)}\right] + g_m V_{in}.$$

$$\frac{V_{od}}{V_{in}} = -\left(1/R_L + \frac{1}{r_o}\left[\frac{1/R_L + 1/R_o/2 + 1/r_o}{\frac{1}{r_o} + g_m(A+1)}\right]\right)^{-1} g_m. = \text{Common mode gain.}$$

(ii) Common mode gain calculations:

$$-\frac{V_{oc}}{R_L} = \frac{V_{oc}}{R_o/2} + \frac{V_{oc}-V_x}{r_o} + g_m(-AV_2 - V_x) = \frac{V_x - V_2}{r_o} + g_m(V_{in}-V_2)$$

$$= \frac{V_2}{2R_s},$$

$$V_2 = -V_{oc}\frac{2R_s}{R_L}$$

$$\therefore \quad V_x = V_{oc}\frac{\left[1/R_L + 1/R_o/2 + 1/r_o\right]}{1/r_o + g_m(\blacksquare + A)}.$$

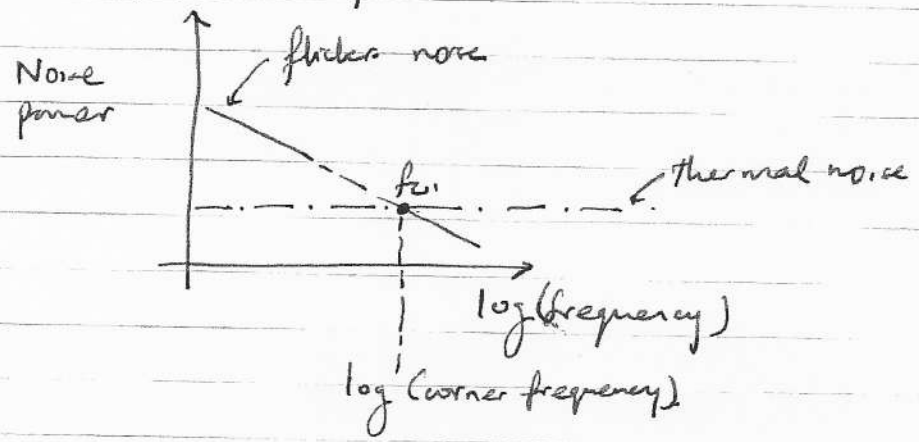
$$-\frac{V_{oc}}{R_L} = \frac{V_x}{r_o} + V_{oc}\frac{2R_s}{R_L r_o} + g_m V_{in} + g_m V_{oc}\frac{2R_s}{R_L}.$$

$$\Rightarrow \frac{V_{oc}}{V_{in}} = -\left(\frac{1}{R_L} + \frac{2R_s}{R_L r_o} + \frac{2R_s}{R_L} g_m + \frac{1}{r_o}\left[\frac{1/R_L + 1/R_{o/2} + 1/r_o}{\frac{1}{r_o} + g_m(1+A)}\right]\right)^{-1}$$

g_m

CMRR = $\frac{\text{Diff gain}}{\text{common Mode Gain.}}$

(c) (i) The corner frequency of a MOSFET is the frequency at which the flicker noise power equals the thermal noise power.



(ii) Thermal noise voltage = $4kT\left(\frac{2}{3} g_m^{-1}\right)$.

Flicker noise voltage = $\frac{\alpha}{C_{ox} W L f}$

At $f = f_c$.

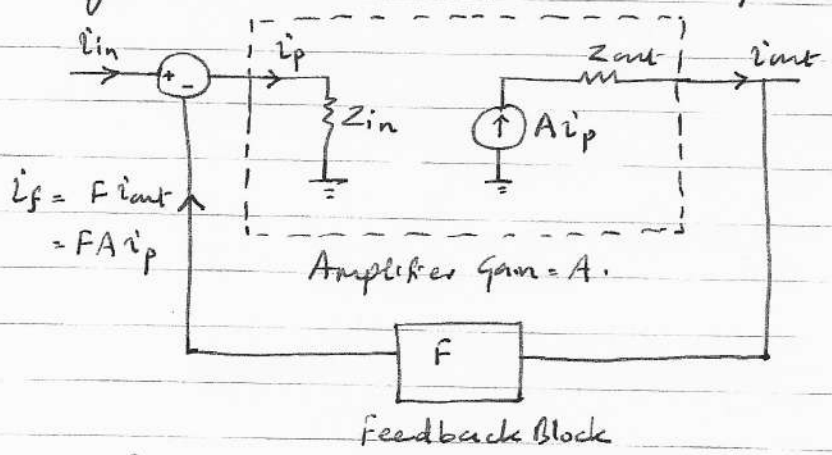
$$\frac{\alpha}{C_{ox} W L f_c} = 4kT\left(\frac{2}{3}\right)\left(\frac{1}{g_m}\right).$$

$$f_c = \frac{\alpha}{(C_{ox} WL)(4kT)\left(\frac{2}{3}\right)} \cdot \qquad g_m = \frac{\alpha\sqrt{2\mu C_{ox}\frac{W}{L} I_{dc}}}{(C_{ox} WL)(4kT)\left(\frac{2}{3}\right)}$$

$$= \frac{\alpha\sqrt{2\mu C_{ox} I_{dc}}}{C_{ox}\left(\frac{8}{3}kT\right)} \frac{1}{W^{1/2} L^{3/2}}, \Rightarrow \alpha = \frac{1}{2^{1/2} 2^{-3/2}} = 2.$$

with negative feedback.

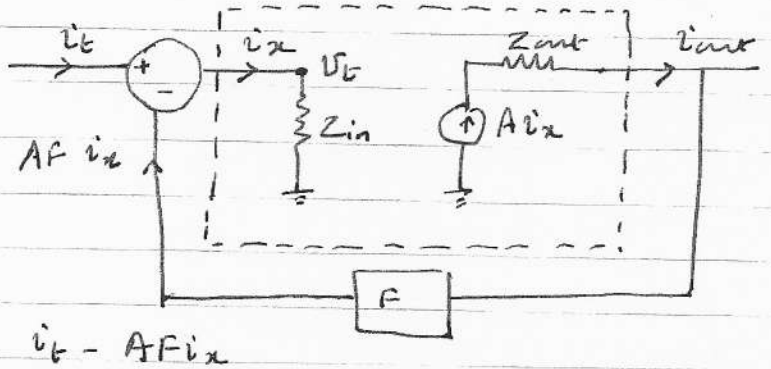
(3.) (c) The general current amplifier is represented as



$$\frac{i_{out}}{i_{in}} = \frac{A}{1+AF}$$

(i) Input impedance: Remove i_{in} and apply a test current i_t. Observe the voltage v_t developed.

$\frac{v_t}{i_t}$ = $Z_{in,feedback}$ = Effective input impedance with feedback



$i_x = i_t - AF i_x$

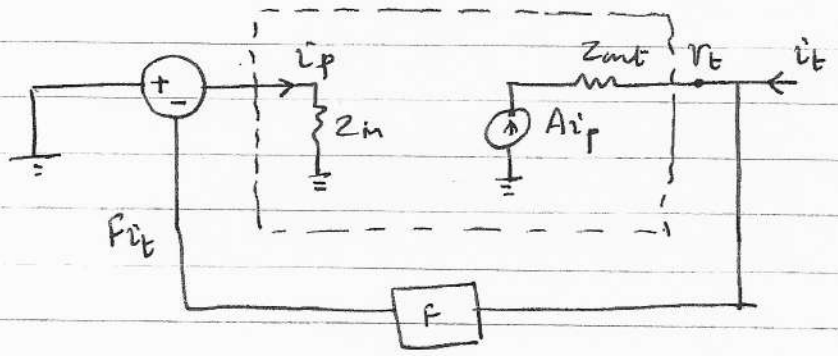
$\Rightarrow i_x = i_t / 1+AF$

$V_t = i_x Z_{in} = \frac{i_t Z_{in}}{1+AF} \Rightarrow \frac{v_t}{i_t} = Z_{in,feedback} = \frac{Z_{in}}{1+AF}$

i.e input impedance has effectively reduced by a factor of $1+AF$

(ii) Output impedance: Again remove the input & apply a test current at the output node and measure v_t.

$\frac{v_t}{i_t}$ = $Z_{out,feedback}$ = Effective output impedance with feedback.



$$i_p = -Fi_t$$

$$V_t = (i_t - Ai_p) Z_{out}$$
$$= (i_t + AFi_t) Z_{out}$$

$$\frac{V_t}{i_t} = Z_{out}(1+AF) = Z_{out,feedback}$$

$\therefore$ The effective output impedance increases.