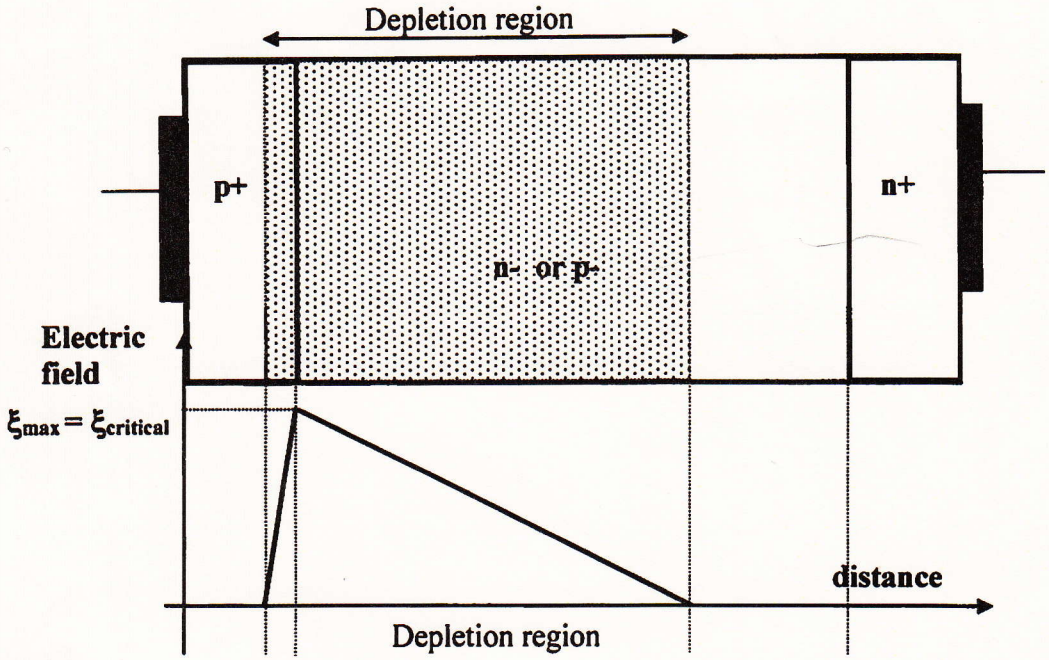
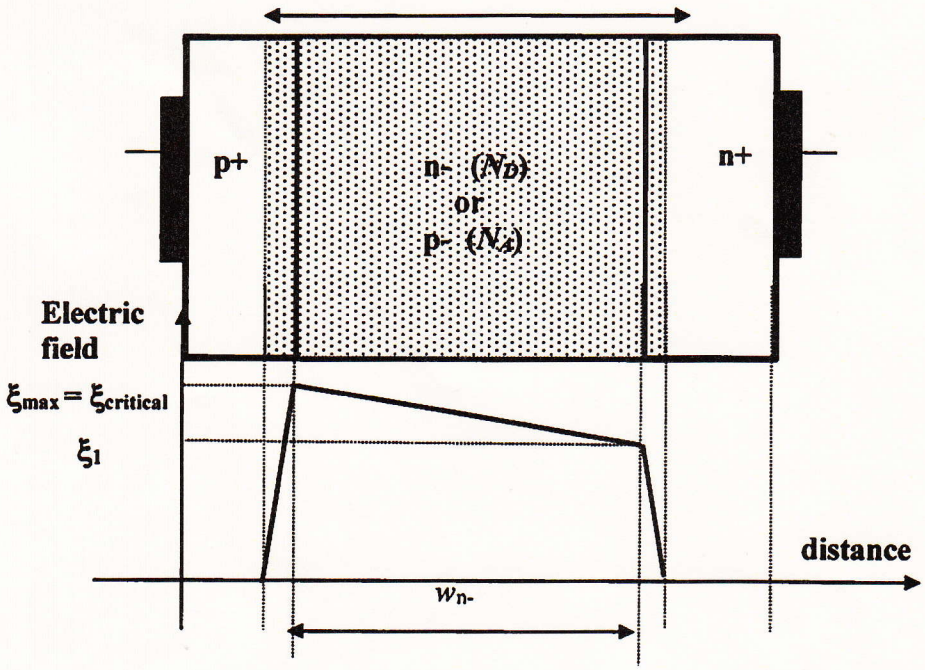
1. (a) The Non punch-through (NPT) high voltage diode is a based on a PIN diode where the thickness (width) of the lowly doped layer (n- or p-) is larger than the depletion region thickness (width) at breakdown. Thus the depletion region never reaches the n+ cathode region.



The Punch-through (PT) high voltage diode is a based on a PIN diode where the thickness (length) of the lowly doped layer (n- or p-) is smaller than the depletion region thickness (length) at breakdown. Thus the depletion region reaches the n+ cathode region before avalanche breakdown takes place.



For the BJT the PT design is more appropriate. The drift length is shorter in the PT design, and since the BJT operates in hard saturation, the charge in the drift region (collector) is much greater than the doping, so a PT design will ensure minimum drop across this region. [40%]

(b) $f = \frac{1}{T} = 10\text{kHz}$ *to*...100kHz, $D = 50\%$, $t_{on} = DT = \frac{D}{f}$

$$P_{ON} = \frac{1}{T}\int_0^{t_{ON}} V_{ON} I_{ON} dt = V_{ON} I_{ON} D, \qquad P_{ON\_MOS} = 3\times 5\times 1/2 = 7.5W$$

$$P_{ON\_IGBT} = 3\times 2\times 1/2 = 3W$$

TURN – OFF

Delay time: $P = V_{ON} I_{ON} t_s f$

$P_d = 3\times 5\times 0.1\times 10^{-6} f = 1.5\times 10^{-6} f$ (for both IGBT and MOS)

Growth time:

$$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left(V_{ON} + \frac{V_{dc} - V_{ON}}{t_g} t\right) = t_g f I_{ON}\left[\frac{V_{dc}}{2} + V_{ON}\right]$$

$$P_{g\_MOS} = 0.3\times 10^{-6}\times 3\times 205\times f = 184.5\times f\times 10^{-6}$$

$$P_{g\_IGBT} = 0.3\times 10^{-6}\times 3\times 202\times f = 184.5\times f\times 10^{-6}$$

Fall time :

$$P_f = tf\times f\frac{V_{dc}\times I_{ON}}{2}$$

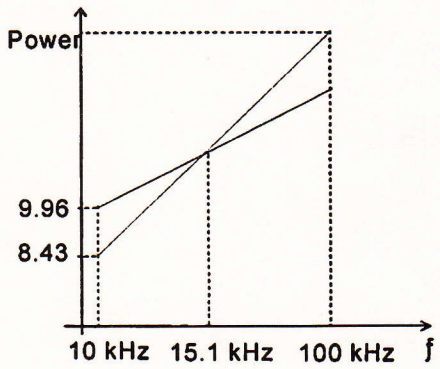
$$P_{f\_MOS} = 0.1\times 600\times 10^{-6} f = 60\times 10^{-6} f$$

$$P_{f\_IGBT} = 0.6\times 600\times 10^{-6} f = 360\times 10^{-6} f$$

Total losses (on-state + turn-off):

$MOS: 7.5 + 246\times 10^{-6} f$

$IGBT: 3 + 543.3\times 10^{-6} f$



MOS is more efficient at high frequencies (due to lower switching losses) > 15 kHz

IGBT is more efficient at low frequencies (due to lower on-state losses) <15kHz

[40%]

(c) In the MOSFET the on-state resistance (on-state voltage) is expected to increase by 2-3 times from 25 to 150 °C. The turn-off losses in MOSFET are generally unaffected. In the IGBT, it depends if a positive temperature coefficient (NPT) or negative temperature coefficient (PT) design is employed. In any case the voltage drop can decrease or increase by a very small amount (say 0.1 V – 1V). The turn-off losses are expected to increase slightly in the IGBT as the tail current gets larger and longer at higher temperatures. Overall, the IGBT will perform better at higher temperatures and therefore it will increase slightly the maximum operating frequency beyond which the MOSFET will be more efficient.

[20%]

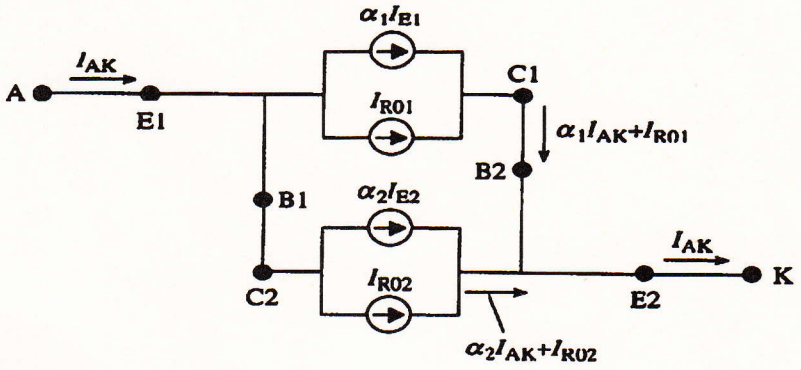
2. . (a) The dI_F/dt condition appears during the turn-on of the thyrsitor. If the rise time is too short (dI_F/dt is too high), the plasma cannot spread fast enough from the edge of the cathode (in the proximity of the gates) to the middle of the cathode. Therefore during the risetime the device conduction is limited to a small area around the edge (compared to the cross-sectional area of the device) and the voltage cannot fall quickly enough. Hence, large instantaneous power dissipation occurs during this period of time which leads to hot spot formation followed by thermal runaway and eventually permanent failure.

Two ways to improve this:

- increase the density of gates per total area – that is to say that we increase the density of gate-cathode inderdigitation. This also has the advantage of shortening the turn-off time (as well as the turn-on time). This is simple but requires advanced layout and photolithography.
- use a smaller auxiliary or pilot thyristor integrated on the same silicon chip with the main thyristor. The current injected into the gate of the pilot thyristor is relatively small but this is amplified by the pilot thyristor so that the gate current delivered to the main thyristor is relatively high. This is however expensive as it needs another component (or larger chip area).

[30%]

(b) (i) The Ebers-Moll equivalent circuit of the thyristor based on the two equivalent circuits for the bipolar transistors is shown below. The gate current was considered to be zero as the thyristor is in the off-state.



From the equivalent circuit above (Fig. 6.5 c) one can obtain the following expression:

$$I_{AK} = \alpha_1 I_{AK} + I_{R01} + \alpha_2 I_{AK} + I_{R02}$$

where I_{AK} is the anode current (same as cathode current) and I_{R01} and I_{R01} are saturation currents (leakage currents) associated with the two transistors.

$$I_{AK} = \frac{I_{R01} + I_{R02}}{1-(\alpha_1 + \alpha_2)}$$

If $\alpha_1 + \alpha_2 < 1$ the thyristor blocks the voltage and the anode-cathode current I_{AK} (i.e. leakage current) is small; of the same order of magnitude as the saturation currents of the bipolar transistors. However when $\alpha_1 + \alpha_2$ approaches one, the leakage current increases and when $\alpha_1 + \alpha_2 = 1$ the device no longer can block the voltage and the device turns on. [30%]

(ii) Breakover occurs when

$\alpha_1 + \alpha_2 = 1$ or $\alpha_{npn} + \alpha_{pnp} = 1$

$$\alpha_{npn} = 0.5 \quad \alpha_{pnp} = 1 - \frac{w_{eff}^2}{2L_p^2}$$

$w_{eff} = w_{drift} - w$ (The effective base of the pnp transistor is the undepleted region of the n –drift region – n-base).

$$\Rightarrow \alpha_{pnp} = 1 - \frac{(w_{drift} - w)^2}{2L_p^2} = 0.5$$

$$\Rightarrow (w_{drift} - w) = L_p$$

$$\Rightarrow w = w_{drift} - L_p \Rightarrow \frac{2\varepsilon_0\varepsilon_r V}{q}\frac{1}{N_D} = (w_{drift} - L_p)^2$$

$$\Rightarrow V = \text{BREAKOVER VOLTAGE} = \frac{qN_D(w_{drift} - L_p)^2}{2\varepsilon_0\varepsilon_r}$$

$$V = \frac{1.6\times10^{-19}\times10^{13}\times10^{6}\times150^2\times10^{-12}}{2\times11.9\times8.854\times10^{-12}} = 170.83V \Rightarrow BREAKOVER$$

For 10^{13} cm^{-3}, the avalanche breakdown voltage ~10^3 V, much higher than the breakover voltage.

[30%]

(iii) The break-over voltage is based on the positive feedback of the two bipolar transitors, while the avalanche breakdown refers strictly to the abrupt multiplication of carriers when the electrical field at one location reaches a critical limit. The break-over voltage is in general smaller (and in some cases significantly smaller) and tends to limit the breakdown before avalanche sets in. Nevertheless if the gains of the npn and pnp transistors are very small (by for example applying heavy lifetime killing), it is possible, in theory that avalanche sets in before break-over. In diodes, only avalanche is possible as there is no positive feedback (no bipolar transistors present) [10%]

3. (i) This device has a built-in PIN diode formed between the n well/n- drift/p+ anode. This diode will prevent the easy collection of holes to the cathode terminal and thus will result in an improved conductivity modulation, with enhanced plasma at the top side of the device. This will offer a lower on-state voltage drop without a severe penalty in the switching speed.

- The n-well is an enhancement layer (as part of the built-in PIN diode) and is responsible for higher electron injection in the drift region at the top side. Its doping concentration needs to be carefully controlled. The higher the doping the better the conductivity modulation and the better the on-state performance. However the higher the concentration the lower the breakdown, as the n- well will force a higher electric peak at the p –well/n-well junction. So its trade-off needs to be carefully assessed.
- The deep p+ at the bottom of the trench is designed to protect the thing gate oxide against electric field peaks. Its role is to push the depletion region down away from the trench. Its action is also helping to faster deplete the n-well and thus allowing a higher doping concentration in the n-well.

- In the off-state the device behaves similarly to an IGBT with most of the voltage supported across the n- drift region. The reverse biased junction is that formed between the p-well/n-weel and the n-drift region. The n-well needs to be completely depleted during the turn-off and off-state.
- The device is turned on by applying a positive voltage onto the gate, thus forming a channel in the p well and an accumulation layer in the n well. This allows injection of electrons into the n- drift.
-In the on-state, the channel formed in the p well still controls the flow of the current. A small fraction of hole current will escape through the relatively lowly doped n well to the cathode short terminal. The built

in PIN diode will ensure high conductivity modulation and as such the n- drift region resistance is reduced significantly.
- The turn-off of the device is achieved by reducing the gate voltage under the threshold voltage. Holes are extracted during turn-off via the n well /p well path. The depletion region extends into the n-drift region, clearing out plasma. Note that the n well needs to be completely depleted during turn-off [50%]

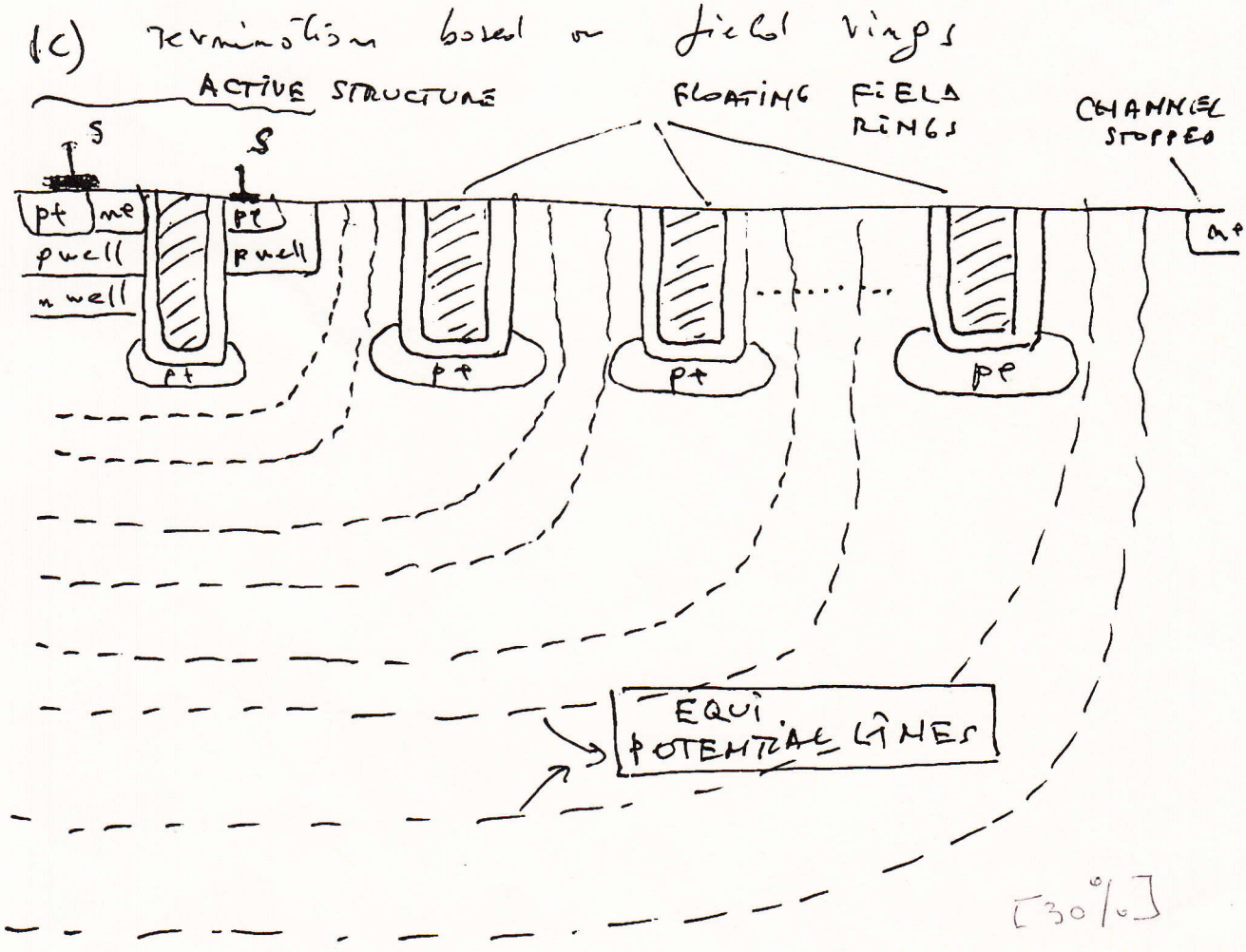
(b)
Advantages:

1. The structure has a reduced on-state voltage drop (on-state resistance or resistance of the drift region) as the PIN diode increases the electron injection at the top side of the drift region (via theinjection of electrons from the n well).
2. The p+ deep p well protects the trench and thus the gate oxide from the high electric fields which can cause reliability problems such as dielectric breakdown or hot carrier injection.

Disadvantages:

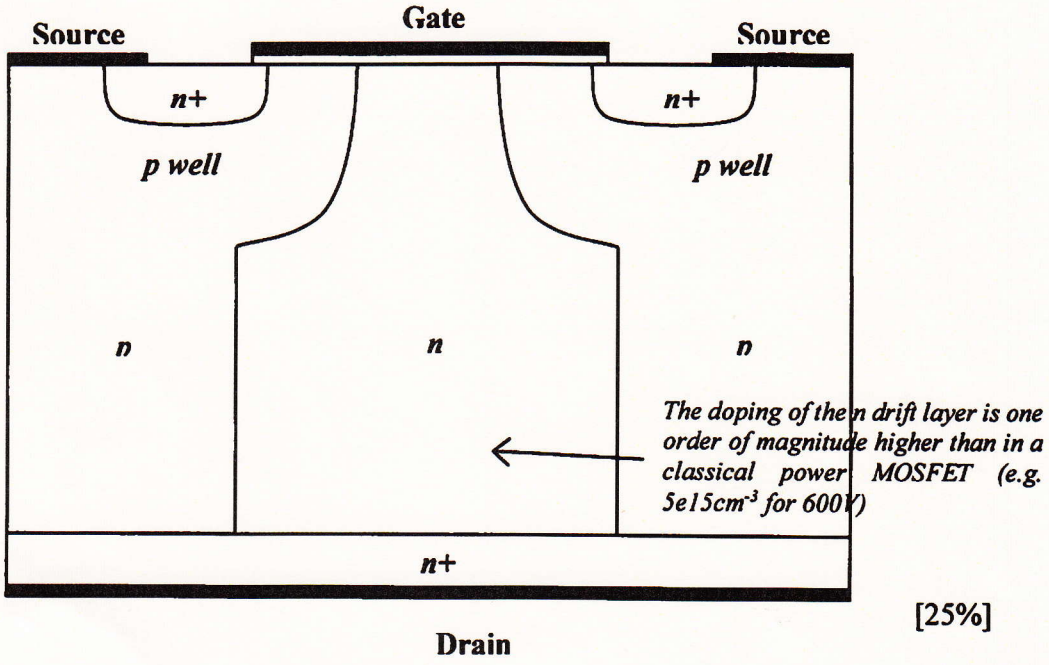
1. The technology is complex (and therefore the cost is high). The insertion of the n well and the deep p+ through the trench are difficult from a process point of view.
2. The injection of extra electrons will slow down slightly the device. The penalty will not be huge as this extra plasma is formed at the top of the device and cleared quickly by the depletion region

[20%]



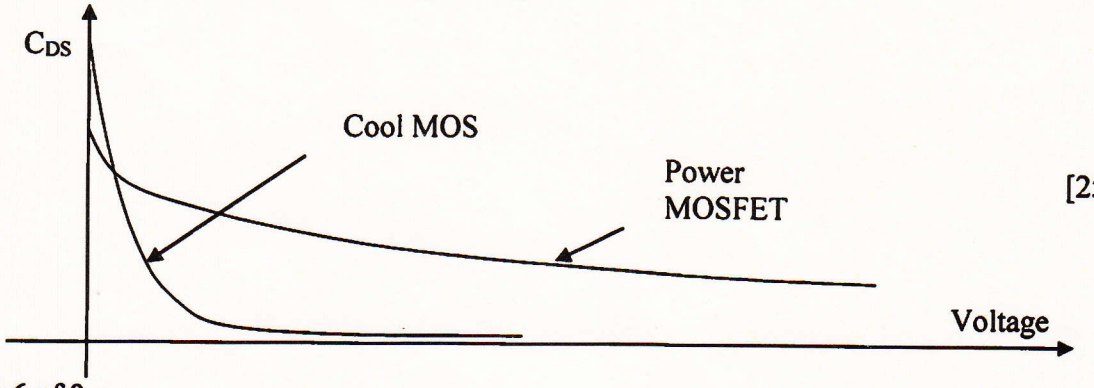
4. (a) (i) The Cool MOS is based the superjunction effect. The superjunction comprises multiple junctions disposed in the drift region with alternate layers of relatively highly doped n and p layers. The drift region is therefore made of thin and highly doped n/p stripes rather than a single n- layer. The depletion of the drift region is in this case dictated by these n/p multiple junctions rather than by the classical p+/n- junction. Since the stripes are very thin (compared to their length), they deplete at much lower voltage (due to the extension of the depletion region across the n/p junctions). The net advantage is a major reduction in the on-state resistance for the same breakdown capability. The electric field distribution is square rather than triangular, and the doping of the n pillars is considerably higher than that of the classical power MOSFET. For the same breakdown a reduction of 5-10 times in the on-resistance is possible.

The Cool MOS is shown below:



[25%]

(ii) The C_{DS} capacitance for the Cool MOS is high to start with, as the multiple junctions have a large (folded) area. At the same time the doping of the n and p pillars are very high limiting the extension of the depletion region at low voltages. These 2 effects lead to very high C_{DS} in Cool MOS at low voltages. At high voltages, in Cool MOS, the whole n-p pillar stack depletes, thus reducing sharply the capacitance. In contrast in Power MOSFET, the capacitance at low voltages is quite low (reduced area and reduced doping), while decreasing with $1/V^2$ at high voltages.



[25%]

reasons

(b) (i) The main resons that SiC, GaN and Diamond are attractive materials for power devices (when compared to Silicon) is that they have a large bandgap which results in a higher critical electric field (as indicated in Table 2) and much lower intrinsic carrier concentration. This allows the design of more highly doped and significantly shallower drift regions which would result in lower on-state resistance (by orders of magnitude) for the same voltage rating. The smaller devices, with smaller drift regions also result in lower switching losses.

SiC

Advantages:

1) Higher critical electric field leading to lower on-state resistance

2) Higher thermal conductivity leading to lower losses and more reliable operation due to lower temperature

Disadvantages

1) cost of the wafer

2) high temperature processing – results in higher processing cost

GaN

Advantages:

1) Higher critical electric field leading to lower on-state resistance

2) Higher 2DEG mobility which results in lower on-state resistance and faster commutation

Disadvantages

1) presence of interface and bulk traps which lead reliability problems

2) cost of the wafers which need epitaxial layers of GaN and AlGaN

Diamond

Advantages:

1) Higher critical electric field leading to lower on-state resistance

2) Higher thermal conductivity leading to lower losses and more reliable operation due to lower temperature

Disadvantages

1) cost of the wafer and only small diameter CVD wafers available.

2) very difficult processing with deep energy levels for both the n and p dopants.

[25%]

(ii) $V_{BR} = \frac{E_{cr} \cdot W_{dl}}{2}$ with $W_{dl} = \sqrt{\frac{2\varepsilon_0 \varepsilon_r V_{BR}}{q N_D}}$

$\Rightarrow V_{BR} = \frac{E_{cr}}{2} \frac{\varepsilon_0 \varepsilon_r}{q N_D}$

$R_{sp} = \frac{W_{dl}}{q \mu_n N_D} = \frac{2 V_{BR}}{E_{cr} \cdot q \mu N_D}$

$\Rightarrow R_{sp} = \frac{4 V_{BR}^2}{E_{cr}^3} \cdot \frac{1}{\varepsilon_0 \varepsilon_r \mu_n}$

$\frac{R_{sp\,SiC}}{R_{sp\,Si}} = \frac{E_{cr\,Si}^3}{E_{cr\,SiC}^3} \cdot \frac{\varepsilon_{r\,Si}}{\varepsilon_{r\,SiC}} \cdot \frac{\mu_{n\,Si}}{\mu_{n\,SiC}}$

$\frac{R_{sp\,SiC}}{R_{sp\,Si}} = \left(\frac{0.3}{3}\right)^3 \cdot \frac{11.9}{10} \cdot \frac{1350}{700} = 0.002295$

$R_{Si} = 435.73\, R_{SiC}$

[25%]

Module 4B2 – 2015 – Assessor's coments

Q1. Calculation of losses question.

This was the most popular questions, answered by all candidates. It was very well answered by most candidates. The question was not too easy and it was pleasing to see that most of the candidates were able to do the power calculations. Not all the candidates were able to make a qualitative assessment of the MOSFETs and IGBTs at high temperature.

Q2. Thyristor question

This was one of the most popular questions. Most of the students answered the theoretical part of the question well. Only a few candidates succeeded in calculating the break-over voltage. Most candidates were able to differentiate between the avalanche breakdown in a PIN diode and the break-over voltage in a thyristor.

Q3. The IGBT question

A difficult question answered only by two candidates. The candidates were not able to spot the shallow superjunction at the top side of the drift region of the IGBT and were not able to understand the injection for the n-enhancement layer

Q4. The Cool MOS and wide bandgap materials question.

This question was taken by 12 candidates and it was relatively well answered. Most of the candidates were able to draw the structure of the COOL MOS and most were able to point out the advantages and disadvantages of the wide bandgap materials compared to silicon. There is some evidence that this question was in most cases last attempted and some candidates ran out of time.