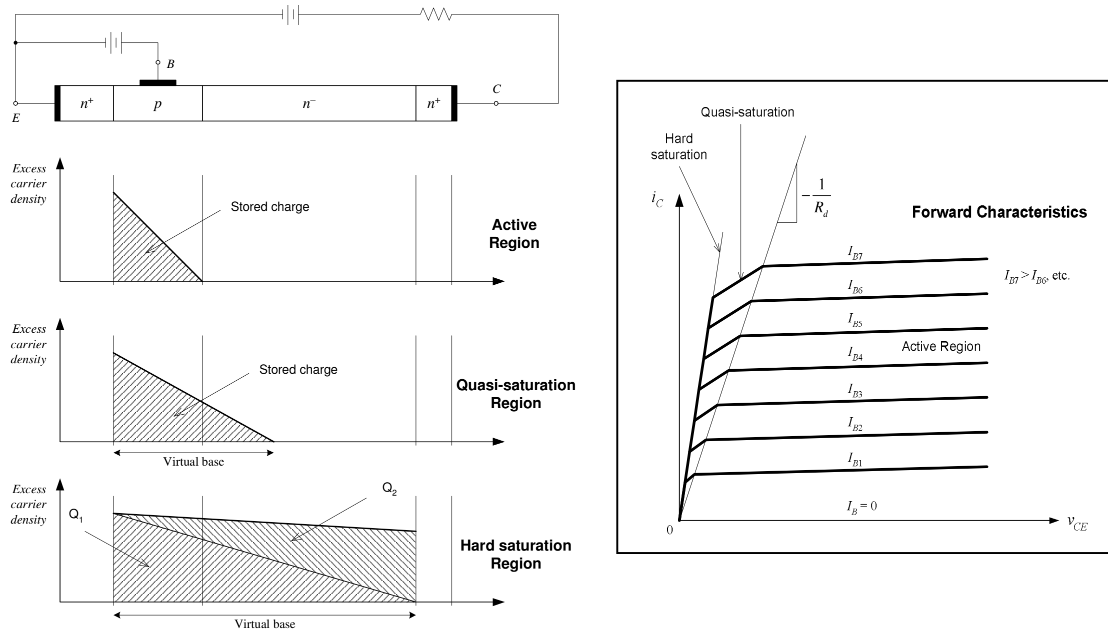
1. (a) There are four important regions in the on-state:

Active region: the base-emitter junction is forward-biased while the base-collector junction is reverse-biased. Since the base-collector region is reverse-biased a depletion region is formed across the base-collector junction. Mobile charge (plasma) is only stored in the base of the BJT (as the collector is largely depleted). The I-V characteristic shows a fairly flat shape and the current increases little with the increase in the collector-emitter voltage.



The quasi-saturation is the condition where the stored charge (plasma) moves into the collector region reducing significantly the depletion region and eventually removing it completely. In this regime, the base-collector junction becomes forward-biased.

The hard saturation occurs when the whole collector region is filled with plasma (excess mobile carriers) and the base-collector junction is fully forward-biased. In this case the base-emitter voltage drop (V_{BEsat}) is virtually cancelled by the base-collector voltage drop (V_{BEsat}) and the only voltage drop across the collector-emitter terminals is given by the resistive drop across the collector region (V_D) which depends on the amount of the plasma stored.

Deep saturation occurs when additional charge is built in the collector region (Q2) leading to excess carriers to increase well above the doping even in the proximity of the n+ collector region.

[30%]

(b) (i) In Non Punch Through IGBTs, the depletion region cannot reach the p+ anode region and the plasma (excess carrier charge) built during on-state cannot be cleared by sweeping out charge with electric field (in the depletion region) but only by carrier recombination. Given the high lifetime of silicon (few microseconds), this results in a current tail [10%]

(ii) $f = \frac{1}{T} =$ $\quad D = 50\%$, $\quad t_{on} = DT = \frac{D}{f}$

t_{on} must be greater than $t_s+t_g+t_{f1}+t_{f2}$. At the limit the minimum ton that still maintains a duty cycle of 50% is t_{on} = 0.1+0.3+0.2+1 = 1.6 microseconds. The maximum frequency in this case is f_{max} = D/t_{on} = 1/(2x1.6) MHz = 312.5 kHz [10%]

[Note that in practice the frequency should be limited by the transient power losses.]

(iii) ON-STATE power $P_{ON} = \frac{1}{T}\int_0^{t_{ON}} V_{ON} I_{ON} dt = V_{ON} I_{ON} D \quad P_{ON} = 2\times 10\times 1/2 = 10W$

TURN – OFF power

Delay time: $P = V_{ON} I_{ON} t_s f$

$P_d = 2\times 10\times 0.1\times 10^{-6} f = 2\times 10^{-6} f$ (for both IGBT and MOS)

Growth time:

$$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left(V_{ON} + \frac{V_{dc} - V_{ON}}{t_g} t\right) = t_g f I_{ON}\left[\frac{V_{dc}}{2} + V_{ON}\right]$$

$$P_g = 0.3\times 10^{-6}\times 10\times 202\times f = 606\times f\times 10^{-6}$$

Fall time 1 & 2:

$$P_{f_1} = t_{f1}\times f\frac{V_{dc}\times(I_{ON} + I_{tail})}{2} = 0.2\times 200\times(10+2)\times 10^{-6} f == 480\times 10^{-6} f$$

$$P_{f_2} = t_{f2}\times f\frac{V_{dc}\times I_{tail}}{2} = 1\times 200\times 2\times 10^{-6} f == 400\times 10^{-6} f$$

Total losses (on-state + turn-off):

$10 + (400 + 480 + 606)\times 10^{-6} f$

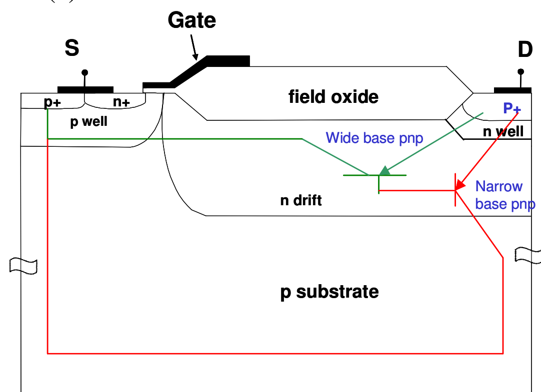
$T_{max} - T_{ambient} = R_{thja}$ *x Power*

$10 + 1486\times 10^{-6} f$ = 150/7.5 = 20 which gives a max allowable f =6.73 kHz [40%]

(iv) The turn-off time and the charge stored in the on-state are likely to increase severely with temperature which will increase the power losses during the turn-off and therefore it is expected that the maximum frequency needs to be reduced further . Alternatively, a package/module used with lower junction to ambient thermal resistance could be used [10%]

This question was attempted by all candidates with an average of 79.09% for undergraduates. This question was virtually answered by all the candidates to a very high standard. It was pleasing to see that the candidates had good knowledge of SMPS systems and calculation of losses in an IGBT. Most of the candidates were able to identify the tail of the IGBT. Almost all candidates were able to work out the max power for a given junction temperature. The question was easier than the others.

2. (a) The LIGBT cross-section is shown below



The presence of the two bipolar pnp transistors having the emitter connected to the drain terminal and the collector to the source terminal are indicated. One of the transistor has a narrow base and wide collector while the other a wide base and a narrow collector. [Note that the names of the terminals could be 'anode and chathode' instead of 'drain and source'].

Turn-on: This is similar to the LDMOSFET. The channel induced at the surface of the p well allows flow into the drift region providing that the anode (drain) junction is forward biased. The electron current acts as the base current for the two pnp transistors leading to injection of holes into the drift region and the p substrate.

On-state: The injection of both holes and electrons into the drift region and the p-substrate leads to accumulation of excess mobile carrier charge formed by electrons and holes in equilibrium. As a result the resistance of the drift layer decreases significantly. Note that the narrow base transistor tends to inject plasma deep in the substrate. This transistor is not present in the vertical devices.

Turn-off: The turn-off process is based on sweeping of holes to the cathode short when the depletion advances in the n- drift region from the p well side. Another major turn-off mechanism is via recombination of holes and electrons in the drift region, especially at the anode side where the depletion region takes time to reach. Unlike in a vertical device, injection in the on-state does not only occur in the drift region but also in the substrate via the narrow base pnp transistor p+ anode/n-epi/p-substrate. Thus accumulation of mobile charge occurs deeply into the p substrate. This charge has to be removed during turn-off which slows down considerably the turn-off process. Therefore, the turn-off of the LIGBT is generally slow characterized by a specific long tail

Blocking: This is similar to the LDMOSFET – based on RESURC concept-, however in most cases the leakage current is slightly higher because of the gain of the pnp transistor during avalanche.

Advantages compared to LDMOSFET:

- Higher current capability & lower equivalent on-state resistance

Disadvantages compared to LDMOSFET:

- Higher turn-off losses, lower operating frequency, injection of plasma into the substrate which could affect the ioperation of other circuits around. [30%]

(b) The *dV/dt* effect appears during turn-off when a high forward voltage is re-applied to the structure. There is a maximum *dV/dt* rating above which the displacement current created through the junction capacitance will be greater than the breakover current, thus resulting in a parasitic re-turn-on (the device refuses to turn-off).

One solution to minimize the effect of the *dV/dt* (or in other words to increase the maximum *dV/dt* rating) is to use cathode shorts. The shorts can collect some of the displacement current that could otherwise turn-on the npn transistor. Since a large component of the displacement current is safely absorbed via the cathode shorts, the slope dV_F/dt, can be higher without triggering the parasitic re-turn-on of the thyristor. The smaller the short resistance R_s, the more effective the cathode short is, and the higher the maximum dV_F/dt rating. The effect of the cathode short can also be seen as an effective reduction in the current gain of the npn transistor (α_2). As a result the thryristor feedback reaction is weaker, making the *dV/dt* rating higher.
There are two more advantages resulting from the use of cathode shorts:

- (i) the increase in the breakover point – this gets closer to the maximum breakdown (dictated by avalanche)
- (ii) a faster turn-off. This is due to lower plasma injectionand removal of part of the hole current from the base via the cathode shorts.

There are however two major drawbacks:

- (iii) the turn-on is slightly slower. Also the breakover current and the hold current are higher which means that for the same gate current, the cathode-shorted thyristor opens more slowly (in time and voltage). These effects can be reduced by employing a structure with a high density gate-cathode interdigitation.
- (iv) The on-state losses are slightly higher as the npn transistor has lower gain and therefore the plasma injection will be slightly weaker. This is nevertheless compensated by lower turn-off losses.

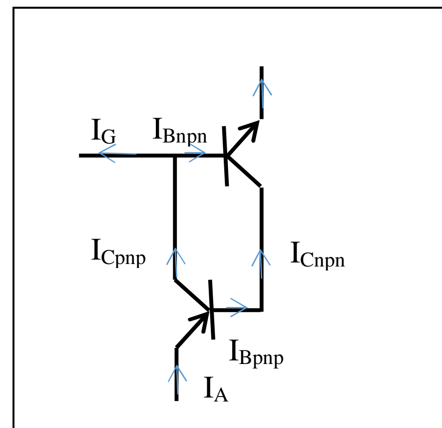
Similarly to the cathode-shorted thyristors, the anode-shorted devices are used to increase *dV/dt* rating as well as the turn-off speed and the breakover voltage. This time the gain of the pnp transistor is lowered. The anode shorts allow higher level of cathode-gate interdigitation as no top surface area is wasted to form the cathode shorts. Anode shorts are slightly more difficult to fabricate as they require a photolithographic process on the backside of the wafer, but they offer good overall trade-off between robustness & turn-off speed on one hand and turn-on and on-state losses on the other hand. [30%]

(c) The condition for the turn-off of the GTO thyristor is to turn-off the npn transsitor and thus to 'cut off' the positive feedback between the npn and pnp transistor.

$$I_{Bnpn} < \frac{I_{Cnpn}}{\beta_{npn}} = \frac{I_{Cnpn}(1-\alpha_{npn})}{\alpha_{npn}}$$

(1) $I_{Cpnp} = I_G + I_{Bnpn}$

(2) $I_{Cnpn} = I_{Bpnp} = (1-\alpha_{pnp}) I_A$



From this, after some calculations:

$$\alpha_{pnp} I_A - I_G < \frac{I_A(1-\alpha_{npn})(1-\alpha_{pnp})}{\alpha_{npn}}$$

Resulting in the turn-off condition: $I_G > \frac{I_A}{G}$ where G is called the turn-off gain with $G = \frac{\alpha_{npn}}{\alpha_{npn} + \alpha_{pnp} - 1}$

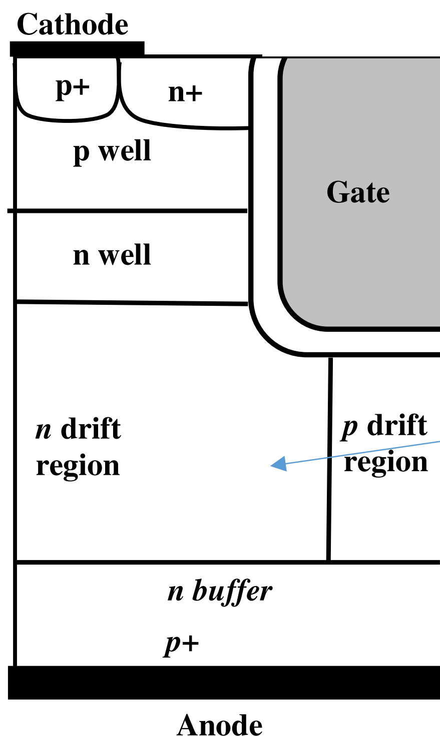
[30%]

G should be as high as possible for safe turn-off. The most effective way to increase G is to reduce α_{pnp} by introducing anode shorts and/or a strong buffer above the anode junction.

[10%]

The question was attempted by 8 undergraduates and 3 graduates with an average of 55.63% for undergraduates. The candidates found confusing the calculation of the gain in a GTO and with the exception of one candidate none has reached a correct result. The theoretical part on dV/dt was answered well, but some candidates struggled with the description of the LIGBT and its advantages over an LDMOSFET.

3. (a) This device is a Superjunction Trench IGBT. Just as a Trench IGBT it has a trench MOS gate and a p+ anode injector of holes and just as a superjunction the drift region incorporates n and p drift pillars, with charge compensation to increase the breakdown ability of the device. The n drift/p-drift design is similar to that of the Cool MOS device. If charge compensation between the n drift region and p region is achieved, the electric field within the drift region will be 'almost' flat leading to high breakdown capability.



Superjunction for high breakdown capability. Note that the charge in the n drift region has to be compensated by the charge in the p drift region. For a 600 V device the n charge could be 2e15cm-3 and 5um width while the p drift could be 1e16cm-3 and 1um width.

This device also has a built-in PIN diode formed between the n well/n- drift/p+ anode. This diode will prevent the easy collection of holes to the cathode terminal and thus will result in an improved conductivity modulation, with enhanced plasma at the top side of the device. This will offer a lower on-

state voltage drop without a severe penalty in the switching speed. The n-well is an enhancement layer (as part of the built-in PIN diode) and is responsible for higher electron injection in the drift region at the top side. Its doping concentration needs to be carefully controlled. The higher the doping the better the conductivity modulation and the better the on-state performance. However the higher the concentration the lower the breakdown, as the n- well will force a higher electric peak at the p –well/n-well junction. So its trade-off needs to be carefully assessed.

In the off-state the voltage is supported across the superjunction (n- drift/p drift region) region. The reverse biased junction is that formed between the pwell/n-well and the depletion extends in the superjunction structure. The n-well needs to be completely depleted during the tum-off and off-state. –

The device is turned on by applying a positive voltage onto the gate, thus forming a channel in the p well and an accumulation layer in the n well. This allows injection of electrons into the n- drift. ln the on-state, the electron channel formed in the p well still controls the flow of the current. A small fraction of hole current will escape through the relatively lowly doped n well to the cathode short terminal. The PIN diode will ensure high conductivity modulation and as such both the n- drift and p drift regions will be modulated by plasma, leading to low on-state resistance.

The tum-off of the device is achieved by reducing the gate voltage under the threshold voltage. Holes are extracted during turn-off via the n well /p well path. The depletion region extends into the superjunction region, clearing out plasma. Note that the n well needs to be completely depleted during tum-off

[60%]

(b) Advantages and disadvantages compared to a Trench IGBT:

Advantages

l. The structure has a reduced on-state voltage drop (on-state resistance or resistance of the superjunction region) as the PIN diode increases the electron injection at the top side oft the drift region (via the injection of elections from the n well).

2. The superjunction region form of the n-drift and p-drift pillars leads to very high breakdown capability as it allows a flat distribution of the electric field.

Disadvantages:

l. The technology is complex (and therefore the cost is high). The insertion of the p drift region and the n well are difficult from a process point of view. 2. The injection of extra electrons from the n well will slow down slightly the device. The penalty will not be huge as this extra plasma is formed at the top of the device and cleared quickly by the depletion region

[20%]

b) Advantages and disadvantages compared to a CoolMOS:

Advantages

l. Higher current density and lower on-state resistance due to bipolar conduction in the drift region

2. Lower temperature dependence in the on-state, as the decrease in the mobility at high temperature is compensated by an almost equivalent incrase in the bipolar injection.

Disadvantages:

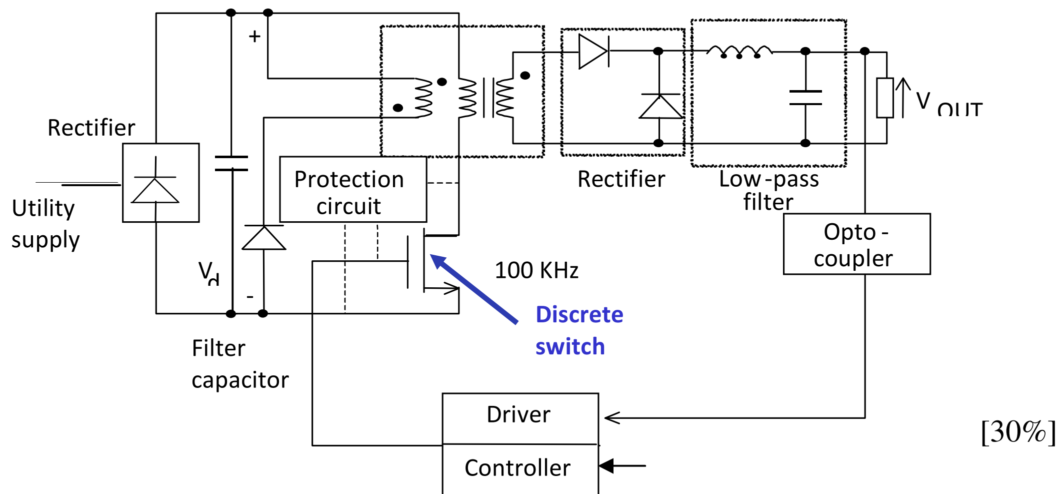
l. 0.7 needed for opening the anode junction (not existent in a Cool MOS)

2. The Superjunction IGBT is slower and has higher turn-off losses than the Cool MOS because of the bipolar charge stored in the drift region.

[20%]

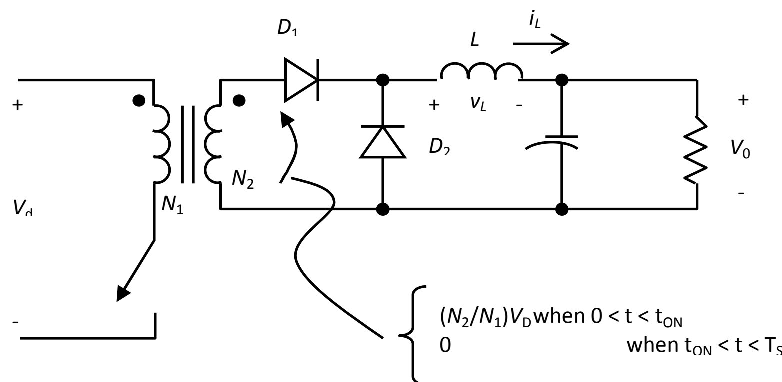
The average mark was 66.43%. This was perceived by the candidates as a relatively difficult question but there were some very good attempts.

4. (a) A typical AC-DC converter is shown below. The signal provided by the utility supply is first rectified and filtered to obtain a high DC voltage V_d. The DC voltage is then converted back into an AC form by switching the transistor ON/OFF at high frequencies (e.g. 100 KHz). The transistor is placed on the primary side of the transformer and therefore sees a high voltage (in the OFF state) and a lower current in the ON state. Since the transistor operates ON/OFF with relatively low losses, the efficiency of the system can be dramatically improved! The ac voltage at the secondary is then rectified by the output diodes and a low-pass filter is used to extract its average DC component so that the load sees a constant DC voltage. A feedback is provided from the output voltage to the gate of the transistors via a controller. This ensures that no matter what the load is, the output voltage remains unchanged. This can be done by finely adjusting the ON to OFF time ratio of the transistor.



[30%]

(b)

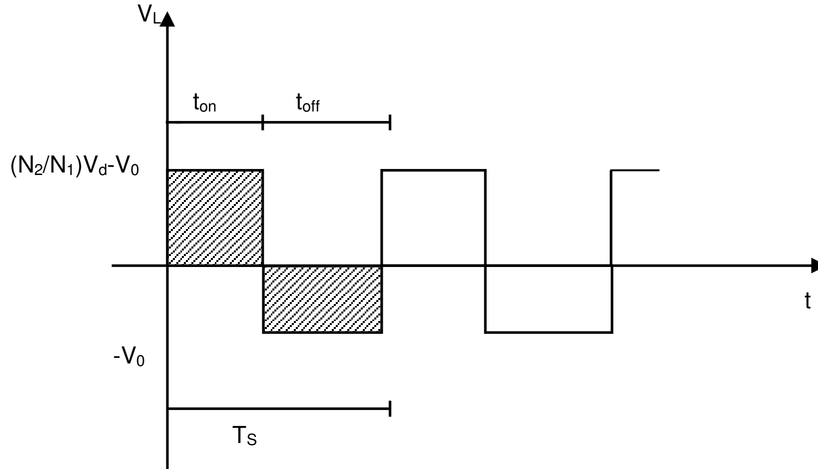


Initially when the switch is ON, D1 is forward biased and D2 is reverse biased. Therefore:

$V_L = \frac{N_2}{N_1} V_d - V_0$ when switch is ON

When the switch is OFF the inductor current i_L circulates through D2:

$V_L = -V_0$ when switch is OFF

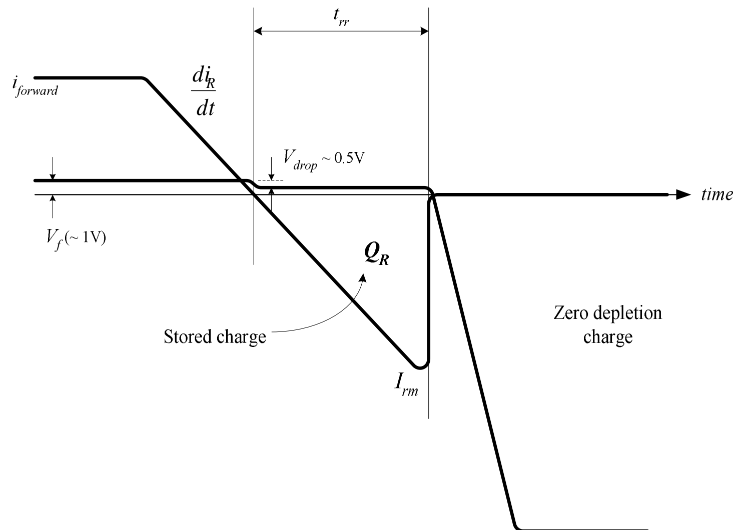


Since the average power dissipated in the inductor is zero, we can equate the integral of the inductor voltage over one period to zero. The result is a DC voltage V_0 across the load:

$V_0 = \frac{N_2}{N_1} V_d \frac{t_{on}}{T_S}$ where $\frac{t_{on}}{T_S}$ is the duty cycle D and $\frac{N_2}{N_1}$ is the transformer turns ratios.

$$t_{ON}\left(\frac{N_2}{N_1} V_d - V_0\right) = V_0\left(T_S - t_{ON}\right) \Rightarrow V_0 = \frac{N_2}{N_1} V_d \frac{t_{ON}}{T_S}$$ [20%]

(c) (i)



$$Q_R = \tfrac{1}{2} I_{rm} t_{rr},$$

where $$t_{rr} = \frac{I_{rm}}{\left(\frac{dI_R}{dt}\right)} \qquad (1)$$

$$\Rightarrow Q_R = \frac{\frac{1}{2} I_{rm}^2}{\left(\frac{dI_R}{dt}\right)}$$

$$\therefore I_{rm} = \sqrt{2Q_R\left(\frac{dI_R}{dt}\right)}$$

$$= \sqrt{2 \times 0.6\ \mu\text{C} \times 25\ \text{A}/\mu\text{s}}$$

$$= 5.46\ \text{A}$$

Substituting into (1) we get

$$t_{rr} = \frac{5.46\ \text{A}}{(25\ \text{A}/\mu\text{s})}$$

$$= 0.21\ \mu\text{s}$$ [40%]

(c) (ii)
If the junction temperature is increased to 150 C, the conductivity modulation is going to be stronger (due to injection of carriers increase and the increase in the lifetime) and as a result the charge stored will be significantly greater resulting in higher peak of revrese recovery current and longer reverse recovery time. [10%]

The question was very well answered by most of the candidates with an average of 78.53%. It was very pleasing to see that most of the candidates were able to calculate the reverse recovery charge and time and they answered the first part on the AC to DC converter very well