Version HJJ/4

EGT0
ENGINEERING TRIPOS PART IA

Monday 10 June 2019 9 to 12.10

Paper 3

ELECTRICAL & INFORMATION ENGINEERING

*Answer **all** questions.*

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

SECTION A

1 **(short)**

(a) Calculate and sketch the Thévenin and Norton equivalents of the circuit of Fig. 1. [6]

(b) A load resistor R_L is connected across terminals A and B of the circuit of Fig. 1. Calculate the value of R_L that achieves maximum power transfer and calculate the power dissipated in the load. [4]

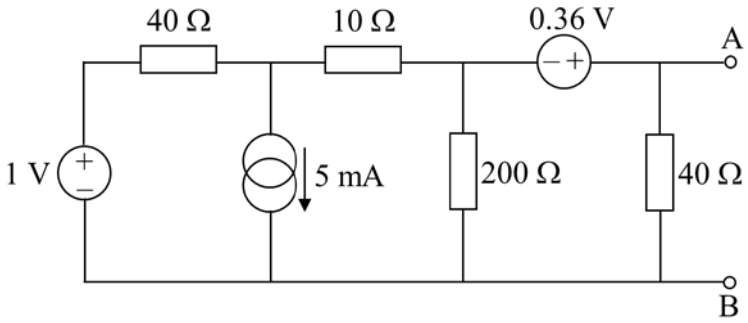

Fig. 1

2 **(short)** Figure 2 shows a simple induction heater used in a domestic kitchen stove top. The heater coil is modelled as an inductor of 90 μH and it is wired in parallel with a capacitor *C*.

(a) Calculate the capacitance, *C*, required to achieve a resonant frequency of 24 kHz. [4]

(b) The capacitance *C* is set to 100 nF and the power supply is set to apply v_{in} with r.m.s. voltage of 200 V at a frequency of 24 kHz. Find the peak amplitude of the current through the resistor and its phase with respect to the voltage v_{in}. [6]

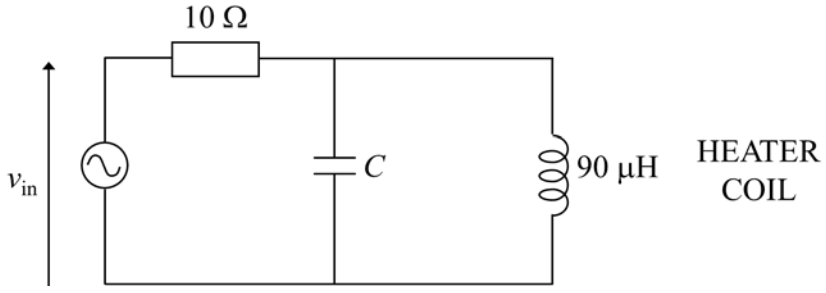

Fig. 2

3 **(short)** A transformer with a primary:secondary turns ratio of 10:1 has a load of impedance $(0.3 + j0.2)\ \Omega$ connected to its secondary winding and its primary winding is connected to a 240 V supply. The equivalent circuit parameters of the transformer referred to the primary are:

$$R_1 = 6\ \Omega,\ R_2' = 4\ \Omega,\ X_1 = 7\ \Omega,\ X_2' = 3\ \Omega.$$

The iron loss resistance R_0 and magnetising reactance X_0 are large enough to be neglected.

(a) Calculate the impedance of the load referred to the primary. [2]

(b) Calculate the load current. [3]

(c) Calculate the real and reactive power in the load. [3]

(d) Calculate the transformer efficiency. [2]

4 **(long)** Figure 3(a) shows a field effect transistor (FET) configured as a source-follower amplifier.

(a) Draw the small-signal equivalent circuit for mid-band frequencies. [4]

(b) Derive expressions for the small-signal voltage gain, the input impedance and the output impedance. [8]

(c) Evaluate the quantities derived in (b) given that the small-signal parameters of the FET are $g_m = 10$ mA V^{-1} and $r_d = 20$ kΩ, and R_1 is 10 MΩ and R_2 is 5 kΩ. [4]

(d) Due to electrical interference from the mains power supply, a low frequency noise signal at 50 Hz is induced at the drain node of the FET circuit. The effects of this noise can be modelled by including a small-signal noise source V_N at the drain of the circuit as illustrated in Fig. 3(b), and by setting v_{in} to zero volts.

(i) Draw the small-signal equivalent circuit. [4]

(ii) Derive an expression for the small-signal voltage gain $|v_{out}/V_N|$ and calculate the value of this gain given the parameters listed in (c). [4]

(e) A load resistor R_L of 100 Ω is connected across the output terminals of Fig. 3(b). To filter out low frequency noise signals, a capacitor C_{out} is placed at the output of the circuit. Explain whether C_{out} should be placed in series or in parallel with R_L. Using the values obtained in part (c), calculate the value of C_{out} required to achieve a 3 dB cut-off frequency of 200 Hz. [6]

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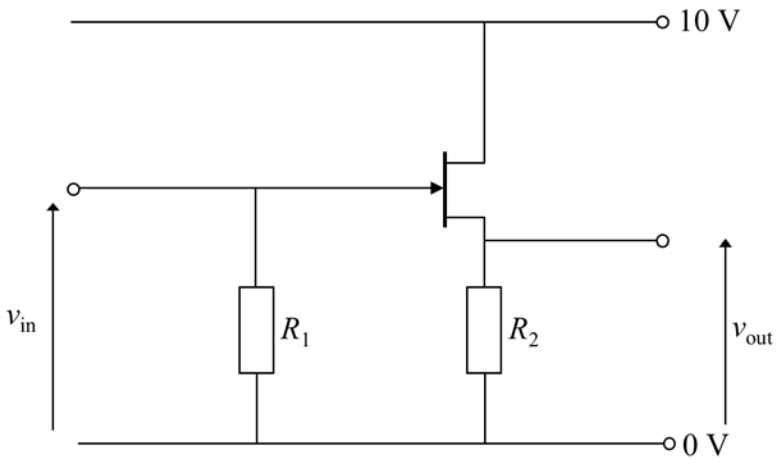

Fig. 3(a)

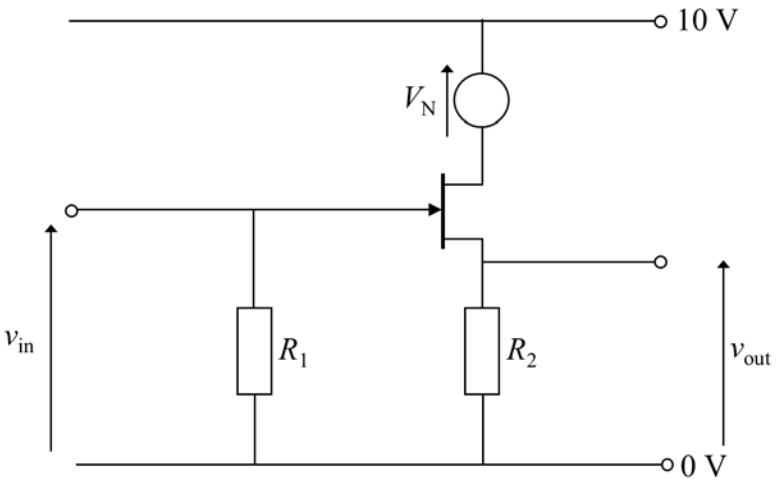

Fig. 3(b)

5 **(long)**

(a) In the integrator circuit of Fig. 4(a) the op-amp can be considered ideal. At time $t < 0$, $v_{in} = 0$ and $v_{out} = 0$. Show that at time $t \geq 0$, v_{out} is given by

$$v_{out} = \beta \int_0^t v_{in} dt$$

and find an expression for the constant of proportionality β in terms of resistance R_1 and capacitance C. [6]

(b) The constant β is set to $\beta = -6.3 \times 10^3 \text{ s}^{-1}$. At time $t < 0$, $v_{in} = 0$ and $v_{out} = 0$. At time $t \geq 0$ a sinusoidal input v_{in} is applied to the circuit of Fig. 4(a). Sketch v_{out} as a function of t if v_{in} is given by:

(i) $v_{in} = 0.1 \sin(2\pi \times 1000t)$, that is, a sine wave of peak amplitude 0.1 V and frequency 1 kHz, [6]

(ii) $v_{in} = 0.1 \sin(2\pi \times 10t)$, that is, a sine wave of peak amplitude 0.1 V and frequency 10 Hz. [6]

(c) In the circuit of Fig. 4(b), the op-amp can be considered ideal. A resistor R_2 is in parallel with capacitor C.

(i) Derive an expression for the small-signal gain $|v_{out} / v_{in}|$ of the circuit in Fig 4(b). [6]

(ii) If the capacitance C in Fig. 4(b) is set to 3.18 nF, calculate the value of R_2 required to achieve a 3 dB cut-off frequency of 10 kHz. [6]

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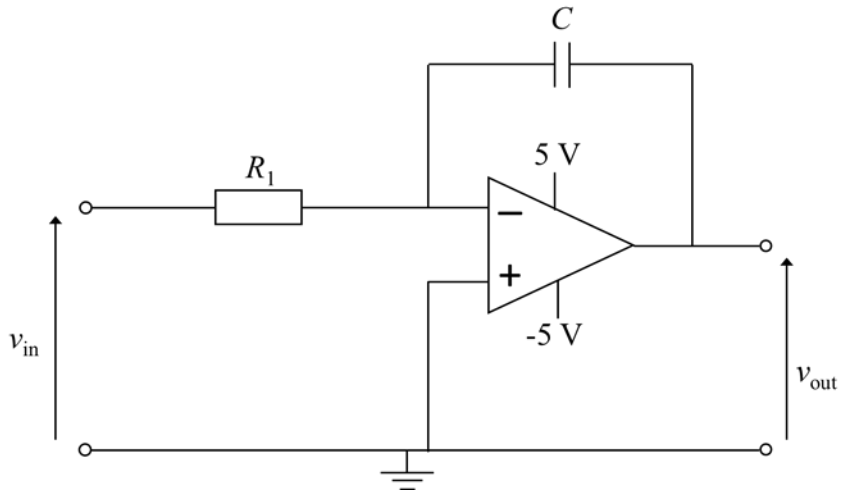

Fig. 4(a)

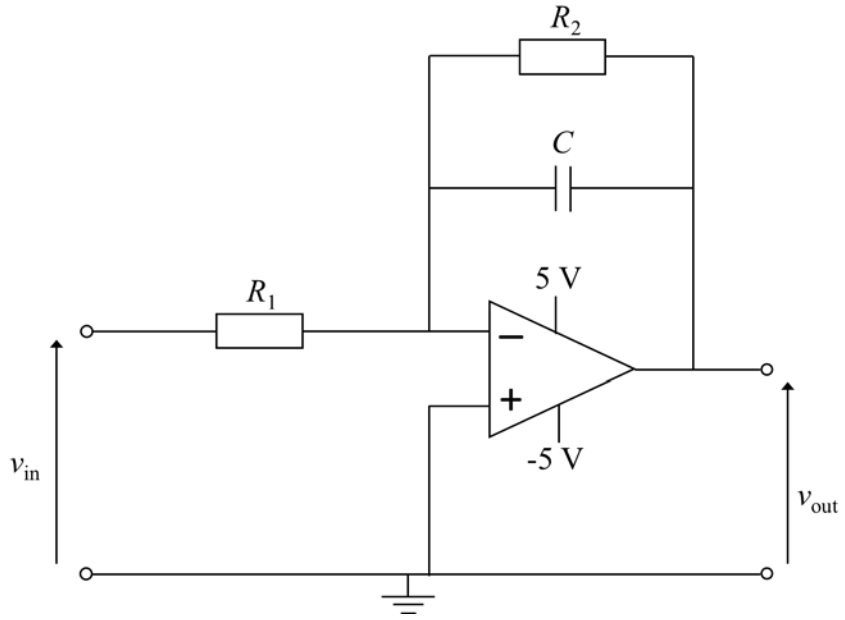

Fig. 4(b)

SECTION B

6 **(short)**

(a) A combinational logic design has four inputs M, N, O, P. The single output Y is HIGH if two or more inputs are HIGH. Otherwise Y is LOW. Using a Karnaugh map, derive the expressions for Y in Sum of Products (SoP) and Product of Sums (PoS) form. [6]

(b) Modify the expressions in (a) using De Morgan's theorem for NAND and NOR gate only implementations. Assuming gates with any number of inputs are available, which implementation will require fewer gates? [4]

7 **(short)**

(a) Figure 5 shows a 4-bit Digital to Analog converter (DAC).

(i) Identify the Least Significant Bit (LSB) and Most Significant Bit (MSB) inputs. [1]

(ii) If the op-amp is ideal and R = 1 kΩ, what are the input impedances at N1 and P1? [2]

(iii) Calculate V_{out} when all the inputs are connected to HIGH (5 V). [2]

(b) What are the drawbacks of this design? With a brief explanation, suggest an alternative DAC architecture that does not have these drawbacks. [5]

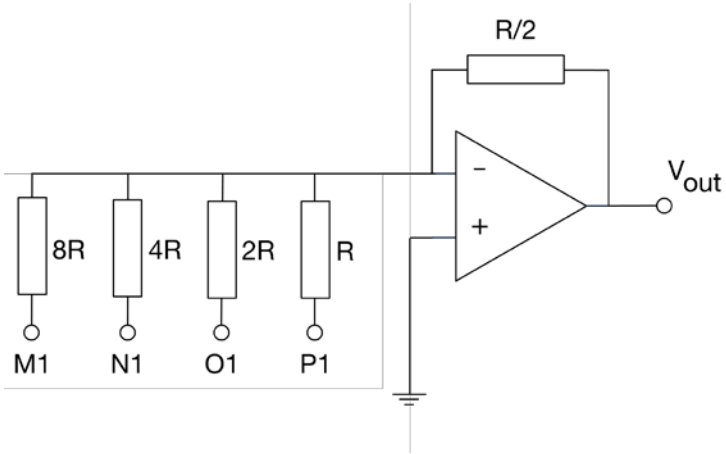

Fig. 5

8 **(short)**

(a) What is a static hazard in a combinational digital circuit? [3]

(b) Identify potential static 0 or static 1 hazards when the four-variable function Z is implemented where $Z = \sum(1, 3, 5, 7, 8, 9, 12, 13)$. Take A, B, C and D to be the four variables with A being the most significant. How can these hazards be avoided? [7]

9 **(long)** A 4 bit synchronous binary up counter is to be designed using JK flip-flops.

(a) Write down the complete truth table. [6]

(b) Construct the Karnaugh maps and derive the logic expressions for the J and K inputs. [6]

(c) Draw the full circuit diagram. Explain how carry in and carry out signals could be implemented in this design. [12]

(d) Draw the outputs Q_n (where n = 1, 2, 3, 4) corresponding to 10 clock cycles. Assume a 10 MHz clock frequency. [6]

SECTION C

10 **(short)**

(a) Describe what is meant by:

(i) magnetic flux, and

(ii) magnetic flux density *B*.

How are these concepts relevant to flux in the electromagnet sketched in Fig. 6? [5]

(b) Calculate the current required to produce $B = 0.2$ T in the air gap if $l_g = 2$ mm, $l_c = 40$ mm, $N = 200$ turns and the electromagnet is made from a linear magnetic material with relative permeability 250. State any approximations made. [5]

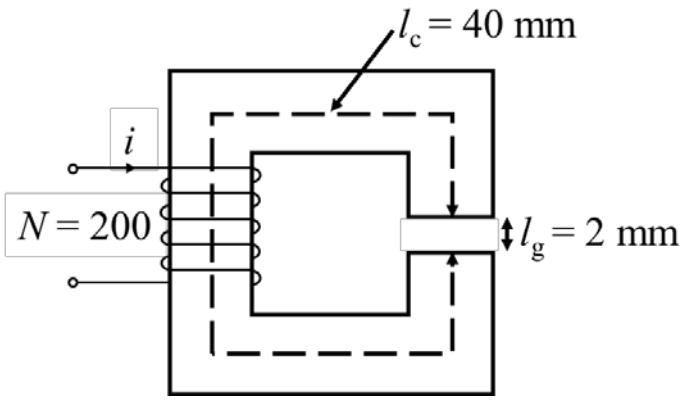

Fig. 6

11 **(long)**

(a) State Gauss' law for electrostatics, and derive an expression for the capacitance of an isolated conductive sphere of diameter d in air. [5]

(b) Derive an expression for the electric field surrounding an infinitely long isolated straight wire of radius R in air with a static charge density of ρ C m^{-1}. [5]

(c) Explain the principle of linear superposition for potential fields. Derive an expression for the capacitance per unit length between two parallel straight wires, each of radius R with centres separated by distance d (where $d >> R$). [10]

(d) Two wires 20 mm in diameter with centre-to-centre separation 2 m in air are to be used to carry high voltage. What is the capacitance per unit length between the wires? If the breakdown field of air is $> 10^6$ V m^{-1}, what is the maximum voltage the wires can carry? [10]

12 **(short)** A straight infinitely long wire is placed in the plane of a square coil and parallel to one side as shown in Fig. 7. Each side of the coil is 10 mm long. What is the magnetic flux through the coil if its centre is 150 mm from the wire which carries a current of 2 A? If the current in the wire alternates at 50 Hz, approximately how many turns should the coil have to generate an alternating potential of 2 μV across its terminals? [10]

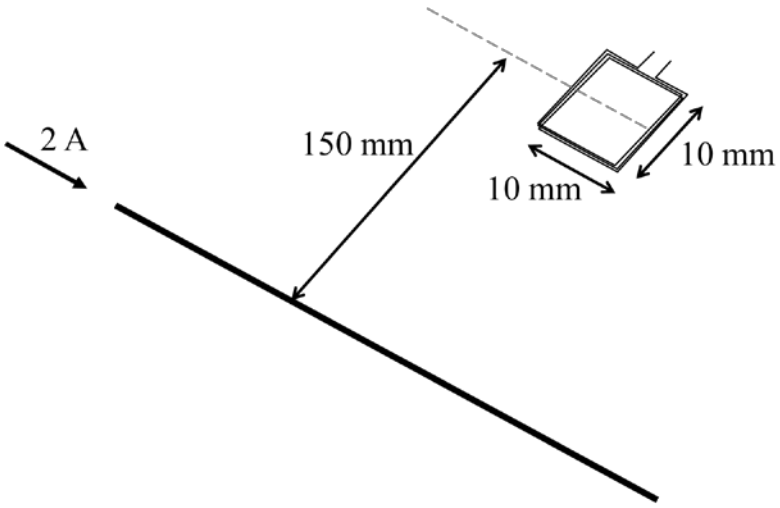

Fig. 7

END OF PAPER

NUMERICAL ANSWERS

Paper 3

ELECTRICAL & INFORMATION ENGINEERING

1 (b) 20 Ω, 3.125 mW

2 (a) 489 nF

(b) 14.3 A ∠ -59.6°

3 (a) 30 + j20 Ω

(b) 48 A

(c) 691.2 W, 460.8 VAR

(d) 75%

4 (c) 10 MΩ, 0.976, 97Ω

(d) -0.005

(e) 4.04 μF

5 (c) 5 kΩ

7 (a) -4.6875 V

10 (b) 1.72 A

12 2.66×10^{-10} Wb, 24 turns