Version DP/3

EGT2
ENGINEERING TRIPOS PART IIA

Monday 29 April 2019 9.30 to 11.10

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM
CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

1 (a) Give the reasons for the popularity of CMOS technology in the design of digital logic systems instead of bipolar devices. What are the disadvantages of CMOS? Your answer may include references to: implementation, compactness, input and output levels, and drive capability, as well as any other factors you consider important. [20%]

(b) With the aid of a diagram, show how to determine the noise margins from the input and output logic levels V_{IL}, V_{IH}, V_{OL} and V_{OH}. [20%]

(c) Implement a CMOS NAND gate using the minimal number of transistors. [20%]

(d) A CMOS inverter is run from a supply V_{DD} = 5 V as shown in Figure 1. It is fabricated from two transistors each with a device transconductance of k_n and k_p, respectively. The threshold voltages for the NMOS and PMOS devices are 1 V and -1 V, respectively. The battery connected to the source of the NMOS device supplies V_A = 1 V.

(i) Derive an expression for the inverter switching point voltage V_{SP}, at which the output and input voltages are equal. [30%]

(ii) Design a minimum-sized CMOS inverter operating with the switching point of $V_{DD}/2$ using the transistor parameters in Table 1. [10%]

You may assume the following equations for the drain current for the n-type MOSFET:

$$I_{DS} = \frac{k}{2}[2(V_{GS}\text{-}V_{TN})V_{DS}\text{-}V_{DS}^2], \text{ for } V_{DS} < (V_{GS}\text{-}V_{TN}), \quad (1)$$

$$I_{DS} = \frac{k}{2}(V_{GS}\text{-}V_{TN})^2, \text{ for } V_{DS} \geq (V_{GS}\text{-}V_{TN}), \quad (2)$$

and for the p-type MOSFET:

$$I_{SD} = \frac{k}{2}[2(V_{SG}\text{-}|V_{TP}|)V_{SD}\text{-}V_{SD}^2], \text{ for } V_{SD} < (V_{SG}\text{-}|V_{TP}|), \quad (3)$$

$$I_{SD} = \frac{k}{2}(V_{SG}\text{-}|V_{TP}|)^2, \text{ for } V_{SD} \geq (V_{SG}\text{-}|V_{TP}|), \quad (4)$$

where the symbols have their usual meaning.

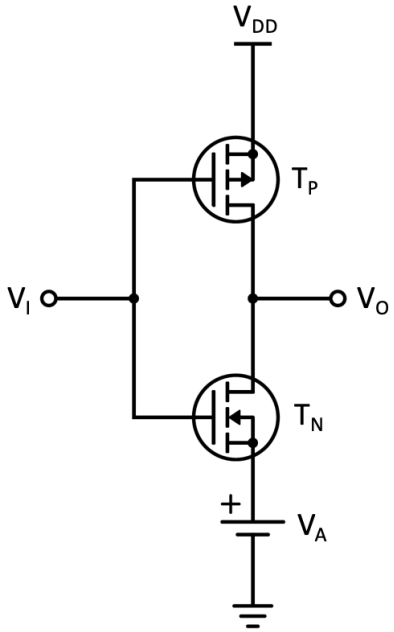


Fig. 1

Table 1: Transistor Parameters.

Parameter	**NMOS**	**PMOS**
k’	300 μAV^{-2}	100 μAV^{-2}
W_{min}	1.0 μm	1.0 μm
L_{min}	1.0 μm	1.0 μm

2 (a) Briefly describe the operation principle of a Schmitt inverter. Sketch a graph depicting a typical voltage transfer characteristic for a Schmitt inverter, and indicate the output high-to-low transition, the output low-to-high transition and the hysteresis. What is the significance of these three terms? [30%]

(b) How might such a gate be used to receive digital signals transmitted along a cable of significant length, and what advantages would this be expected to give? [20%]

(c) Figure 2 shows the configuration of a simple static random-access memory cell. Explain briefly the mode of operation of this circuit, and describe the role of the signals *word*, *bit*, and $\overline{bit}$ in allowing data to be written and read. [25%]

(i) State the measures needed to be considered in the design of the inverters A and B to allow the circuit to work correctly. [10%]

(ii) Describe additional circuit elements necessary for interfacing the cell to an external circuit. [15%]

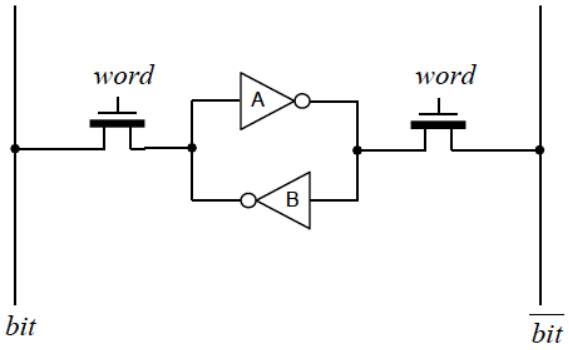


Fig. 2

3 (a) Briefly discuss the advantages and disadvantages of implementing logic functions with *multiplexers*, *ROMs*, *LUTs*, and *PLAs*. [20%]

(b) Consider the VHDL code in Fig. 3. Derive the logical function and draw a circuit implementation. [30%]

(c) A synchronous 3-bit up/down counter with a Gray code sequence is needed. The counter should use J-K flip-flops, and should count up when an UP/DOWN control input is 1 and count down when the control input is 0.

(i) Design the counter by drawing the state diagram and the state table. [20%]

(ii) Determine the Boolean equations for the J-K flip-flop inputs and draw a circuit implementation. [30%]

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY Q4 IS
        PORT ( x  : IN STD_LOGIC_VECTOR(1 TO 3) ;
                f  : OUT STD_LOGIC ) ;
END Q4 ;

ARCHITECTURE Behavior OF Q4 IS
BEGIN
        WITH x SELECT
                        f <= '0' WHEN "000",
                             '0' WHEN "100",
                             '0' WHEN "111",
                             '1' WHEN OTHERS;

END Behavior ;
```

Fig. 3

4 (a) Explain the differences between *Mealy* and *Moore* sequential circuits. Give an example each. [20%]

(b) Determine the functional behaviour of the circuit in Fig. 4. Assume that input x is driven by a square wave signal. [30%]

(c) Figure 5(a) shows the circuit for a BCD-to-7-segment display decoder, with *w* the Most Significant Bit (MSB).

(i) Build the truth table and find the output functions for *a* and *b*. [20%]

(ii) Implement the circuit using a technology of your choice. Comment on its advantages. [20%]

(iii) If the waveforms shown in Fig. 5(b) are applied to the decoder input, determine the sequence of digits that appears on the display. [10%]

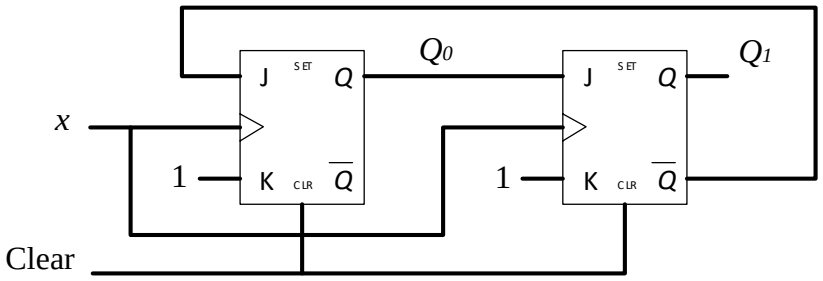
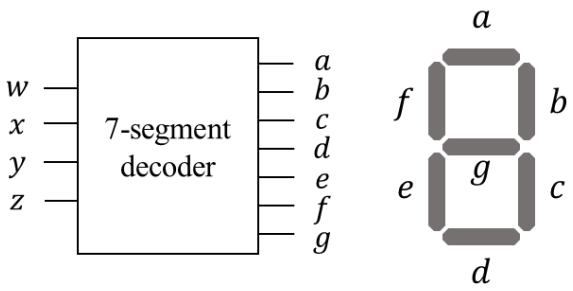
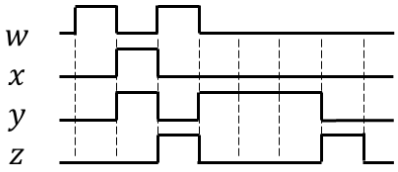


Fig. 4



(a)



(b)

Fig. 5

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