EGT2
ENGINEERING TRIPOS PART IIA

Wednesday 01 May 20192 to 3.40

Module 3B3

## SWITCH-MODE ELECTRONICS

Answer not more than three questions.
All questions carry the same number of marks.
The approximate percentage of marks allocated to each part of a question is indicated in the right margin.

Write your candidate number not your name on the cover sheet.

## STATIONERY REQUIREMENTS

Single-sided script paper

## SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

## Version TL/3

1 A single phase, full-wave, diode rectifier is shown in Fig. 1. The input AC voltage has a Root-Mean-Square (RMS) value $V$ and a frequency $f$. The AC source is considered as an ideal power supply without internal impedance. The load is purely resistive and the resistance is $R$. The diodes are assumed to be ideal.


Fig. 1: Single phase diode rectifier
(a) Sketch the load voltage $v_{o}$ and load current $i_{o}$ against time.
(b) Derive the expression of the average load current and the peak value of the largest harmonic of the load current.
(c) In order to smooth the load voltage, an inductor $L$ can be connected with the load. Draw the circuit with the inductor $L$. Derive the expression of the RMS value of the ripple voltage at the load, assuming that $2 \pi f L \gg R$.
(d) If the ripple current at the load can be ignored when the inductor is very large, sketch the current at the AC input against time and calculate the power factor at the input.
(e) Instead of using an inductor, a capacitor $C$, can be connected at the output to smooth the load voltage. Draw the circuit. By using the simplified method, sketch the load voltage against time and state the assumption you have made. Derive the expression of the peak-to-peak value of the ripple voltage at the load.
(f) Give two advantages of using the inductor over the capacitor for smoothing the load voltage.

## Version TL/3

2 (a) Draw the cross-section structure of an IGBT cell and explain briefly the phenomenon of conductivity modulation in the drift region.
(b) A power device is formed of an IGBT rated for 1.2 kV placed in parallel with a MOSFET rated for 600 V . Assume that gate terminal is common and the IGBT and the MOSFET have the same threshold voltage and same surface area. The cathode of the IGBT is connected to the source of the MOSFET and the anode of the IGBT is connected to the drain of the MOSFET.
(i) Briefly analyse the behaviour of the power device in terms of breakdown voltage and leakage current during the off-state (blocking mode).
(ii) Draw schematically and explain briefly the on-state output characteristics of the MOSFET, the IGBT and the power device. Use at least two different gate voltages.
(iii) Describe briefly the operation of the power device during the reverse conducting mode (the current flowing from the source/cathode terminal of the power device to the drain/anode terminal of the power device). Assume that in this mode the gate is shorted to the source/cathode terminal.
(iv) Explain briefly what would happen with the on-state characteristics if the MOSFET and the IGBT were integrated in the same silicon chip. Draw the crosssection of such a power device.

3 (a) A Buck-Boost converter is shown in Fig. 2. The output current is assumed to be constant as $I_{o}$. The switching period is $T$ and the duty ratio is $k$. The inductor current is continuous and all devices are assumed to be ideal.


Fig. 2: Buck-Boost converter
(i) Derive the expression of the average output voltage $V_{2}$ as a function of the duty ratio $k$ and input voltage $V_{1}$.
(ii) At the steady state, sketch $v_{L}, i_{L}, i_{D}, i_{C}$, and $v_{C}$ against time. The charging and discharging transitions are assumed to be linear.
(iii) Derive the critical value of the inductor $L_{c r i}$ when the inductor current is at the boundary of continuous conduction.
(iv) Derive the critical value of the capacitor $C_{c r i}$ when the capacitor voltage is at the boundary of continuous voltage of the output.
(b) A Zeta converter is shown in Fig. 3 and all components are assumed to be ideal.


Fig. 3: Zeta converter
(i) Assuming continuous conduction of current at both inductors, derive the expression of the output voltage $V_{o}$ as a function of duty ratio $D$ and input voltage $V_{i}$ at the steady state (hint: the voltage polarity of any capacitor is unchanged at any time of the steady state).
(ii) Give two advantages of the Zeta converter over the Buck-Boost converter.

4 A three-phase battery charger is shown in Fig. 4. All power electronic devices are ideal. The ideal transformer has a primary to secondary turns ratio of $1: 1$. The filter inductance $L_{f}$ is 10 mH and the grid is ideal with zero internal impedance. The line voltage of the input is 400 V . The rated power is 22 kW at unity power factor. The battery voltage varies from 330 to 410 V and the internal impedance is negligible. The DC capacitor is very large.


Fig. 4: Battery charger circuit
(a) Calculate the modulation depth of the rectifier when using sinusoidal PWM if the average voltage of the DC capacitor $V_{d c}$ is required to be maintained at 740 V .
(b) If the rectifier is under square-wave operation, calculate $V_{d c}$. Sketch the line voltage and calculate the magnitude of its largest harmonic line current at the input.
(c) If $T_{1 A}, T_{2 A}, T_{1 B}$, and $T_{2 B}$ operate under unipolar switching scheme and the zero state angle is $\alpha$, derive the charger average output voltage $V_{o}$ in terms of $V_{d c}$ and $\alpha$. Sketch the waveforms of the gate signals of devices in the H -Bridge, the voltage between terminal A and $\mathrm{B} v_{A B}$, and $i_{L}$ against time.
(d) If the peak to peak value of the ripple current into the battery is less than 1 A and the inductance $L$ is 10 mH , calculate the switching frequency $f$ of the H -Bridge. The average voltage of DC capacitor $V_{d c}$ is required to be maintained at 740 V .
(e) Why it is less necessary to have capacitor connected at the output when the battery has negligible internal impedance?

Version TL/3

THIS PAGE IS BLANK

