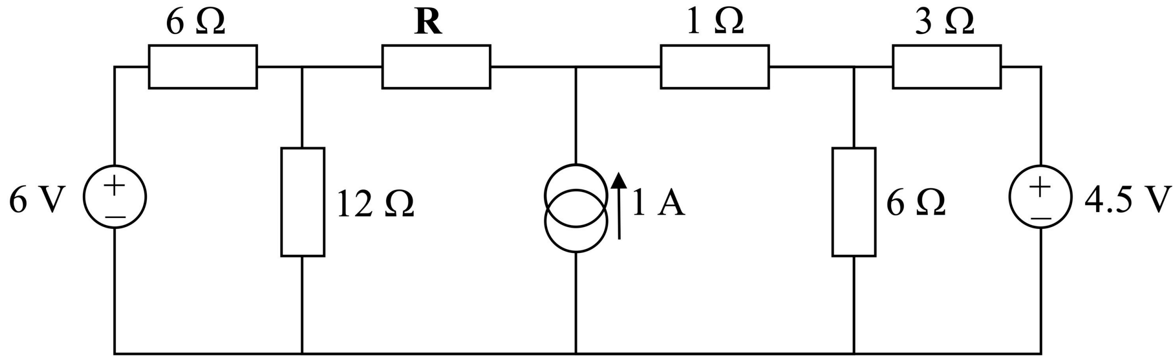
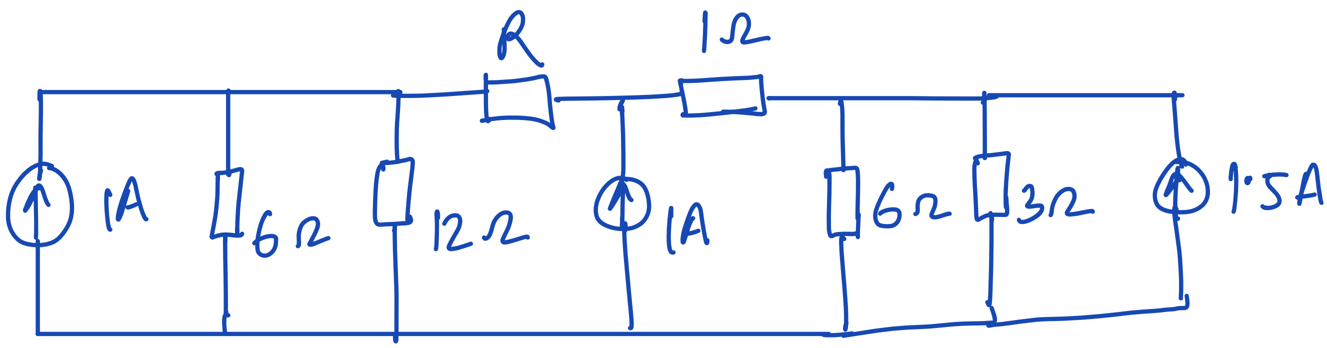
1A Paper 3 – Electrical and Information Engineering 2024 (Cribs)

Q1

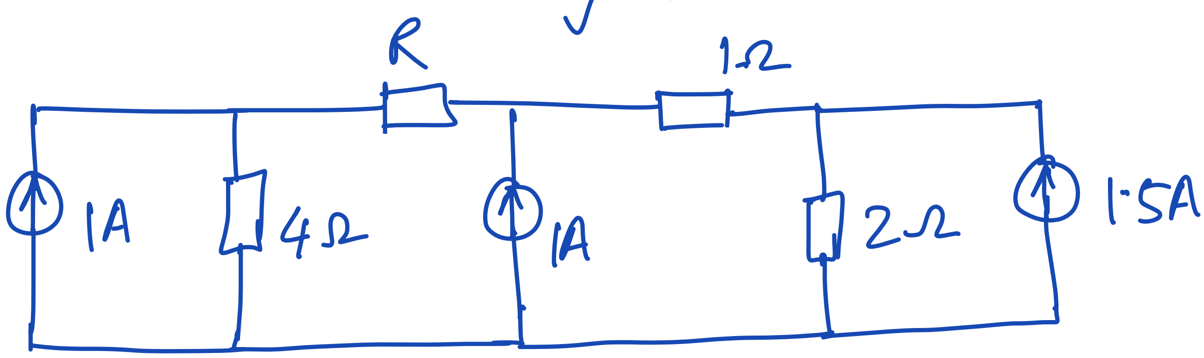
Section A



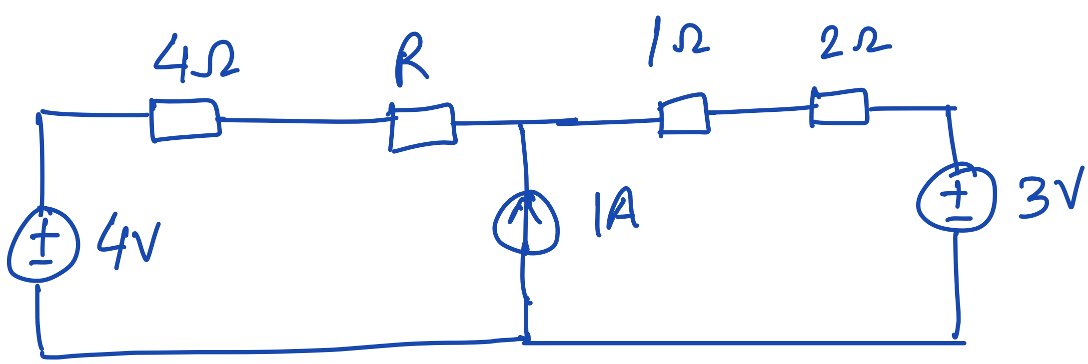
Transforming the circuit, we get:

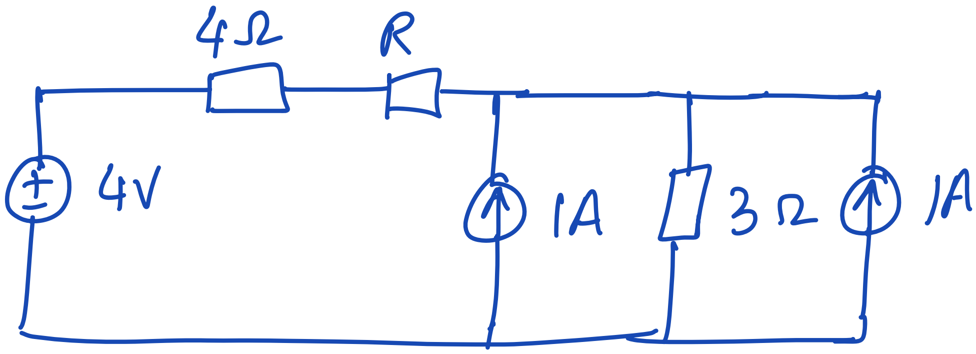


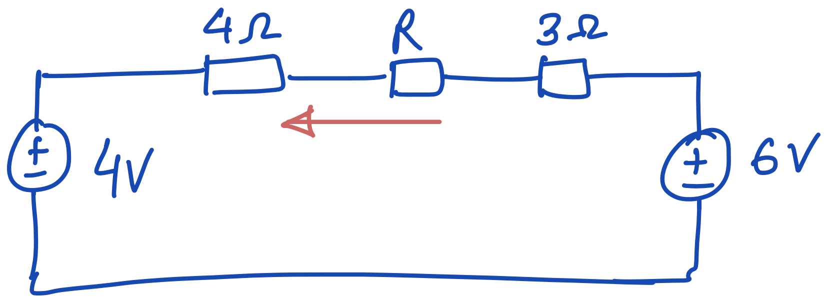
From the above, we get,



Then,

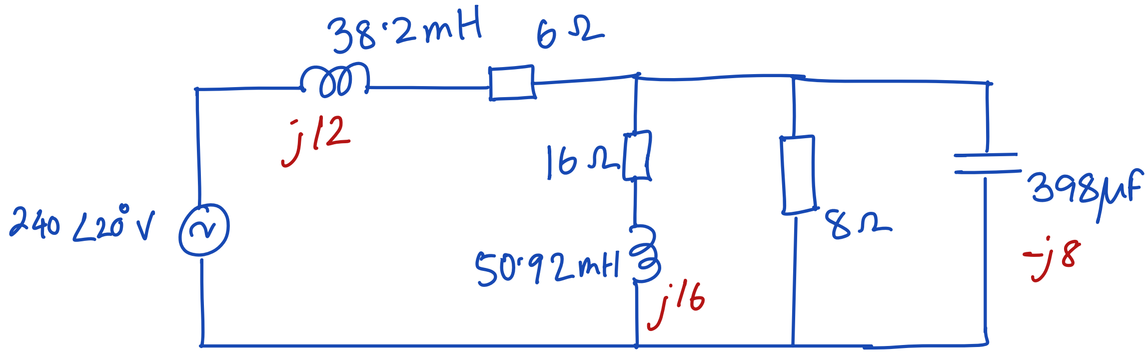






hence $I = \dfrac{6-4}{4+3+R} = \dfrac{2}{7+R}$

Q2



Total impedance $= (6+j12) + \left[(16+j16) \,\|\, 8 \,\|\, (-j8)\right] \ \Omega$

$= 10{\cdot}70 + j9{\cdot}176 \ \Omega$

$= 14{\cdot}09 \angle 40{\cdot}61^\circ \ \Omega$

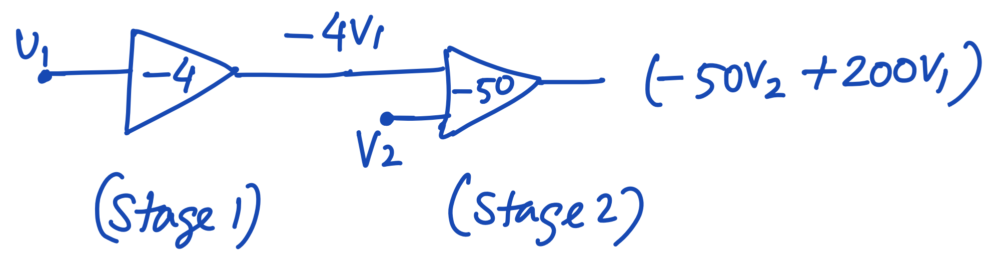
Supply current $= \dfrac{240 \angle 20^\circ}{14{\cdot}09 \angle 40{\cdot}61^\circ} = 17{\cdot}033 \angle -20{\cdot}61^\circ$ Amp.

Q3 First part is bookwork.

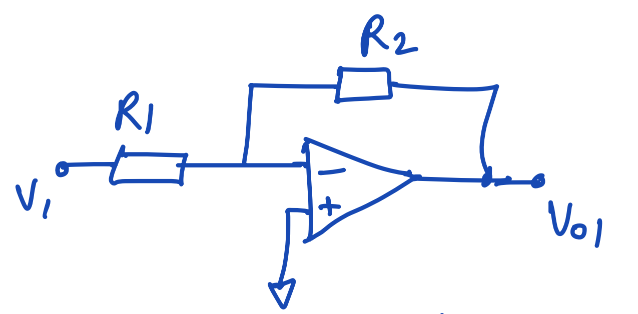
$$V_{out} = -R_f\left(\frac{V_{in1}}{R_1} + \frac{V_{in2}}{R_2} + \frac{V_{in3}}{R_3}\right)$$

Rewrite the expression $V_{out} = 50(4V_1 - V_2)$.

Therefore, we can use a two stage design like the following:



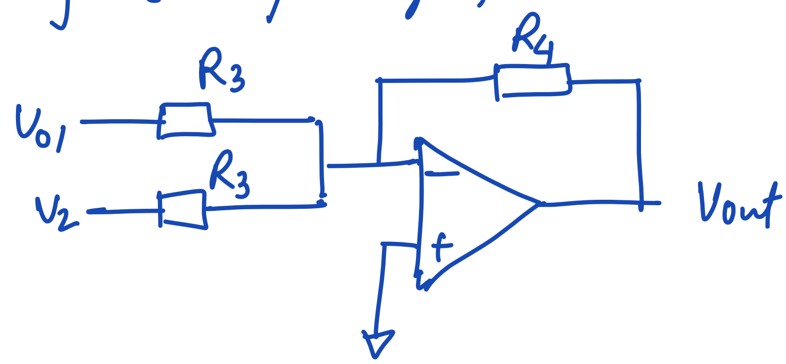
For stage 1, we can use an inverting amplifier



$$V_{o1} = -\frac{R_2}{R_1}V_1$$

Let us take $R_1 \sim 10k$ (too low values are best avoided as source resistances are small or negligible. Hence, $R_2 = 40k\Omega$

For second stage amplifier, we use the following summing amplifier:



We need,

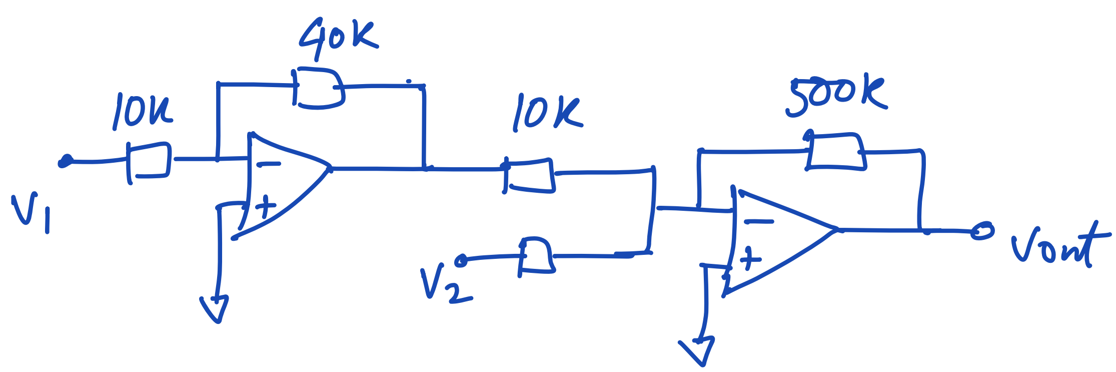
$$V_{out} = -R_4\left(\frac{V_{01}}{R_3} + \frac{V_2}{R_3}\right).$$

$$V_{out} = -\frac{R_4}{R_3}\left(V_{01} + V_2\right)$$

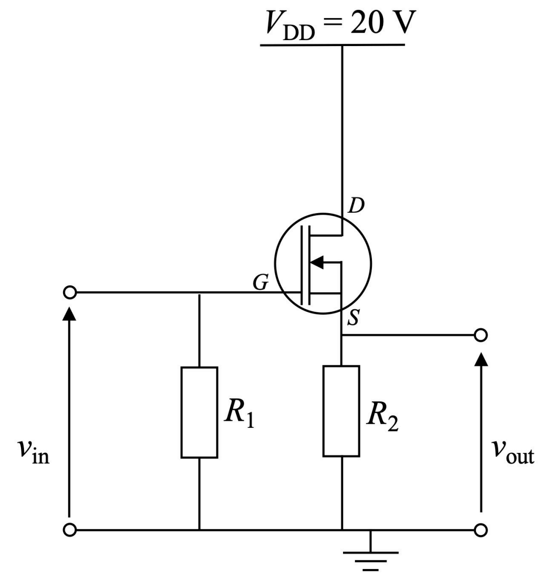
We need, $\frac{R_4}{R_3} = 50$

If R_3 is chosen at $10k\Omega$, $R_4 = 500k\Omega$

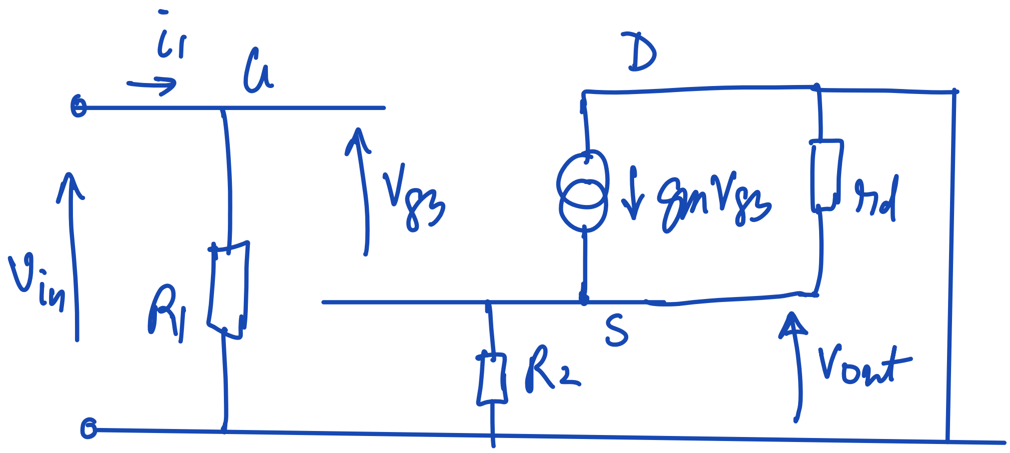
Full circuit.



Q4



Small signal model:



i) Input impedance : $R_{in} = \frac{v_i}{i_1} = R_1$

ii) No load gain : $V_{in} = V_{gs} + V_{out}$ —— ①

Also, $V_{out} = g_m V_{gs} (R_2 \| r_d)$ —— ②

We need to eliminate V_{gs} to find gain.

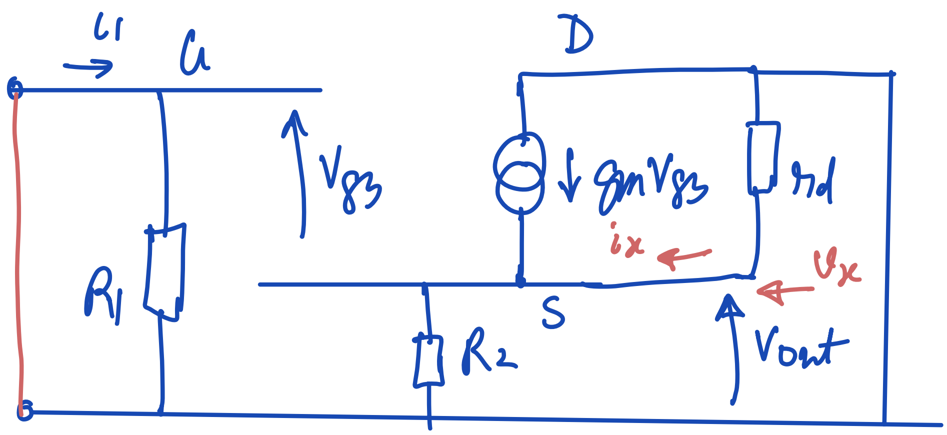
From ②, we get, $V_{g3} = \dfrac{V_{out}}{g_m(R_2 \| r_d)}$

$$V_{in} = V_{out} + \frac{V_{out}}{g_m(R_2 \| r_d)}$$

$$V_{in} = V_{out}\left(1 + \frac{1}{g_m(R_2 \| r_d)}\right)$$

$$V_{out}/V_{in} = \frac{g_m(R_2 \| r_d)}{1 + g_m(R_2 \| r_d)}.$$

iii) Output impedance: Short circuit the input. Push a voltage at the output & find the current.



$$V_{g3} = -v_x$$

$$v_x = (g_m V_{g3} + i_x)(R_2 \| r_d)$$

$$v_x = (i_x - v_x g_m)(R_2 \| r_d)$$

$$v_x[1 + g_m(R_2 \| r_d)] = i_x (R_2 \| r_d)$$

$$v_x/i_x = \text{Output impedance} = \frac{(R_2 \parallel r_d)}{1 + g_m (R_2 \parallel r_d)}$$

Values: $R_{in} = 10\,M\Omega$.

$$\text{Gain} = \frac{5 \times 10^{-3} (20K \parallel 20K)}{1 + 5 \times 10^{-3} (20K \parallel 20K)}$$

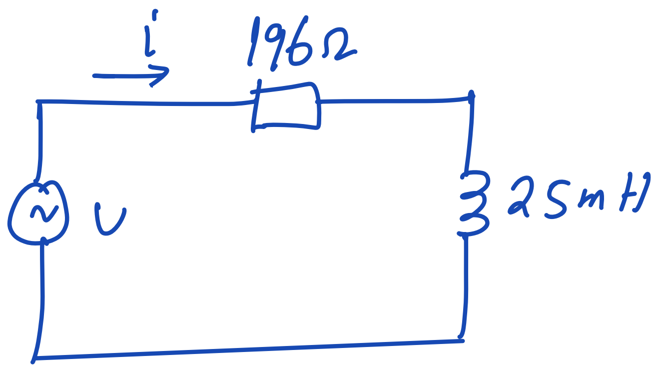
$$= 0.98$$

$$\text{Output impedance} = \frac{10K}{1 + 5 \times 10^{-3} \times 10K}.$$

$$= 196\,\Omega.$$

(b) This is a non-inverting source follower circuit. It has a high input impedance, low output impedance & a gain close to unity. This is very useful as a pre-amplifier circuit, for example in a microphone where source impedance is very high & requires a buffer circuit to isolate & drive the lower impedance loads without causing large signal attenuation.

(c) The circuit with load looks like the following:



$$i = \frac{v}{196 + j2\pi f\, 25\times10^{-3}}.$$

For the load current to drop at 70% the mid-band value, we get

$$196 = 2\pi \times 25\times10^{-3} f$$

$$f = 1247 \text{ Hz}.$$

5

(a) The turns ratio N = voltage ratio $= \frac{240}{40} = 6:1$

Impedance is transferred across as $\times N^2$.

hence load transferred to the H.V side

$$Z_L' = (8 + j4) \times 36$$
$$= (288 + j144)\,\Omega$$

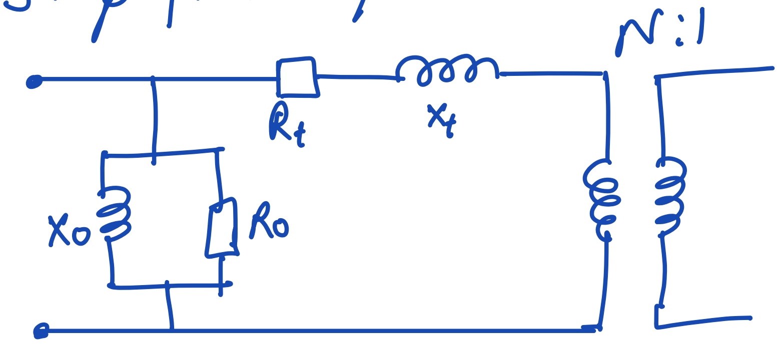
(b) R_t (or R_{t1}) represents the series resistance of the windings.

X_t (or X_{t1}) represents leakage flux across the transformer.

R_0 represents hysteresis & eddy current loss in the core (iron loss)

X_0 represents inductance on windings on core.

(c) Simplified equivalent circuit



For open circuit test: Ignore X_t & R_t.

Given, $V_{primary} = 240V$, $I_{primary} = 0.1A$, $P = 10W$.

$$R_o = \frac{V^2}{P} = \frac{(240)^2}{10} = 5760\,\Omega.$$

$$X_o = \frac{V^2}{Q} \qquad Q^2 = (VI)^2 - P^2 = (240 \times 0.1)^2 - (10)^2 = 476.$$

$$Q = 21.87 \text{ VAR}$$

Therefore, $X_o = \dfrac{(240)^2}{21.87} = 2640\,\Omega$

For short circuit test, ignore R_o & X_o.

Given, $V_{primary} = 45V$. $I_{primary} = 2A$, $P = 20W$.

$$R_t = \frac{P}{I^2} = \frac{20}{2^2} = 5\,\Omega$$

$$X_t = \frac{Q}{I^2}, \quad \text{Also, } Q^2 = (VI)^2 - P^2$$

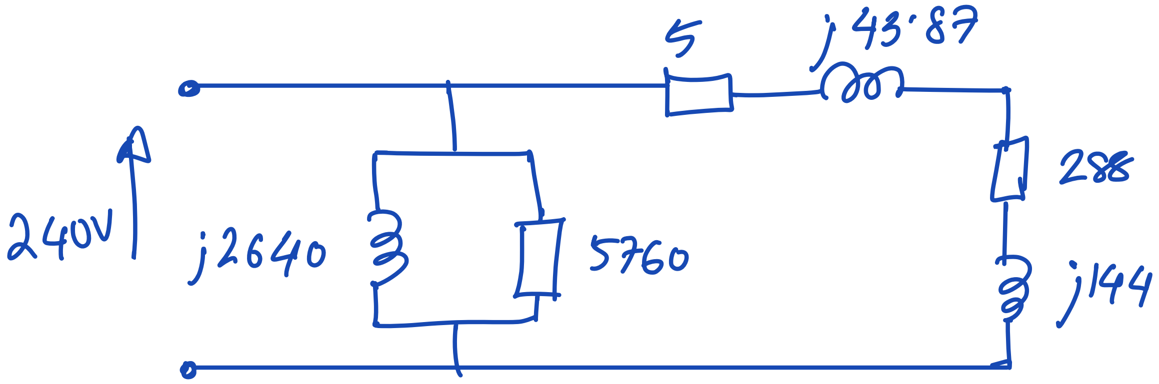
$$= (45 \times 2)^2 - (20)^2$$

$$= 7700$$

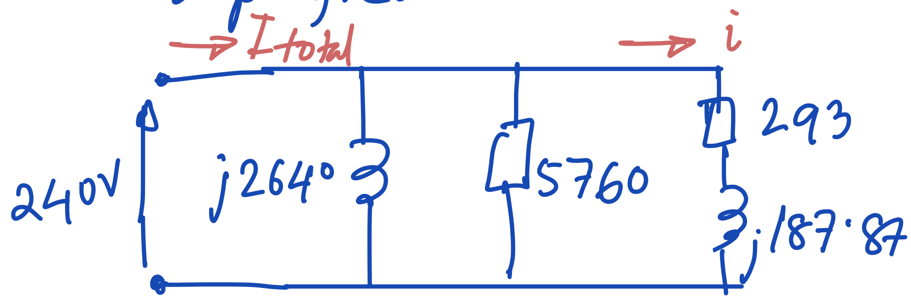
$$Q = 87.75 \text{ VAR}$$

$$X_t = \frac{87.75}{2} = 43.87\,\Omega$$

When the load is connected & referred to the high voltage side.



Simplified:



$$i = \frac{240}{348\angle 32{\cdot}67} = 0{\cdot}69\angle -32{\cdot}67^\circ \text{ Amp.}$$

For load & series components

$$P = V i \cos\phi = 240 \times 0{\cdot}69 \times \cos(32{\cdot}67^\circ) = 139{\cdot}4 \text{ W}$$

$$Q = V i \cos\phi = 240 \times 0{\cdot}69 \times \sin(32{\cdot}67^\circ) = 89{\cdot}39 \text{ VAR}$$

$$\text{Total Power } P = \frac{(240)^2}{5760} + 139{\cdot}4 = 10 + 139{\cdot}4 = 149{\cdot}4 \text{ W}$$

$$\text{Total } Q = \frac{(240)^2}{2640} + 89{\cdot}39 = 111{\cdot}2 \text{ VAR}$$

Total current $\Rightarrow$ $(VI)^2 = P^2 + Q^2$

$$(240 \times I)^2 = (149.4)^2 + (111.2)^2$$

$$I = 0.776 \text{ Amp.}$$

Therefore, power factor $= \dfrac{P}{VI} = \dfrac{149.4}{240 \times 0.776} = 0.802$ lag.

(e) We need a capacitor to generate the total Q i.e. 111.2 VAR to change the power factor to unity.

$$\frac{V^2}{1/\omega C} = 111.2 = V^2 \omega C = (240)^2 \, 2\pi \times 50\, C$$

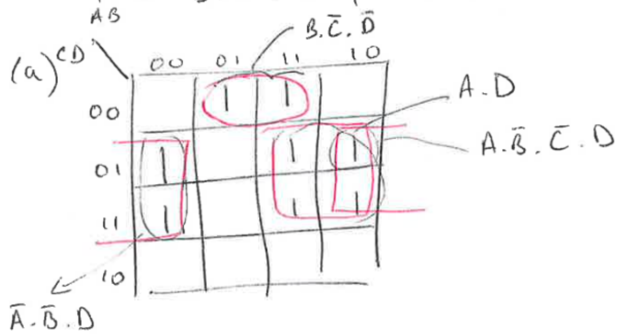
$$C = 6.14\ \mu F$$

Section B
6 **(short)**

Section B.

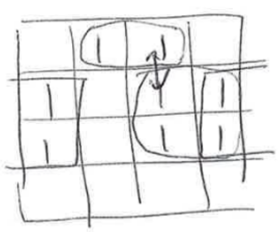
6. $F = B.\bar{C}.\bar{D} + A.D + A.\bar{B}.\bar{C}.\bar{D} + \bar{A}.\bar{B}.D$

(a)



Simplest SOP $F = B.\bar{C}.\bar{D} + A.D + \bar{B}.D$

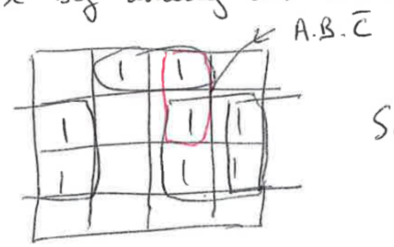
(b)



If $A = B = 1$ and $C = 0$, changing D from $0 \to 1$ or $1 \to 0$ should not have an effect according to the Boolean expression (ie F should be 1) However races in the circuit may mean that F temporarily drops to 0 before returning to 1

This is known as a static 1-hazard.

(c) Fix by adding and extra term to the SOP expression



So $F = B.\bar{C}.\bar{D} + A.D + \bar{B}.D + A.B.\bar{C}$

7 **(short)**

C	A=00	01	11	10
B=00	00001	00001	00001	00001
01	00000	00001	00011	00010
11	00000	00001	11011	01000
10	00000	00001	01001	00100

C_4	A=00	01	11	10
B=00	0	0	0	0
01	0	0	0	0
11	0	0	1	0
10	0	0	0	0

C_3	A=00	01	11	10
B=00	0	0	0	0
01	0	0	0	0
11	0	0	1	1
10	0	0	1	0

C_2	A=00	01	11	10
B=00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	1

C_1	A=00	01	11	10
B=00	0	0	0	0
01	0	0	1	1
11	0	0	1	0
10	0	0	0	0

C_0	A=00	01	11	10
B=00	1	1	1	1
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

$C_4 = A_1A_0B_1B_0,$

$C_3 = A_1A_0B_1 + A_1B_1B_0$

$C_2 = A_1\overline{A}_0B_1\overline{B}_0$

$C_1 = A_1A_0B_0 + A_1\overline{B}_1B_0$

$C_0 = A_0 + \overline{B}_1\overline{B}_0$

$$C_4 = \overline{\overline{A_1A_0B_1B_0}}$$

$$C_3 = \overline{\overline{A_1A_0B_1}\,.\,\overline{A_1B_1B_0}}$$

$$C_2 = \overline{\overline{A_1\overline{A}_0B_1\overline{B}_0}}$$

$$C_1 = \overline{\overline{A_1A_0B_0}\,.\,\overline{A_1\overline{B}_1B_0}}$$

$$C_0 = \overline{\overline{A_0}\,.\,\overline{\overline{B}_1\overline{B}_0}}$$

8 **(short)**

(a) The working register holds the data the PIC is working on at the current time (a bit like the memory on a simple calculator).
The STATUS register stores the results of the previous calculation (the carry, zero and half-carry flags) as well as power down, time out and register bank information.
The TRISIO register holds the information as to (and is used to set) which particular bits in the GPIO register are inputs and which are outputs.

main	movlw 0x31 ;	moves 0x31 into W	~1
	movwf FSR ;	moves (address) 0x31 into FSR (to set up indirect addressing	~1 ~2
	call sr ;	calls subroutine labelled sr	
	decf FSR ;	decrements FSR (now pointing to 0x30)	~1
	call sr ;	calls subroutine	~2
end	sleep ;	ends programme	~1
. . . . . .			
sr	rrf INDF ;	rotates right FSR contents (effectively ÷2)	~1
	movlw 0x10 ;	move 0x10 into W	~1
	addwf INDF ;	add 10 to contents of FSR (i.e. $\frac{\text{original no.}}{2}$ + 16 (decimal))	~1
	return ;	return to main programme	~2

(i) contents of 0x30 $= \frac{20}{2} + 16 = 26$ (0x1A)
" " 0x31 $= \frac{50}{2} + 16 = 41$ (0x29)
" " W = 16 (0x10) as last time it is changed is in the 2nd call of the subroutine

(ii) main programme 8 cycles
subroutine 5 cycles.
subroutine called twice
$\Rightarrow$ total run time $= 8 + (2 \times 5)$ cycles
$= 18 \times 50$ns
$= 0.9$ μs or 900ns.

Clock = 20MHz
$\Rightarrow$ 1 cycle = 1 period
$= \frac{1}{20 \times 10^6} = 50$ns

9 **(long)**

(a)

Sychronous : uses single clock for all sequential logic elements, circuit operates at clock speed

Asynchronous : outputs from various stage clock other stage, speed of operation depends on circuit delays

Synchronous logic is much easier to design for large circuits but is slower (uses more power) than asynchronous.

(b)

i)

Current C B A	Next C B A	J_A	K_A	J_B	K_B	J_C	K_C
0 0 0	0 0 1	0	X	0	X	1	X
0 0 1	0 1 0	0	X	1	X	X	1
0 1 0	0 1 1	0	X	X	0	1	X
0 1 1	1 0 0	1	X	X	1	X	1
1 0 0	1 0 1	X	0	0	X	1	X
1 0 1	0 0 0	X	1	0	X	X	1
1 1 0	0 0 0	X	1	X	1	0	X
1 1 1	0 0 0	X	1	X	1	X	1

J_A (B over the middle two columns, C under the right two columns)

A=0	1	1	0	1
A=1	X	X	X	X

K_A

X	X	X	X
1	1	1	1

J_B

0	X	X	0
1	X	X	0

K_B

X	0	1	X
X	1	1	X

J_C

0	0	X	X
0	1	X	X

K_C

X	X	1	0
X	X	1	1

For NOR map 0's

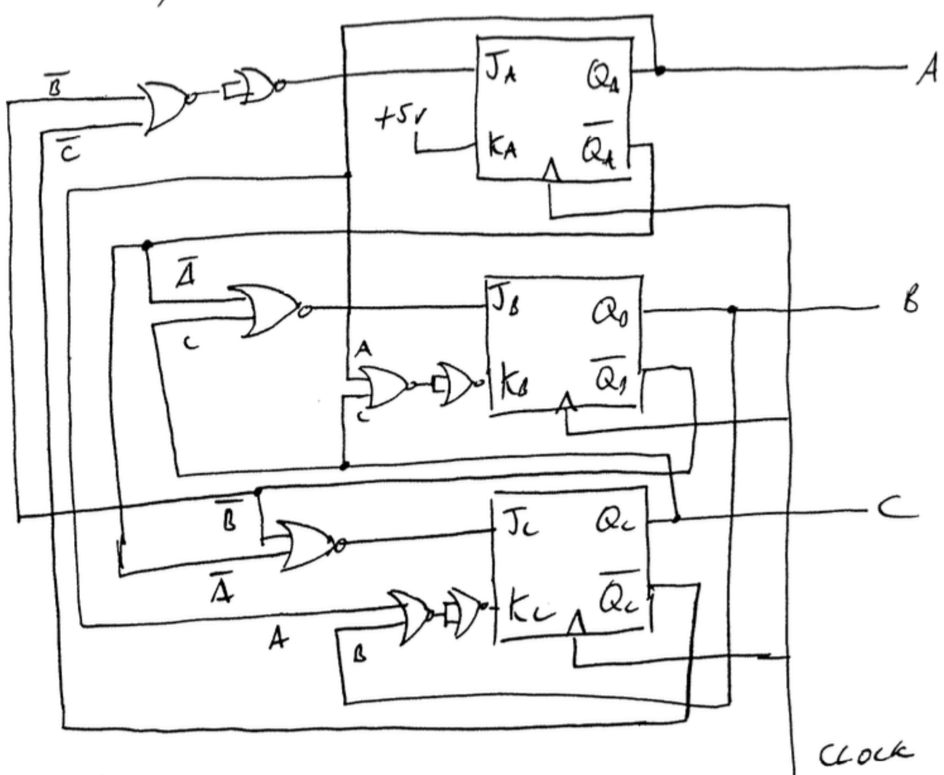
$\overline{J_A} = BC \Rightarrow J_A = \overline{\overline{\overline{B}+\overline{C}}}$ $K_A = 1$

$\overline{J_B} = \overline{A}+C$ $J_B = \overline{\overline{A}+C}$ $\overline{K_B} = \overline{A}.\overline{C}$ $K_B = \overline{\overline{A+C}}$

$\overline{J_C} = \overline{A}+\overline{B}$ $J_C = \overline{\overline{A}+\overline{B}}$ $\overline{K_C} = \overline{A}.\overline{B}$ $K_C = \overline{\overline{A+B}}$

Assuming $\overline{A}, \overline{B}, \overline{C}$ available $\Rightarrow$ 5 NORs + 2 inverters (2 NOR)

iii) Circuit



iv) MAP 1's from K-MAP.

$J_A = \overline{B}+\overline{C}$, $K_A = 1$

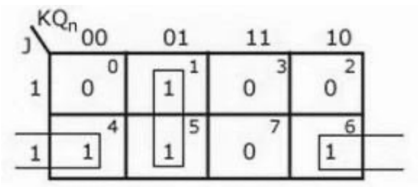
$J_B = A\overline{C}$, $K_B = A+C$

$J_C = A.B$ $K_C = A+B$

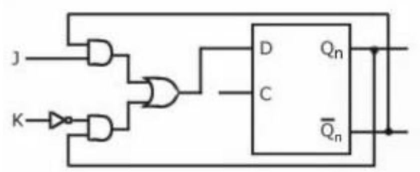
2 AND, 3 OR (5 total) vs 7 NOR

(c) In case of conversion of D flip flop to JK flip flop we have to use J and K as the external inputs and D as the input of actual flip flop. J,K and Qn makes eight possible combinations. Express D in terms of J, K and Qn.The conversion table, K-Maps and logic diagram for the conversion of D flip flop into JK flip flop is shown below:

J-K Input		Outputs		D Input
J	K	Q_n	Q_{n+1}	
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0



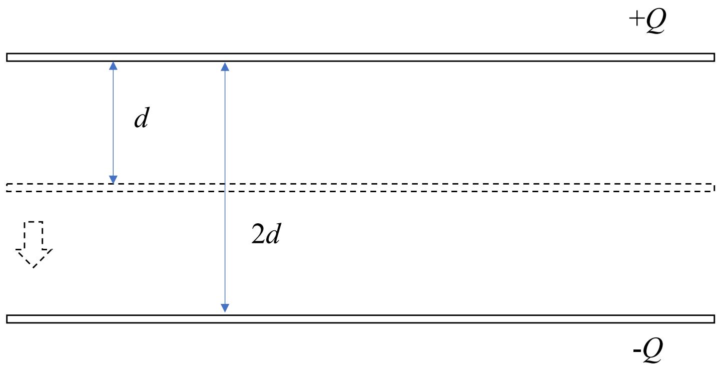
$$D = J\overline{Q}_n + \overline{K}Q_n$$



SECTION C

10 **(short)**

(a) The stored electrostatic energy is doubled.



Stored electrostatic energy is given as:

$$W = \frac{1}{2}\frac{Q^2}{C}$$

$$C = \varepsilon_0 \frac{A}{d}$$

$$W = \frac{1}{2}\frac{dQ^2}{\varepsilon_0 A}$$

$$\Delta W = \frac{1}{2}\frac{2dQ^2}{\varepsilon_0 A} - \frac{1}{2}\frac{dQ^2}{\varepsilon_0 A} = \frac{1}{2}\frac{dQ^2}{\varepsilon_0 A}$$

(b)

$$F = \frac{1}{2}V^2\frac{\partial C}{\partial x}$$

$$F = \frac{1}{2}(\frac{Q}{C})^2\frac{\partial C}{\partial d}$$

$$F = -\frac{Q^2}{2\varepsilon_0 A}$$

11 **(short)** The current flowing in the core wire will be distributed on its outer surface and thus no current inside the wire. The current flowing in the coaxial cylinder will be distributed on its inner surface.

For $0 \leq r < R_1$,

According to Ampere's law,

I=0, thus B=0;

For $R_1 \leq r < R_2$,

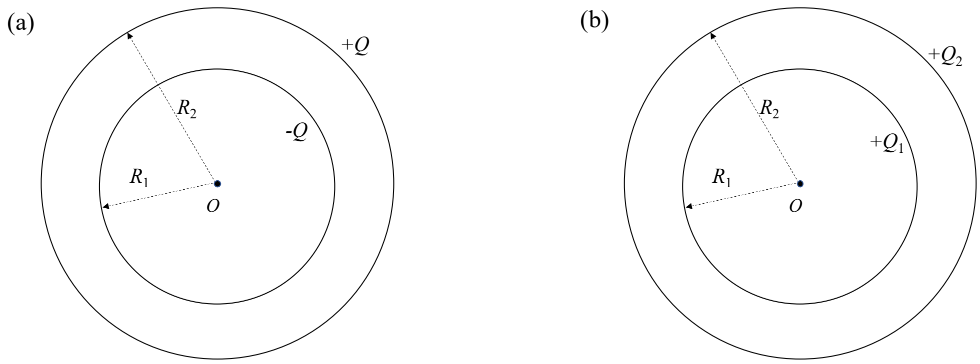
According to Ampere's law,

$$B = \frac{\mu_0 \mu_r I}{2\pi r};$$

For $R_2 \leq r \leq R_3$,

Again, total I=0, thus B=0

12 **(long)**



(a) According to Guess's law,

Electric filed:

$$E = \frac{Q}{4\pi\varepsilon_0 R^2}$$

When $R_2 \leq r$,

Total charge equals to 0, and thus E =0, and V = 0.

When $R_1 \leq r < R_2$,

Total charge equals to -*Q*, and thus:

$$E = \frac{-Q}{4\pi\varepsilon_0 r^2}$$

When $r < R_1$,

Total charge equals to 0, and thus E =0, and V = 0.

Thus, electric potential at R_2 with respect to earth is:

$$V = \int_{R_2}^{\infty} E\,dx = 0$$

(b) Electric potential at R_1 with respect to earth is:

$$V = \int_{R_2}^{\infty} E_1\, dx + \int_{R_1}^{R_2} E_2\, dx$$

$$V = \int_{R_1}^{R_2} \frac{-Q}{4\pi\varepsilon_0 r^2} dr$$

$$V = \frac{Q(R_1 - R_2)}{4\pi\varepsilon_0 R_1 R_2}$$

(c) When $R_2 \leq r$,

Total charge equals to Q_1+Q_2,

$$E = \frac{(Q_1 + Q_2)}{4\pi\varepsilon_0 r^2}$$

When $R_1 \leq r < R_2$,

Total charge equals to Q_1, and thus:

$$E = \frac{Q_1}{4\pi\varepsilon_0 r^2}$$

When $r < R_1$,

Total charge equals to 0, and thus E =0, and V = 0.

Thus, electric potential at R_2 with respect to earth is:

$$V = \int_{R_2}^{\infty} E\, dx = \int_{R_2}^{\infty} \frac{(Q_1 + Q_2)}{4\pi\varepsilon_0 r^2} dr$$

$$V = \frac{(Q_1 + Q_2)}{4\pi\varepsilon_0 R_2}$$

Also, electric potential at R_1 with respect to earth is:

$$V = \int_{R_2}^{\infty} E_1\, dx + \int_{R_1}^{R_2} E_2\, dx$$

$$V = \int_{R_2}^{\infty} \frac{(Q_1 + Q_2)}{4\pi\varepsilon_0 r^2} dr + \int_{R_1}^{R_2} \frac{Q_1}{4\pi\varepsilon_0 r^2} dr$$

$$V = \frac{(Q_1 + Q_2)}{4\pi\varepsilon_0 R_2} + \frac{Q_1(R_2 - R_1)}{4\pi\varepsilon_0 R_1 R_2}$$
$$= \frac{Q_1 R_2 + Q_2 R_1}{4\pi\varepsilon_0 R_1 R_2}$$