Version OBA/2

EGT0
ENGINEERING TRIPOS PART IA

Monday 10 June 2024 9.00 to 12.10

Paper 3

ELECTRICAL & INFORMATION ENGINEERING

*Answer **all** questions.*

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

*Write your candidate number **not** your name on the cover sheet.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS TO BE SUPPLIED FOR THIS EXAM

CUED approved calculator allowed
Engineering Data Book

10 minutes reading time is allowed for this paper at the start of the exam.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed to do so.

You may not remove any stationery from the Examination Room.

Section A

1 (**short**) Using Thevenin's and/or Norton's theorem, simplify the circuit in Fig. 1 and derive the expression for current in the resistor **R**. [10]

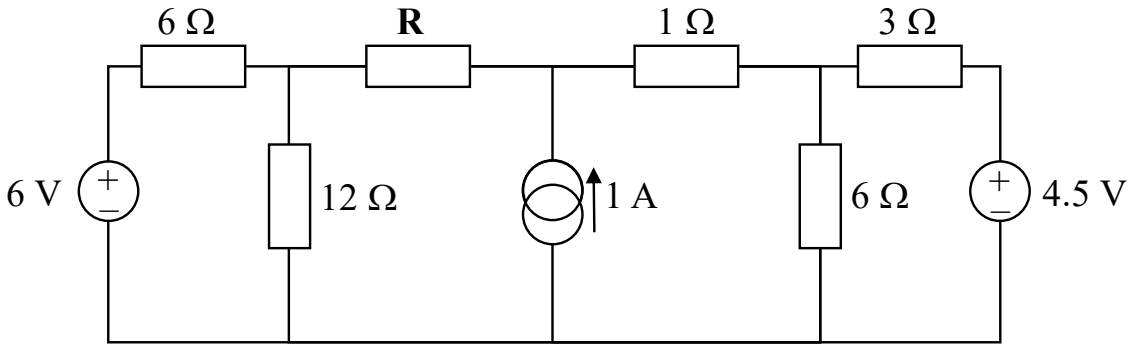

Fig. 1

2 (**short**) Calculate the total complex impedance of the circuit shown in Fig. 2. Find the magnitude and phase of the supply current ***i***. [10]

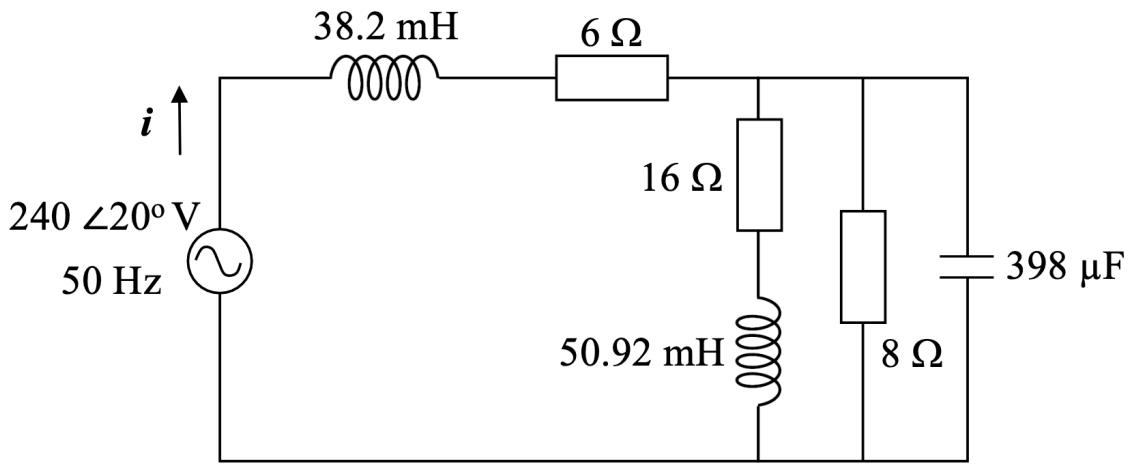

Fig. 2

3 (**short**)

(a) Derive an expression for the output voltage v_{out} in the circuit shown in Fig 3. The operational amplifier is ideal. [3]

(b) Consider two signal sources $v1$ and $v2$ with negligible output resistance. Design a circuit with two ideal operational amplifiers to produce a circuit output of $(200\,v1 - 50\,v2)$. You may decide the values of the resistances in your design. Justify your choice of resistance values. [7]

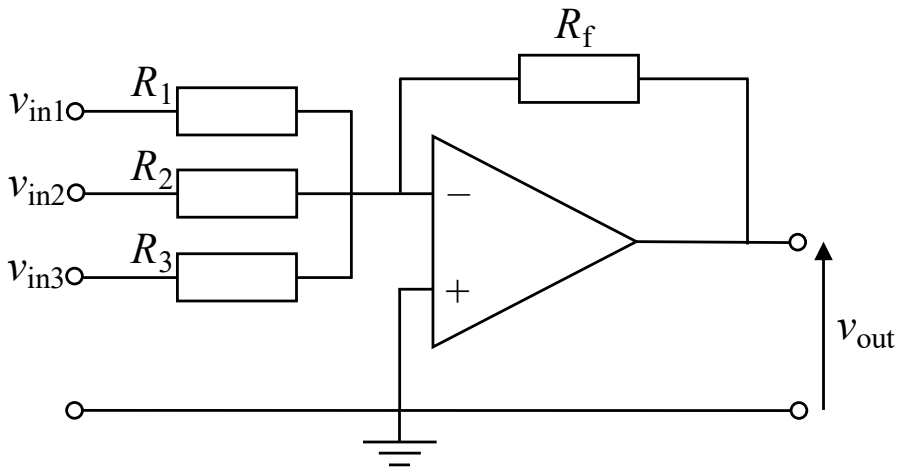

Fig. 3

4 (**long**)

(a) Draw the small signal model for the circuit shown in Fig. 4 and derive the expressions for:

(i) Input impedance

(ii) No-load gain

(iii) Output impedance

Determine the values of the above circuit parameters if $g_m = 5$ mS, $r_d = 20$ kΩ, $R_1 = 10$MΩ and $R_2 = 20$ kΩ. [16]

(b) What is the function of this circuit? Suggest an application and briefly explain why this circuit would be useful. [6]

(c) If the circuit drives an inductive load of 25 mH, calculate the frequency at which the load current drops to 70% of its mid-band value. [8]

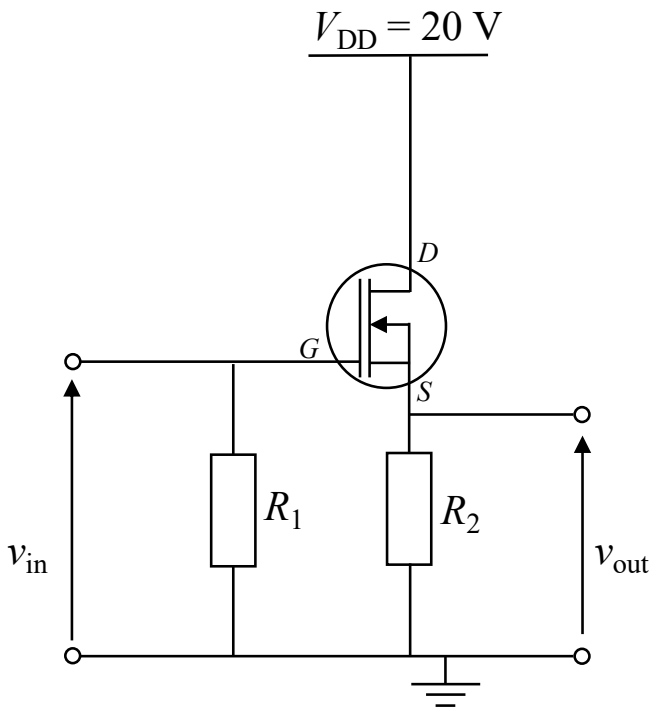

Fig. 4

5 (**long**) A 240 V, 50 Hz transformer is used to drive a load of $(8+j4)\ \Omega$ with 40 V rms.

(a) Assuming the transformer is ideal, calculate the turns ratio of the windings and the impedance of the load when referred across to the high voltage (primary) side. [2]

(b) Briefly explain the physical significance of each of the elements of a non-ideal transformer equivalent circuit. You may use the simplified equivalent circuit shown in the Electrical Engineering Data Book, in which R_0 and X_0 are shown connected directly to the primary input voltage supply. [4]

(c) The transformer is open circuit tested and short circuit tested to measure its characteristics. The following test results are obtained:

(i) Open circuit test (low voltage winding open circuit): V_{primary} = 240 V, I_{primary} = 0.1 A, P = 10 W

(ii) Short circuit test (low voltage winding short circuit): V_{primary} = 45 V, I_{primary} = 2.0 A, P = 20 W

Determine the values of the equivalent circuit elements (referred to the primary, high voltage side) of the transformer. [14]

(d) What is the power factor, current and power drawn from the mains when the transformer is connected to the above load? [6]

(e) A capacitor is now connected to correct the power factor to unity. Calculate the value of this capacitor. [4]

Section B

6 (**short**) A four variable Boolean function is defined as

$$F = AD + B\bar{C}\bar{D} + \bar{A}\bar{B}D + A\bar{B}\bar{C}D.$$

Using a Karnaugh map, or otherwise:

(a) Find the simplest Sum of Products expression for F. [4]

(b) Identify under what circumstances a change to a single input variable may cause a momentary unexpected change in F. Give the technical term for this problem. [3]

(c) Modify the Sum of Products expression found in part (a) to remove this possible problem. [3]

7 (**short**) A logic circuit has four inputs and five outputs. The four inputs A_1, A_0 and B_1, B_0 represent two 2-bit unsigned binary numbers. The five bits of the output C, i.e., C_4, C_3, C_2, C_1, and C_0, are the result of the number A being raised to the power B. Derive the expressions for the output C of a calculator circuit to be implemented using NAND and inverter gates only. Note: $A^0 = 1$ for all values of A. [10]

8 (**short**)

(a) Explain the functions of STATUS Register, Working Register (W) and TRISIO Register in PIC12F675 microcontroller. [3]

(b) Before the following PIC assembly code is executed, the contents of memory locations 0x30 and 0x31 are the decimal numbers 20 and 50, respectively.

```
main
        movlw 0x31;
        movwf FSR;
        call sr;
        decf FSR, f;
        call sr;
end     sleep;
...
sr      rrf INDF, f;
        movlw 0x10;
        addwf INDF, f;
        return;
```

(i) What are the contents of Working Register (W) and the memory locations of 0x30 and 0x31 after the code has executed? [4]

(ii) Determine the time taken to execute the code assuming a 20 MHz operational clock. [3]

9 (**long**)

(a) What is the difference between asynchronous and synchronous sequential circuits, and give one advantage and disadvantage of each. [2]

(b) A modulo-6 synchronous binary counter is to be designed using only J-K bistables and 2-input NOR gates. If an unused state occurs, the counter returns to the state 0 on the next clock pulse.

(i) Draw a state table for the counter. [5]

(ii) Find the required J-K logic inputs for each bistable. [5]

(iii) Draw the complete circuit. [5]

(iv) If other 2-input gates were also available, show how the design could be changed to use a smaller total number of gates, and list the gates used. [3]

(c) Implement a J-K bistable with a D bistable and a minimum number of AND, OR and inverter gates. Draw the circuit to show your implementation. [10]

Section C

10 (**short**) A capacitor is formed by two parallel plates that are spaced by a distance d, and each carries a charge of $+Q$ and $-Q$, respectively. Both plates have an area of A. Now the distance between the two plates is enlarged from d to $2d$, as shown in Fig. 5.

(a) What is the change of the stored electrostatic energy? [5]

(b) What is the initial force used to enlarge the separation of the two plates at distance d? [5]

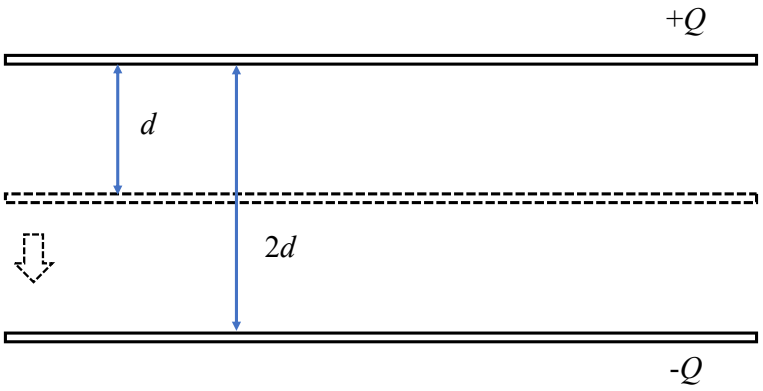

Fig. 5

11 (**short**) A coaxial cable is shown in Fig. 6 that has a core conducting wire with a radius of R_1, and a coaxial cylinder with inner and outer radii of R_2 and R_3, respectively. The gap is filled with an insulator material that has relative permeability μ_r. Current, I, is flowing bottom up in the core wire and flowing top down in the coaxial cylinder, as indicated by Fig. 6. Draw the magnetic flux density profile in the whole coaxial cable as a function of radius (r), i.e., $0 \leq r \leq R_3$. [10]

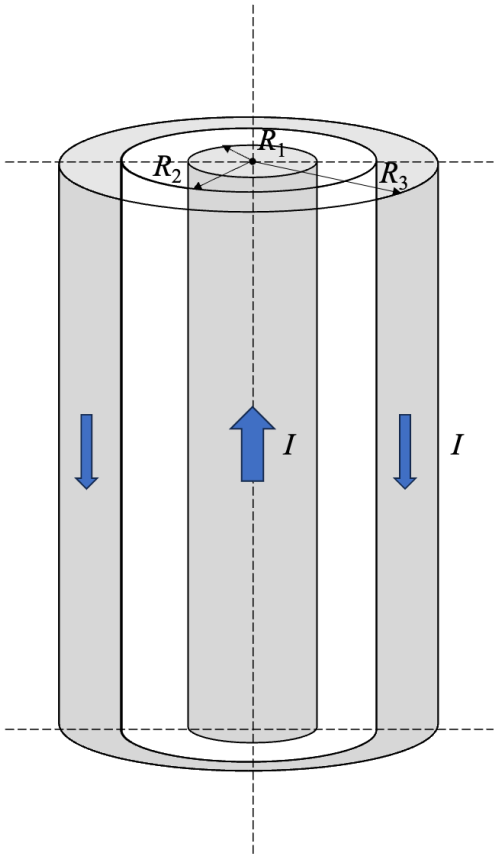

Fig. 6

12 (**long**) Two concentric spherical surfaces have radii of R_1 and R_2, and each uniformly carries a charge of $-Q$ and $+Q$, as shown in Fig. 7(a), respectively.

(a) What is the electric potential at R_2 with respect to Earth? [7]

(b) What is the electric potential at R_1 with respect to Earth? [8]

(c) The two concentric spherical surfaces now uniformly carry a charge of $+Q_1$ and $+Q_2$ as shown in Fig. 7(b). What is the electric potential at R_2 and R_1 with respect to Earth? [15]

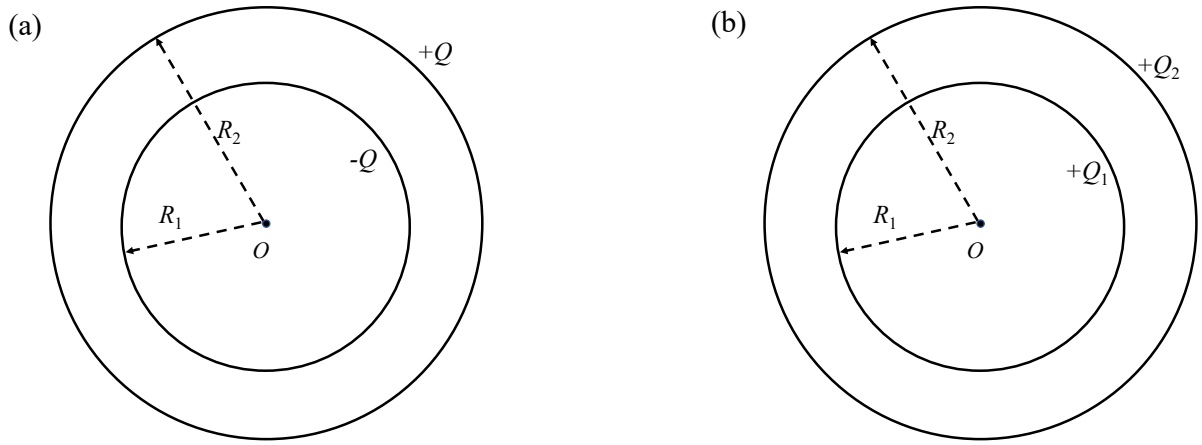

Fig. 7

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