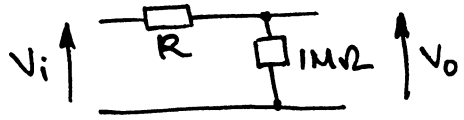
PART 1A PAPER 3 1996 SECTION A

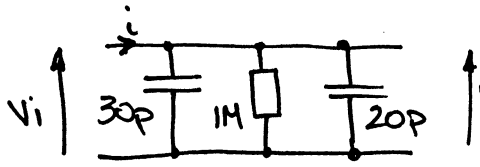
1 a) Potential divider circuit, ignoring capacitors :-



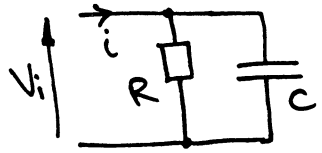
$$V_o = \frac{1M\Omega}{R + 1M\Omega} \cdot V_i = \frac{V_i}{10}$$

$$\therefore R = 9M\Omega$$

b)



$\equiv$



$R = 1M\Omega$
$C = 50pF$
(parallel capacitors add in value)

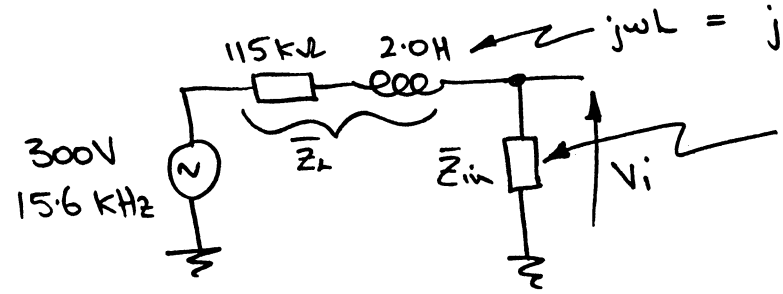
$$\bar{Z}_{in} = \frac{V_i}{i} = R \,/\!/\, C \quad (\text{parallel}) = \frac{1}{\frac{1}{R} + \frac{1}{1/j\omega C}} = \frac{R}{1 + j\omega CR}$$

$$\therefore \bar{Z}_{in} = \frac{R}{1+j\omega CR} \frac{(1-j\omega CR)}{(1-j\omega CR)} = \frac{R - j\omega CR^2}{1 + \omega^2 C^2 R^2}$$

Substituting for $R = 10^6\,\Omega$, $C = 50 \times 10^{-12}$ F, $\omega = 2\pi f$ rad/s

$$\bar{Z}_{in} = \frac{10^6 - j100\pi f}{1 + 10^{-8}\pi^2 f^2} \quad @\ f\ \text{Hz}.$$

c)



$\bar{Z}_{in}$ @ 15.6 kHz using expression above

$= 39.97 \times 10^3 - j\,195.88 \times 10^3\ \Omega$

$= 199.92 \times 10^3 \angle -78.5°$

Consider this as a potential divider circuit,

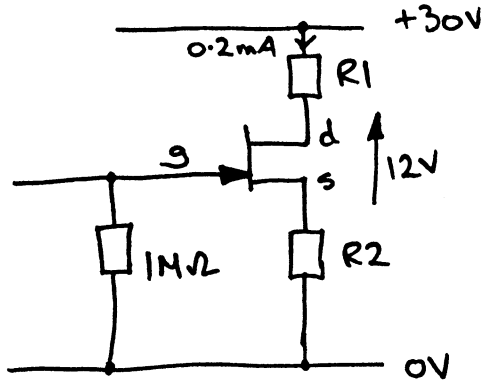
$$V_i = \frac{\bar{Z}_{in}}{\bar{Z}_L + \bar{Z}_{in}} \cdot 300\ \text{V} = \frac{199.92 \times 10^3 \angle -78.5 \cdot 300}{(115\times10^3 + 39.97\times10^3 + j196.04\times10^3 - j195.88\times10^3)}$$

$$= \frac{300 \cdot 199.92 \times 10^3 \angle -78.5}{154.97 \times 10^3 + \cancel{j60}\ \text{ignore as small}} = 387 \angle -78.5°$$

Note: the output voltage is higher than the input due to resonance effects.

Part IA 1996 (electrical)

2 a)



DC OPERATING POINT :-

$V_g = 0$ due to 1MΩ resistor.

So for $V_{gs} = -2V$, V_s must be 2V

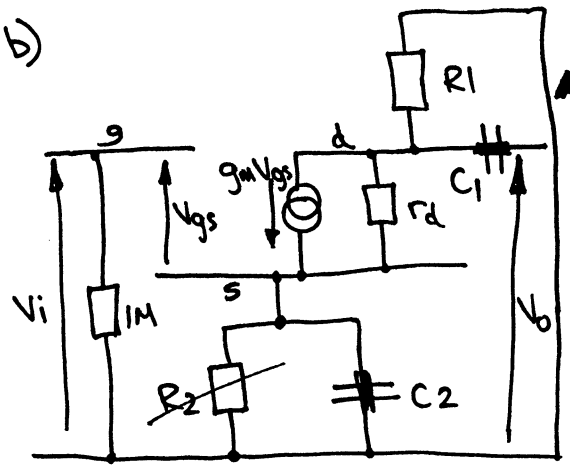
∴ R2 has 2V across it with 0·2mA flowing through it

$$\Rightarrow R_2 = \frac{2}{0.2\times10^{-3}} = \underline{\underline{10\,k\Omega}}$$

So, voltage across R1 = $30 - (12+2) = 16V$ for 0·2mA

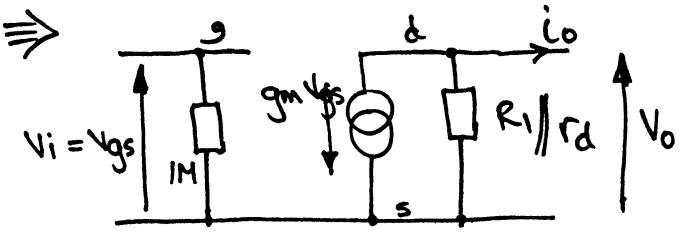
$$\therefore R_1 = \frac{16}{0.2\times10^{-3}} = \underline{\underline{80\,k\Omega}}$$

b)



supply is short circuit to signal frequencies

∴ re-arrange to give this,



capacitors considered short circuit at signal frequencies (∴ C2 shorts R_2)

c)

Small signal gain = $V_o/V_i = V_o/V_{gs}$

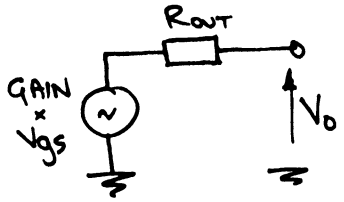
Sum currents at drain node :- $g_m V_{gs} + \frac{V_o}{\frac{R_1 . r_d}{R_1 + r_d}} + i_o = 0$

$$\therefore V_o = (-g_m V_{gs} - i_o)\frac{R_1 . r_d}{R_1 + r_d}$$

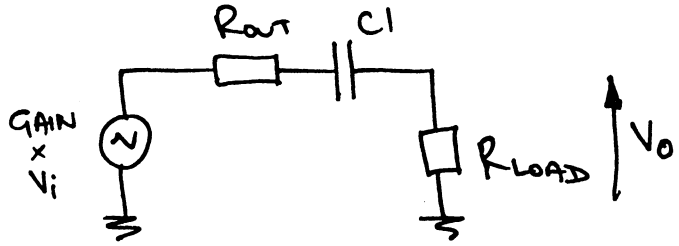
Expressed as V_o = GAIN × V_{gs} − R_{OUT} × i_o we get,

$$\text{GAIN} = \frac{-g_m . R_1 . r_d}{R_1 + r_d} = \underline{\underline{-44.4}}$$

$$R_{OUT} = \frac{R_1 . r_d}{R_1 + r_d} = \underline{\underline{44.4\,k\Omega}}$$



2 d)



[see Electrical Data Book section on coupling between stages]

$$V_o = \frac{R_{LOAD} \cdot GAIN \times V_i}{R_{LOAD} + R_{OUT} + \frac{1}{j\omega C_1}}$$

(potential divider arrangement)

This drops to -3dB or $1/\sqrt{2}$ of mid-band value when the real and imag. parts of denominator are equal in magnitude

ie: $R_{LOAD} + R_{OUT} = \frac{1}{\omega C_1}$, $\omega = 30\pi$ rad/s $(= 2\pi f)$

$$\therefore C_1 = \frac{1}{30\pi \cdot 54.4 \times 10^3} = \underline{\underline{195\ nF}}$$

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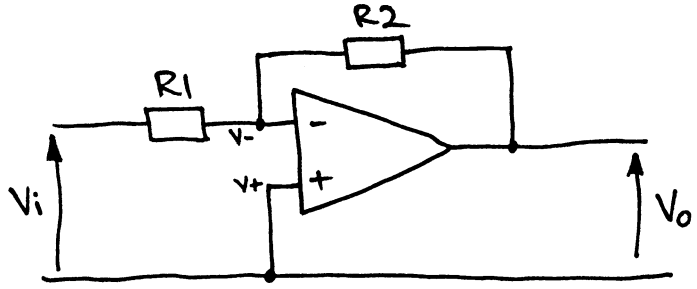
3 a) 40 dB = Voltage gain of $10^{\frac{40}{20}} = \times 100$



standard inverting op-amp circuit. $V_- \approx 0$ comprising a 'virtual earth'. Ignore capacitor for mid-band gain.

$V_+ = V_- = 0$

Sum currents at - node :-

$$\frac{V_i - 0}{R_1} = \frac{0 - V_o}{R_2} \quad \therefore \frac{V_o}{V_i} = GAIN = -\frac{R_2}{R_1} = -100$$

$$\therefore R_2 = \underline{\underline{1M\Omega}} \text{ with } R_1 = 10k\Omega$$

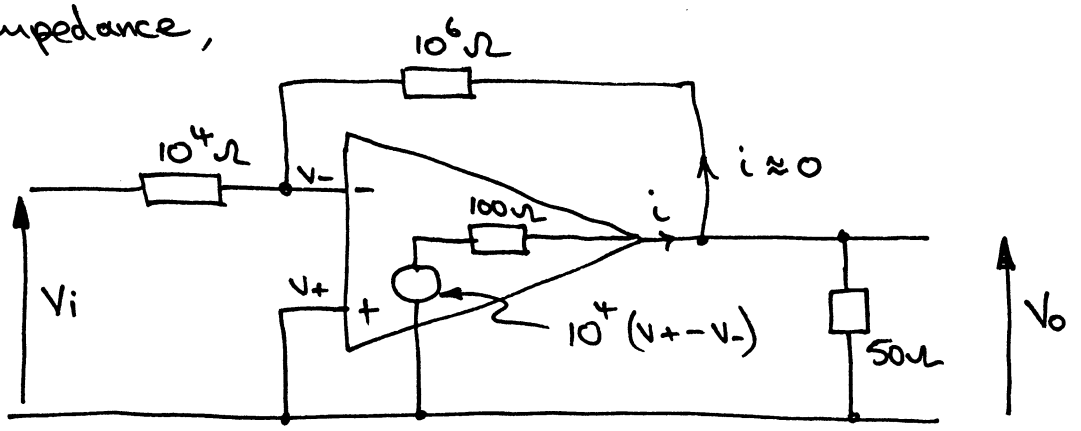
b) The 'virtual earth' at the - node means that the input impedance is just R1 = $\underline{\underline{10k\Omega}}$

3 c) Considering the effect of C1 on the gain,

$$\text{GAIN} = \frac{-R_2 /\!/ C_1}{R_1} = \frac{\frac{-1}{\frac{1}{R_2} + j\omega C_1}}{R_1} = \frac{-R_2/R_1}{(1 + j\omega C_1 R_2)}$$

this drops to $1/\sqrt{2}$ of its mid-band value ie: -3dB when $\omega C_1 R_2 = 1$ $\therefore$ if $\omega_{-3dB} = 2\pi . 5\times10^3$ and $R_2 = 10^6\,\Omega$ then $C_1 = \frac{1}{\pi \times 10^4 . 10^6} = \underline{\underline{31.8\,pF}}$

d) Consider effects of finite open-loop gain and output impedance,



Sum currents @ V- node: $\frac{V_i - V_-}{10^4} = \frac{V_- - V_o}{10^6}$ ——(1)

Sum currents @ output: $\frac{V_o}{50} \approx i \approx \frac{10^4(V_+ - V_-) - V_o}{100}$

Also, $V_+ = 0$ $\therefore V_o = \frac{-10^4}{2} V_- - \frac{V_o}{2} \Rightarrow V_o = \frac{-10^4}{3} V_-$

Substituting into (1): $\frac{V_i - \frac{-3}{10^4} V_o}{10^4} = \frac{\frac{-3}{10^4} V_o - V_o}{10^6 \, 100}$

$\therefore 100 V_i + \frac{3}{100} V_o = \left(\frac{-3}{10^4} - 1\right) V_o$

$\Rightarrow V_o = \frac{-100 V_i}{(1 + \frac{3}{100} + \frac{3}{10^4})} = -97.06 V_i$

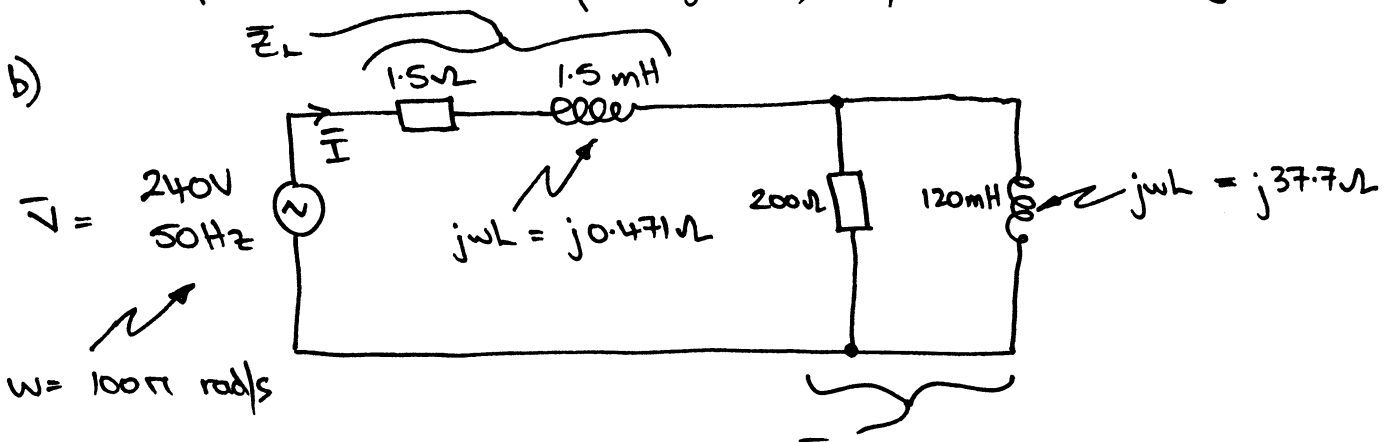
So gain in dB = $20 \log_{10}(97.06) = \underline{\underline{39.7\,dB}}$

(cf. 40dB in ideal case)

Part IA 1996 (electrical)

4 a)
- Watts = $VI\cos\phi$ produce useful work, heat, light etc.
- Vars = $VI\sin\phi$ represent energy stored and released in capacitors and inductors during the ac cycle and produce no useful work.
- Vars increase the line current for a given amount of power (Watts) supplied, hence I^2R losses in the lines are higher – electricity supplies charge for this.
- Vars can be reduced to zero by matching inductive and capacitive loads ⇒ power factor, $\cos\phi$ correction to unity.

b)



$$\bar{Z}_m = \frac{200 \cdot j37.7}{200 + j37.7}$$

$$\bar{Z}_m = R'_m + jX'_m = 6.88 + j36.41\ \Omega$$

(equivalent series R & jωL for motor)

current,

$$\bar{I} = \frac{\bar{V}}{\bar{Z}_L + \bar{Z}_m} = \frac{240}{1.5 + 6.88 + j(0.471 + 36.41)} = \frac{240}{8.38 + j36.88}$$

$$= \underline{6.34\ \angle -77.2^\circ}\ \text{A}$$

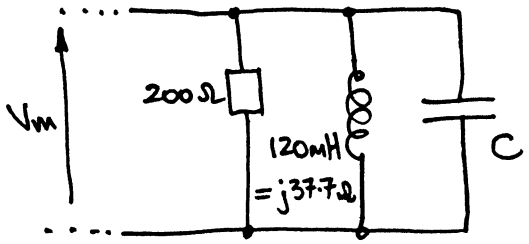
Power factor = $\cos\phi = \cos 77.2^\circ = \underline{0.22\ \text{lag}}$

c) Motor power = $I^2 R'_m = 6.34^2 \cdot 6.88 = \underline{276\text{W}}$

Motor vars = $I^2 X'_m = 6.34^2 \cdot 36.41 = 1464$ vars

Cable power loss = $I^2 R_c = 6.34^2 \cdot 1.5 = \underline{60.3\text{W}}$

4 d) To correct power factor to unity, we need to shunt the motor with a capacitor producing equal but opposite VARs to the motor inductance.



$$\text{Motor VARs} = 1464 = \frac{V_m^2}{37.7}$$

$$\text{Capacitor VARs} = \frac{-V_m^2}{\frac{1}{\omega C}} = -\omega C V_m^2$$

$$\therefore \quad 1464 \cdot 37.7 = V_m^2$$

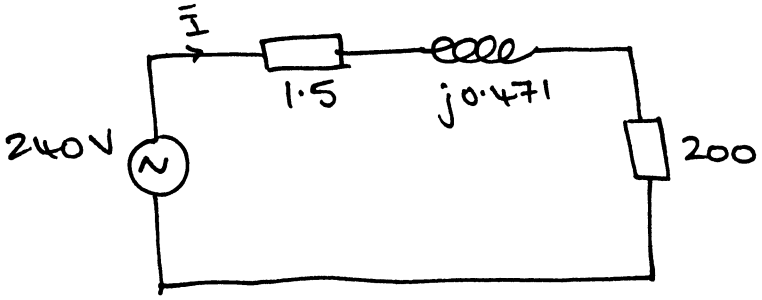
and for C to give -1464 VARs,

$$\cancel{-}1464 = \cancel{-} 2\pi \cdot 50\, C \quad \cancel{1464} \cdot 37.7$$

$$\therefore C = \frac{1}{100\pi \; 37.7} = \underline{\underline{84.4\ \mu F}}$$

The motor L and C are effectively parallel resonant, leaving only the 200Ω resistor.

Circuit now becomes :-



$$\bar{I} = \frac{240}{201.5 + j0.471} = \frac{240}{201.5 \angle 0.13^\circ} = 1.19 \angle -0.13^\circ$$

$$\therefore \text{ New cable loss} = I^2 R = 1.19^2 \cdot 1.5 = 2.13\text{W}$$

& cable (the only ones) vars $= I^2 X = 1.19^2 \cdot 0.471 = \underline{\underline{0.67 \text{ Vars}}}$

Part Ia 1996 (electrical)

5. $Y = AC\overline{D} + \overline{A}B(CD + BC)$

Convert to sum-of-products form and construct the K-map:-

$$Y = AC\overline{D} + \overline{A}BCD + \overline{A}BC$$

CD / AB	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	0	0	1
10	0	0	0	1

To simplify, encircle largest rectangular groups of 1s.

$$Y = AC\overline{D} + \overline{A}BC \qquad (1)$$

Note that this is not hazard-free. To make it so, the additional term $BC\overline{D}$ (shown encircled in dashed line) must be ORed in to the expression. The expression (1) can be rewritten:-

$$Y = \overline{\overline{AC\overline{D}} + \overline{\overline{A}BC}} = \overline{\overline{AC\overline{D}}.\overline{\overline{A}BC}}$$

which can be implemented using three-input NAND gates and inverters as follows:- Fig (i) below

The hazard-free implementation thus requires one additional three-input NAND gate.

To implement the expression for Y using NOR gates, first determine the expression for $\overline{Y}$ by inspection of the K-map:-

$$\overline{Y} = \overline{C} + \overline{A}.\overline{B} + A.D \qquad (2)$$

Hence $$Y = \overline{\overline{C} + \overline{A}.\overline{B} + A.D}$$

By de Morgan:-

$$Y = \overline{\overline{C} + (\overline{A + B}) + (\overline{\overline{A} + \overline{D}})}$$

which can be implemented using two/three input NOR gates and inverters as follows:- Fig (ii) below

Note that the original expression for Y (1) can also be transformed using de Morgan to give:

$$\overline{Y} = \overline{\overline{A + \overline{B} + \overline{C} + \overline{A} + \overline{C} + D}}$$

This also requires three NOR gates, three inverters to invert the signals A, B and C, *plus* one further inverter to generate Y from $\overline{Y}$.

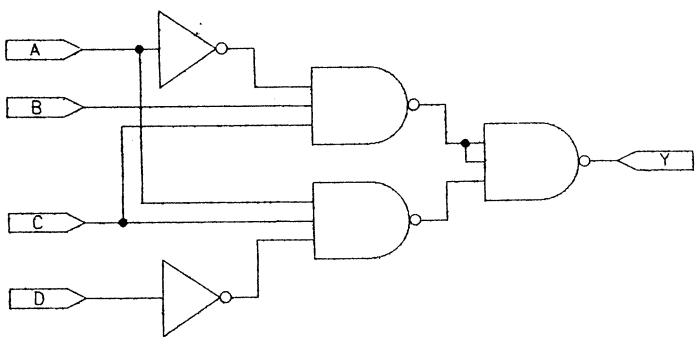


Fig (i)

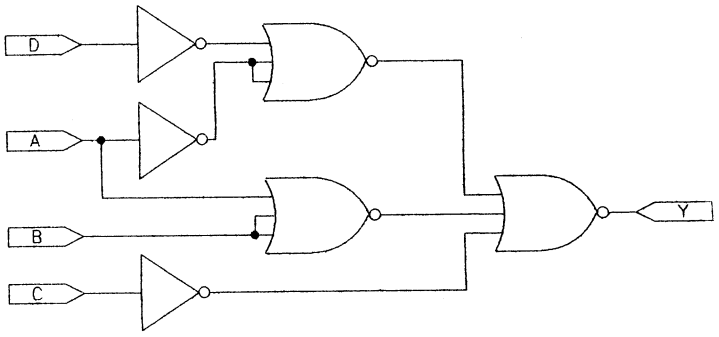


Fig (ii)

6. An unused state in a sequential logic system is a possible combination of states of the bistable outputs which is not actually required. Unused states may lead to simplification of the design if they may be regarded in the same way as 'don't care' states; however, in critical designs it may be important to define the behaviour of the system if it should enter an unused state (for example, at power-on or because of electrical noise).

In this instance the unused states are 000, 011, 100, 110.

The *next* state of Q_A, Q_B, and Q_C is clearly determined by their *present* state, but also by the state of M. The state transition table shows the permitted transitions. Unused states are assumed not to occur. The required values of J_A - K_C are determined by referring to the J-K excitation table in the Data Book.

	Current state			Next state			Required J & K values					
M	Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	1	0	1	1	X	X	1	1	X
0	1	0	1	1	1	1	X	0	1	X	X	0
0	1	1	1	0	0	1	X	1	X	1	X	0
1	0	0	1	1	1	1	1	X	1	X	X	0
1	1	1	1	1	0	1	X	0	X	1	X	0
1	1	0	1	0	1	0	X	1	1	X	X	1
1	0	1	0	0	0	1	0	X	X	1	1	X

J_A and K_A

Q_AQ_B / Q_CM	00	01	11	10
00	U	1	U	U
01	U	0	U	U
11	1	U	X	X
10	0	U	X	X

Hence $J_A = \overline{Q}_C\overline{M} + Q_CM$

Q_AQ_B / Q_CM	00	01	11	10
00	U	X	U	U
01	U	X	U	U
11	X	U	0	1
10	X	U	1	0

$K_A = Q_B\overline{M} + \overline{Q}_BM$

By inspection, $J_B = 1$

$K_B = 1$

J_C and K_C

Q_AQ_B / Q_CM	00	01	11	10
00	U	1	U	U
01	U	1	U	U
11	X	U	X	X
10	X	U	X	X

Hence $J_C = 1$

Q_AQ_B / Q_CM	00	01	11	10
00	U	X	U	U
01	U	X	U	U
11	0	U	0	1
10	1	U	0	0

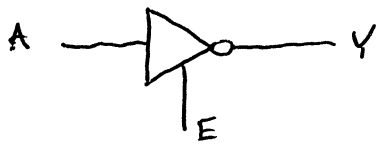
$K_C = Q_A\overline{Q}_BM + \overline{Q}_A\overline{M}$

There are alternative ways of drawing the loops which will give different expressions for the J and K inputs.

The counter may possibly enter an unused state at the moment of applying power (when the state reached by each bistable may be uncertain), or if electrical noise is introduced. To determine what will happen should the counter enter an unused state, it is necessary to complete the state transition table so it incorporates all unused states (for both values of M). The equations derived above are used to determine all three J/K inputs in terms of the corresponding Q values. From this can be deduced the next state the counter will enter.

Part Ia 1996 (electrical)

7(a) Tri-state logic has a third output state 'Z' in addition to 0 and 1. In the Z state, the resistance of the output circuit is set to a high value. Effectively, this means that the device is no longer connected to the external circuit at its output pin. An extra 'enable' input pin allows the device to be placed either in its normal state, or the high impedance state; for example, a tri-state inverter might have the following characteristic:-



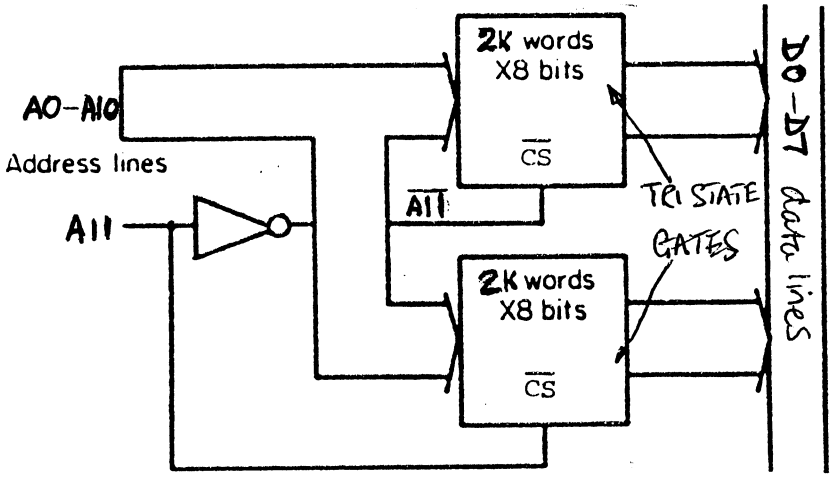
A	E	Y
0	0	Z
1	0	Z
0	1	1
1	1	0

This feature can be used in two ways:-

i) to allow two or more devices to have their output terminals connected together. Only one device is enabled at a time.

ii) to allow the same pin to serve both as an output AND an input. The output circuit is set to Z to allow data to be input via the pin. This is the principle of operation of the bidirectional bus.

Both modes of operation are used in typical microprocessor circuits. Tri-state logic is commonly used for the transmission of data via the Data Bus between microprocessor, memory devices and I/O devices.



7(b) Twos complement notation is based on the idea that *adding the twos complement of a number* is equivalent to subtracting that number. In this notation, the MS bit indicates the sign of the number: if 1, it indicates a negative number; if 0, the number is positive. To form the twos complement:-

i) form the ones complement by substituting 0 for 1, 1 for 0
ii) add 1 to the number.

The concept is important in information processing because it means computers can add and subtract binary numbers using the same hardware.

Binary numbers can be determined using one of the standard methods, e.g. by successive division by two and writing down each remainder. This gives the appropriate string of bits starting with the LS bit.

Number	Bit 7	6	5	4	3	2	1	0
51_{10}	0	0	1	1	0	0	1	1
$+126_{10}$	0	1	1	1	1	1	1	0
Ones comp	1	0	0	0	0	0	0	1
Add 1	1	0	0	0	0	0	1	0
-126_{10}	1	0	0	0	0	0	1	0
98_{10}	0	1	1	0	0	0	1	0

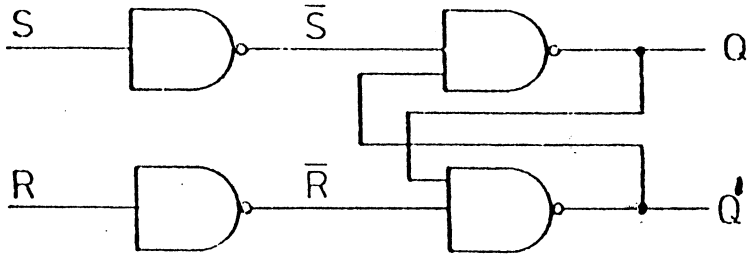
7(c) With outputs Q and Q':

$Q = \overline{\overline{S}.Q'} = S + \overline{Q'}$

$Q' = \overline{\overline{R}.Q} = R + \overline{Q}$

The outputs obey the table below:

S	R	Q	Q'
0	0	no	change
0	1	0	1
1	0	1	0
1	1	not	allowed



When S=R=1 goes to S=R=0, the circuit should (in theory) oscillate between Q=Q'=1 and Q=Q'=0. In a real circuit, one of the output gates will operate slightly faster (here we cannot predict which) than the other, and the circuit will enter one of the states in which Q' is truly complementary to Q. Hence it is not possible to predict the next state, and S=R=1 is therefore a forbidden input combination.

8. The Microprocessor Data Book lists the bits comprised in the CCR. The I (interrupt mask) bit is not described here. The effect on other bits of any instruction are listed in the Data Book under MPU instructions - for example, ADDA (arithmetic operation) affects H, N, Z, V and C; ANDA (logical operation) affects N and Z only; ROLA (logical operation) affect N, Z and C (and V).

C - Carry bit - used in arithmetic operations on signed numbers, when it represents the Carry out of Bit 7. Also required for unsigned binary addition and subtraction for numbers larger than 8 bits. Several of the Shift and Rotate instructions shift data via the Carry bit. This allows for easy testing.

V - 2s complement overflow - set to 1 whenever overflow is detected in 2s complement signed arithmetic. This is the logical XOR of the carries out of Bits 6 and 7.

Z - Zero - set 1 whenever an arithmetic operation generates a zero result.

N - Negative - set 1 when the MS bit of the result of an arithmetic or logical operation is 1.

H - Half-carry - set 1 when an arithmetic operation causes a carry to be generated out of bit 3. Used in BCD arithmetic.

The CCR also:

provides various forms of Carry and Borrow in binary multiple precision arithmetic;

provides a means by which results of comparisons, tests and subtractions are recorded (TST and CMP) before being acted on by conditional branch instructions.

```
      CLR   $40    ; Set value stored at location Hex 40 to zero
      LDX   #0     ; Load index register with immediate zero
LOOP1 LDAA  $80,X  ; Load Acc A with data value stored at
                   ; location (Hex 80 + the value in X) - indexed addressing
      LDAB  #8     ; Load Acc B with immediate 8
LOOP2 ROLA         ; Rotate Acc A to left, placing MS bit in C
      BCC   +3     ; If C is set (i.e. MS bit was 1) ..
      INC   $40    ; .. increment the value at location Hex 40
      DECB         ; Decrement the value in B
      BNE   LOOP2  ; Has inner loop been executed 8 times? If not, repeat
      INX          ; Increment the value in X
      CPX   #10    ; Compare the value in X with 10
      BNE   LOOP1  ; If it's not reached 10 repeat the outer loop
                   ; Finished
```

`LOOP1` and `LOOP2` are labels and are the objects of conditional branch instructions. Note that # signifies immediate data, while $ signifies that a hexadecimal value follows.

The inner loop executes 8 times, on each occasion progressively rotating `ACCA (ROLA)` so the MS bit passes through C. The Carry bit is tested `(BCC)` to see if it is 0 or 1. If it's 1, the value in `$40` is incremented. Hence the inner loop counts the number of bits set to 1 in `ACCA`.

The outer loop is executed (decimal) 10 times, and a new item of data is fetched in `ACCA` each time. Hence at the end of the code segment, `$40` contains the total number of 1 bits set in the ten data values. If these are 0,1, ... 9, the total will be 0+1+1+2+1+2+2+3+1+2=15.

To process 100 pieces of data, change `CPX #10` to `CPX #100`. If the data were arbitrary, 10 elements could contain a maximum of 80 bits set to 1. This will never overflow the 8 bit counter `$40`. If there are 100 data values, the 8 bit counter is liable to overflow. A 16 bit counter could be implemented by inserting extra statements after `INC $40` :-

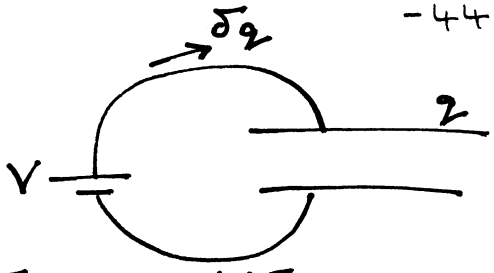
```
      BNE   +3
      INC   $41    ; High 8 bits of counter held at $41
```

Note that `$41` would have to be zeroed at the start of the code using CLR, and the `BCC +3` would have to be adjusted to `BCC +8`.

Q9 Part IA 1996 electrical

Dfm 27.1.96

energy stored in a capacitor



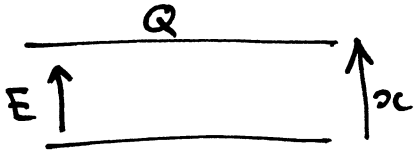
Works done by battery $\delta W = V\delta q$

$= \frac{q}{C}\delta q$

Total work $W = \int_0^Q \frac{q}{C}\,dq$

$= \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2}QV$

Force on plate of capacitor



keep charge constant

Mechanical work done separating plate δx = Change in electrostatic energy

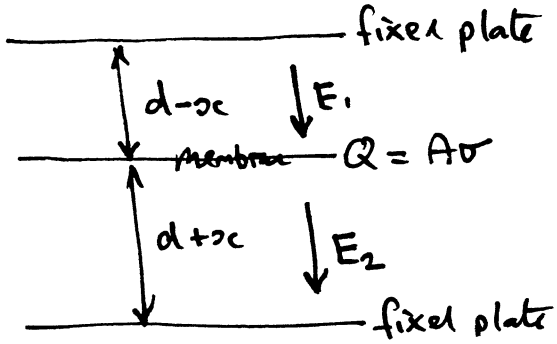
that is $-F\,\delta x = \frac{1}{2}Q\,\delta V$

$$F = -\frac{1}{2}Q\left.\frac{\delta V}{\delta x}\right)_{Q\text{constant}}$$

$$\text{Force } F = -\tfrac{1}{2}QE$$

Loudspeaker

approximate neglect end fringing effects.



Total force on membrane $F = \frac{1}{2}QE_1 + \frac{1}{2}QE_2$ (i)

Apply Gauss Law to membrane $(E_2 - E_1)A = \frac{Q}{\varepsilon_0}$ (ii)

Total voltage V applied $V = E_1(d-x) + E_2(d+x)$ (iii)

Q 9 (continued) Eliminate E_1 and E_2 from the equations to find F. Dfm 27.1.96

Part Ia 1996 electrical

From eqn. (iii) $V = (E_1 + E_2)d + (E_2 - E_1)x$

use from (ii) $E_2 - E_1 = \frac{Q}{A\varepsilon_0}$

$$\therefore V = (E_1 + E_2)d + \frac{Qx}{A\varepsilon_0}$$

$$\therefore E_1 + E_2 = \frac{V}{d} - \frac{Qx}{A\varepsilon_0 d}$$

In (i) $F = \frac{1}{2}Q(E_1 + E_2)$

$$= \frac{1}{2}Q\frac{V}{d} - \frac{1}{2}\frac{Q^2 x}{A\varepsilon_0 d}$$

Force $F = \frac{1}{2}\frac{A\sigma}{d}.V - \frac{1}{2}\frac{A\sigma^2}{\varepsilon_0 d}.x$

Since σ is constant this force is directly proportional to V and to x which is important for linear response in a high quality loudspeaker.

At equilibrium $F = 0$

$$\therefore 0 = \frac{1}{2}\frac{A\sigma}{d}\left(V - \frac{\sigma x}{\varepsilon_0}\right)$$

$$\therefore V = \frac{\sigma x}{\varepsilon_0}$$

For 100 μm equilibrium displacement @ 1 volt

$$\sigma = \frac{V\varepsilon_0}{x}$$

$$= \frac{1 \times 8.9 \times 10^{-12}}{10^{-4}}$$

Charge density $\sigma = 8.9 \times 10^{-8}$ Coulomb metre^{-2} required.

Q10. Part IA 1996 electrical

Gauss Law.

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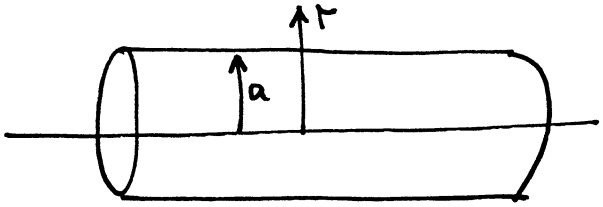
Flux of $\underset{\sim}{D}$ across a closed surface = electrostatic charge enclosed.

$$\iint_S \underset{\sim}{D} \cdot d\underset{\sim}{S} = Q$$

Cylinder geometry radius a cylinder

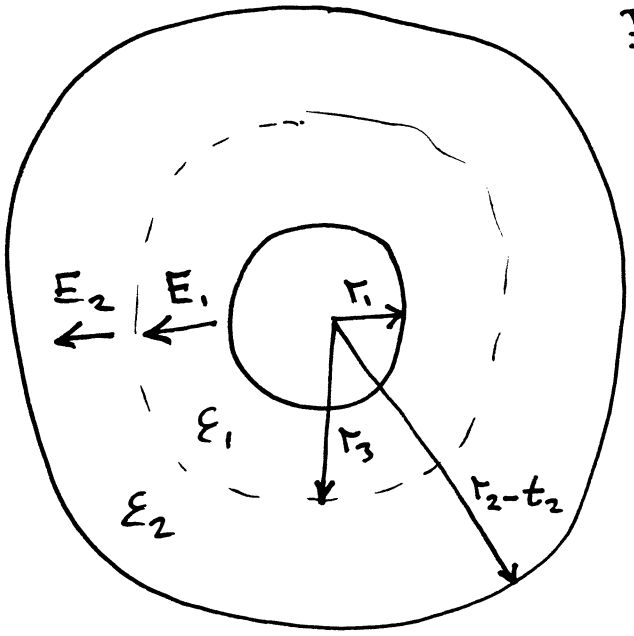


Consider point r where $r \geq a$

$\underset{\sim}{D}$ is radially outwards as $\underset{\sim}{D} \parallel \underset{\sim}{S}$

Here Gauss Law becomes $2\pi r D = Q$

$$\underset{\sim}{D} = \frac{Q}{2\pi r}$$



For the cable the relevant dimensions are $r_2 - t_2$ for the outer conductor and r_1 for the inner conductor

Let the charge per unit length be Q

Apply Gauss Law $D = \frac{Q}{2\pi r}$ i.e. $E_1 = \frac{Q}{2\pi\varepsilon_0\varepsilon_1 r}$

But $D = \varepsilon_0\varepsilon_r E$ $E_2 = \frac{Q}{2\pi\varepsilon_0\varepsilon_2 r}$

Determine the capacitance per unit length from $Q = CV$

$$\text{Total } V = \int_{r_1}^{r_3} \frac{Q}{2\pi r \varepsilon_0 \varepsilon_1} dr + \int_{r_3}^{r_2 - t_2} \frac{Q}{2\pi r \varepsilon_0 \varepsilon_2} dr$$

Q 10. (continued) Part Ia 1996 electrical

$$V = \frac{Q}{2\pi\varepsilon_0\varepsilon_1}\ln\left(\frac{r_3}{r_1}\right) + \frac{Q}{2\pi\varepsilon_0\varepsilon_2}\ln\left(\frac{r_2-t_2}{r_3}\right)$$

Hence $$C = \frac{2\pi\varepsilon_0}{\left(\frac{1}{\varepsilon_1}\ln\left(\frac{r_3}{r_1}\right) + \frac{1}{\varepsilon_2}\ln\left(\frac{r_2-t_2}{r_3}\right)\right)}$$

For $r_1 = 2\,mm$, $r_2 = 5\,mm$, $t_2 = 0.5\,mm$, $r_3 = 3\,mm$, $\varepsilon_1 = 10$, $\varepsilon_2 = 5$

$$C = \frac{2\pi\varepsilon_0}{\frac{1}{10}\ln\left(\frac{3}{2}\right) + \frac{1}{5}\ln\left(\frac{4.5}{3}\right)} = \frac{2\pi\varepsilon_0}{\frac{3}{10}\ln(1.5)} = \underline{\underline{4.6\times10^{-10}\ Fm^{-1}}}$$

With 100 volt applied

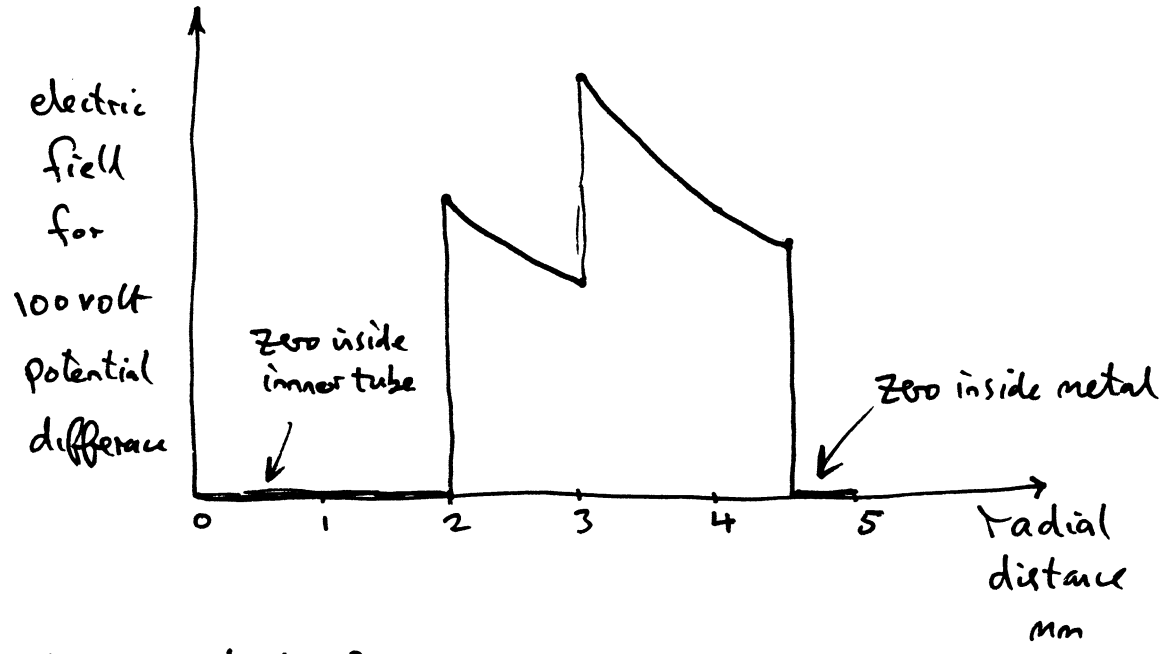
$$Q = CV = 4.6\times10^{-10}\times100 = 4.6\times10^{-8}\ Cm^{-1}$$

$$E_1 = \frac{Q}{2\pi\varepsilon_0\varepsilon_1 r}$$

$$= \text{at } r_1 = 2\,mm \quad \frac{4.6\times10^{-8}}{2\pi\ 8.9\times10^{-12}\times10\times2\times10^{-3}} = 4.1\times10^{4}\ Vm^{-1}$$

$$E_2 = \frac{Q}{2\pi\varepsilon_0\varepsilon_2 r}$$

$$= \text{at } r_3 = 3\,mm \quad \frac{4.6\times10^{-8}}{2\pi\ 8.9\times10^{-12}\times5\times3\times10^{-3}} = 5.5\times10^{4}\ Vm^{-1}$$



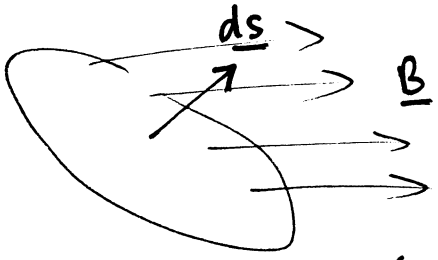
Maximum electric field is at $r = 3\,mm$

and is $\underline{\underline{5.5\times10^{4}\ Vm^{-1}}}$

Q 11. Magnetic flux

Part Ia
1996
electrical

Dfm
27.1.96

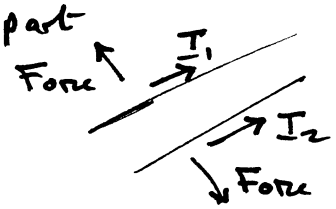


The total magnetic flux Φ through a loop is given by

$$\phi = \iint_S \underline{B} . d\underline{S}$$

where $\underline{B}$ is the magnetic flux density.

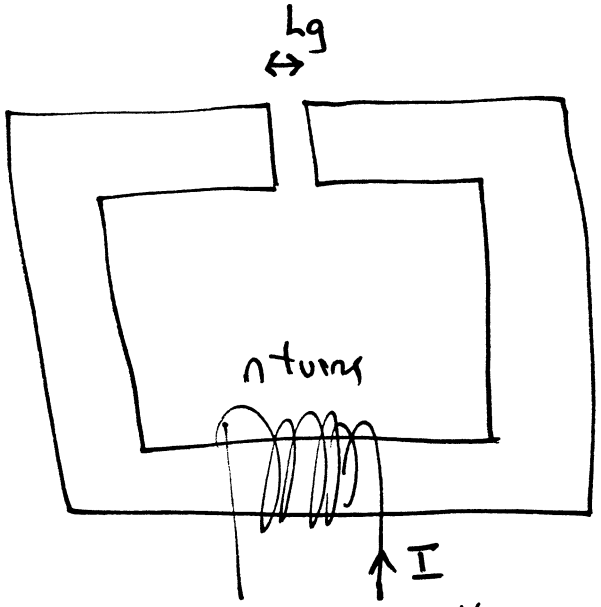
$\underline{B}$ is defined in terms of the force between wires carrying currents I_1 and I_2 r apart length L



$$F = \mu_0 \frac{I_1 I_2 L}{2\pi r} \qquad \left(\frac{\mu_0 I_1}{2\pi r} = B \text{ due to current } I_1 \right)$$

$$= B I_2 L$$

In the electromagnet sketched in the figure the magnetic flux is confined almost entirely to the magnetic material.
Since the cross sections of the magnetic material and the air gap are the same, the magnetic flux density B is also the same.



11 (continued) Part Ia 1996 electrical

DPm 27.1.96

Apply Ampere Law

$$\oint \underline{H} \cdot d\underline{l} = n\underline{I}$$

$$H_g L_g + H_m L_m = n\underline{I} \qquad (i)$$

(H_g: air gap; H_m: magnetic material.)

Apply conservation of magnetic flux $B_g = B_m$ (B_g: gap; B_m: magnetic material.)

But $B_m = \mu_r \mu_0 H_m$

$B_g = \mu_0 H_g$

Substitute into (i)

$$\underline{I} = \frac{1}{n}\left(\frac{B_g}{\mu_0} L_g + \frac{B_m}{\mu_r \mu_0} L_m\right)$$

$$= \frac{1}{\mu_0 n}\left(L_g + \frac{L_m}{\mu_r}\right) B_g$$

For $n = 100$, $L_g = 10^{-3}$ m, $L_m = 50 \times 10^{-3}$ m, $\mu_r = 250$

$$\underline{I} = \frac{1}{4\pi \times 10^{-7} \times 10^2}\left(10^{-3} + \frac{50 \times 10^{-3}}{250}\right) 0.1$$

$$= \frac{1}{4\pi \times 10^{-5}} \times 1.2 \times 10^{-3} \times 0.1$$

$$\underline{I} = 0.95 \text{ amp}$$

If the current were doubled to 2 amp the magnetic flux density would be 0.2T

But if the current were 20x bigger the magnetic material would saturate and there would not be a linear increase in B.

The fringing fields are used in electromagnets for tape heads.