ENGINEERING TRIPOS PART IA

Monday 10 June 1996 1.30 to 4.30

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

Answer not more than **eight** *questions, of which not more than* **three** *may be taken from Section A, not more than* **three** *from Section B, and not more than* ***two*** *from Section C.*

Answers to questions in each section should be tied together and handed in separately.

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SECTION A

Answer not more than **three** *questions from this section.*

1 Figure 1(a) shows the circuit diagram of a test probe, its cable and the input section of an oscilloscope. The oscilloscope input impedance is equivalent to a 1 MΩ resistor in parallel with a 20 pF capacitor. The cable is represented by a 30 pF capacitance to ground.

(a) The probe may be set to either ×1 or ×10 attenuation by the operation of the switch shown. At low frequencies the effects of capacitance may be ignored. Hence calculate the value of R required to achieve the stated attenuation at low frequencies.

(b) For the **×1 switch position** and now also considering the capacitors, derive an expression for the complex input impedance as a function of frequency, seen at the input to the probe.

(c) An engineer wishes to measure the voltage at a test point within a television which monitors the line frequency at 15.6 kHz. An equivalent circuit for the test point is given in Fig. 1(b).

Determine the voltage measured with the probe set to **×1** attenuation.

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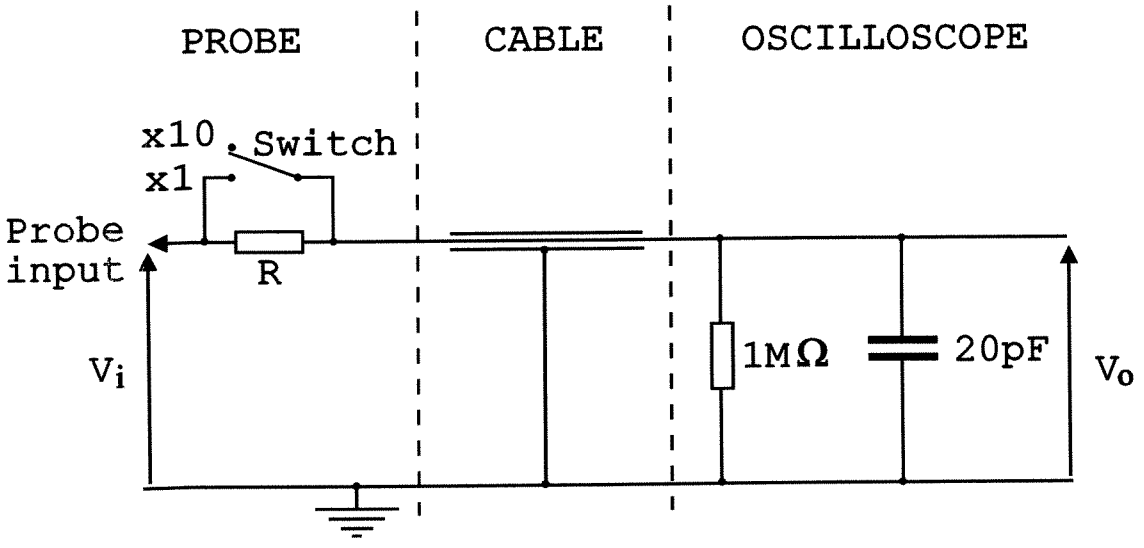

Fig. 1(a)

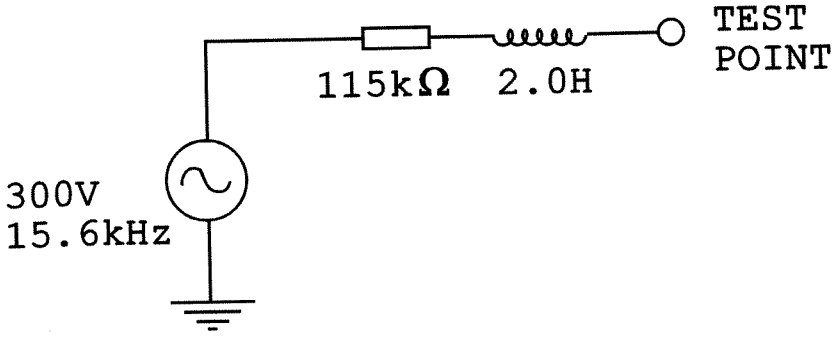

Fig. 1(b)

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2 The circuit of an ac amplifier is shown in Fig. 2.

(a) Calculate the value of R_1 and R_2 required to set the transistor dc operating point where $V_{DS} = 12$ V, $I_D = 0.2$ mA and $V_{GS} = -2$ V. You may assume that the transistor is ideal and that no gate current flows.

(b) Draw the small signal model for the circuit, assuming that the impedances of the capacitors are negligible at signal frequencies.

(c) Derive approximate expressions for the small signal gain V_o / V_i and output impedance for the circuit assuming that the output circuit draws no current. Hence evaluate these expressions with the values of the resistors calculated in (a). For the FET small signal parameters, take $g_m = 10^{-3}$ S and $r_d = 100$ kΩ.

(d) What value of C_1 is required if the circuit is to have a –3 dB $(1/\sqrt{2})$ low frequency cut-off of 15 Hz with a 10 kΩ load connected to the output ?

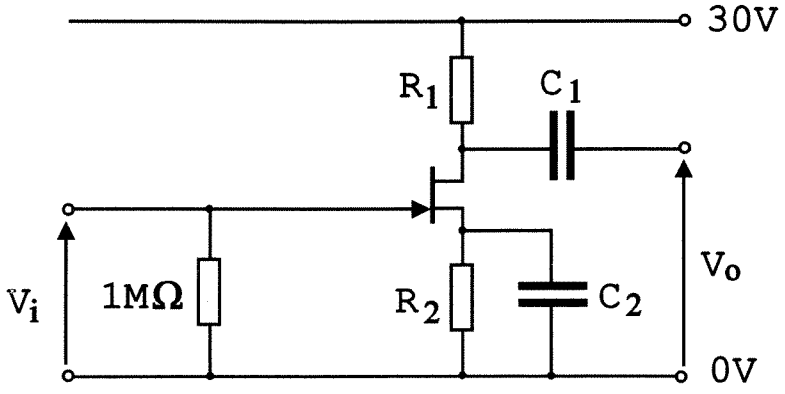

Fig. 2

3 The circuit shown in Fig. 3 represents part of a microphone amplifier from a mobile telephone.

(a) At a mid-band frequency where C_1 may be considered an open circuit, calculate the value of R_2 required to give a voltage gain of 40 dB between input and output. The operational amplifier may be considered to be ideal.

(b) What is the mid-band input impedance of the circuit ?

(c) Calculate the value of C_1 required if the circuit is to have a –3 dB high frequency cut-off of 5 kHz ie. where the circuit gain drops to $1/\sqrt{2}$ of its mid-band value.

(d) If a practical operational amplifier has an open loop voltage gain of ×10,000 and an output impedance of 100 Ω but is otherwise ideal, what is the actual mid-band voltage gain in dB when the circuit drives a load impedance of 50 Ω ?
(Hint: since the load impedance is much smaller than the feedback impedance, the current through R_2 may be neglected if summing currents at the output node).

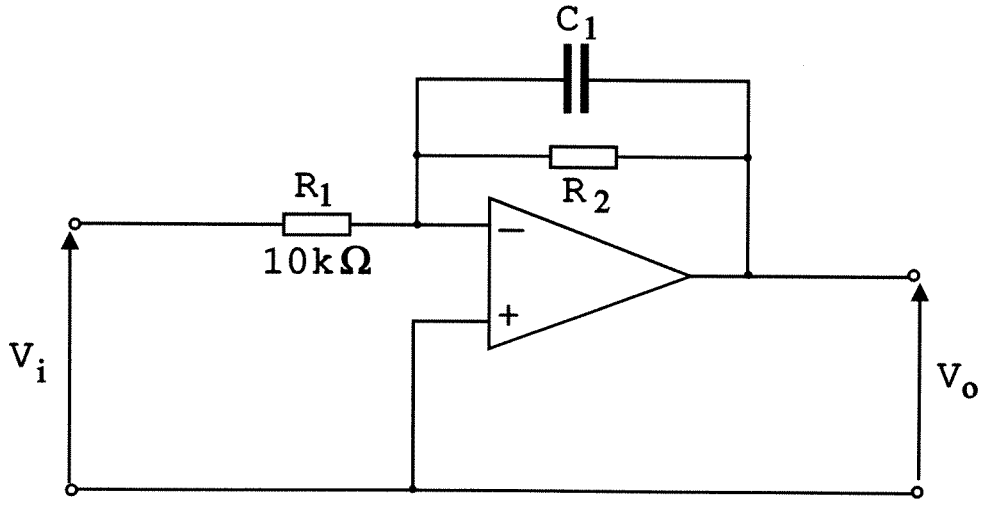

Fig. 3

4 An extraction fan driven by an ac motor is powered from the mains via a long length of cable. The motor, cable and mains supply are represented by the equivalent circuit shown in Fig. 4.

(a) Explain briefly the significance of watts and VARs when delivering power to industrial plant.

(b) Calculate the current drawn from the supply and the power factor.

(c) How many watts and VARs are drawn by the motor and what is the power loss in the cable ?

(d) A capacitor is connected across the motor to correct its power factor to unity. Calculate the required value of this capacitance and determine the new cable loss and VARs drawn from the supply.

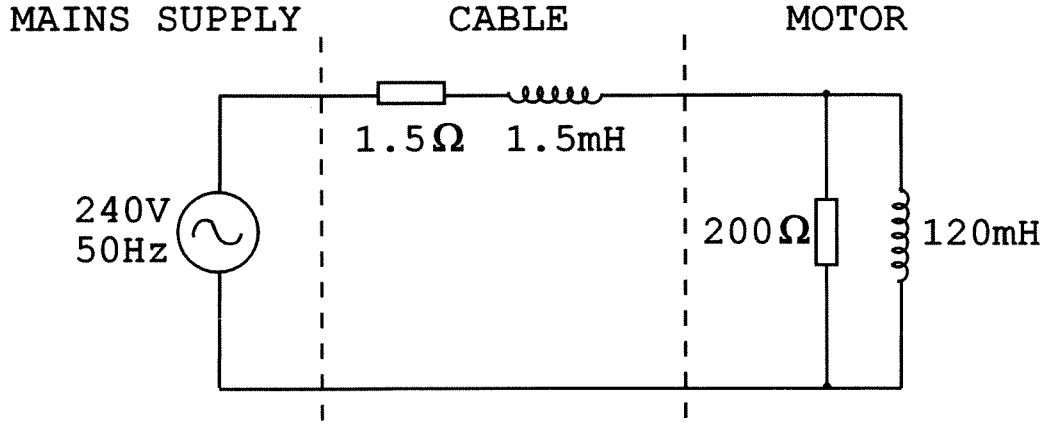

Fig. 4

SECTION B

Answer not more than **three** *questions from this section.*

5 Use a Karnaugh map to simplify the expression

$$Y = A.C.\overline{D} + \overline{A}.B.(C.D + B.C) \quad .$$

Show how to generate the output signal Y from inputs A, B, C and D using only:

(a) inverters and NAND gates;

(b) inverters and NOR gates.

Describe the advantages of making a logic circuit using one type of gate only. What are the disadvantages of a design which uses the minimum number of gates?

6 What is meant by an *unused state* in the design of synchronous sequential logic? How may unused states cause improper operation?

A synchronous sequential logic circuit is to be used to form a four state up-down counter. The counter is to be implemented using three clocked J-K bistables A, B, C with outputs Q_A, Q_B, Q_C. The counter takes two inputs: the clock, and a control signal M which indicates whether the counter should count up or down. M is set at logic 0 to cause the counter to count up, and at logic 1 to cause the counter to count down. The state transition diagram for the counter is shown in Fig. 5, in which the states are shown in the sequence Q_A, Q_B, Q_C.

List the unused states. Assuming that unused states do not occur, construct a state transition table showing each counter state, the next state, and the J and K inputs required for each of the bistables. Hence determine the required J and K inputs for the three bistables.

Explain carefully what happens if the counter takes up one of the unused states at switch-on.

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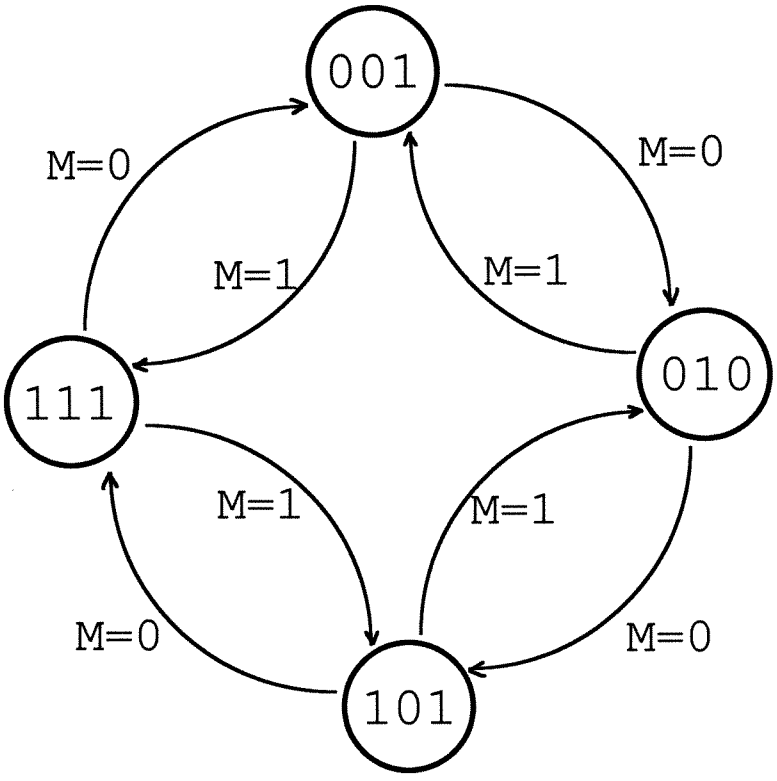

Fig. 5

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7 (a) What is tri-state logic, and what are its major advantages for the implementation of microprocessors and memory systems? Illustrate your answer by means of a diagram showing how to connect a 6800 microprocessor to two 16 K bit random access memory devices organised for 8 bit data, showing clearly the situations in which tri-state devices are employed.

(b) Explain briefly what is meant by *2s complement* representation. Why is it important in information processing?

An eight bit system is required to represent positive and negative numbers using 2s complement notation. Derive the binary equivalents for decimal numbers 51, –126 and 98, explaining your method.

(c) Show how a Set-Reset bistable can be constructed from NAND gates and inverters. Write down the Boolean expressions relating the two outputs to the inputs S and R. What happens if the inputs change from $S = R = 1$ to $S = R = 0$?

8 Explain briefly the role played by the *condition codes register* in programming the 6800 microprocessor. What purposes does this register serve in arithmetic and logical operations?

A system based on the 6800 microprocessor stores an array of data values in consecutive eight bit memory locations starting at location $80. A particular program run on the system contains the segment of code given below:-

```
            CLR   $0040
            LDX   #0
LOOP1       LDAA  $80,X
            LDAB  #8
LOOP2       ROLA
            BCC   $03
            INC   $0040
            DECB
            BNE   LOOP2
            INX
            CPX   #10
            BNE   LOOP1
```

Copy this code segment and add comments to each line which explain what is being done.

Determine what will be the contents of location $40 after executing this code, assuming that the data values stored at location $80 and above consist of ascending numbers 0, 1, 2, ... respectively.

Discuss briefly how you would modify this code in order to handle an array of 100 data values, assuming that sufficient memory is available to store the data.

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SECTION C

Answer not more than **two** *questions from this section.*

9 (a) Derive an expression for the electrostatic energy stored in a capacitor. Then show that the electrostatic force on a capacitor plate is $F = 0.5\,Q\,E$ where Q is the charge and E is the electric field.

(b) Consider an electrostatic loudspeaker the cross section of which is sketched in Fig. 6 where the light plastic membrane area A carries a charge σ per unit area. The signal V is applied between the plates at $x = d$ and at $x = -d$ to displace the membrane from its rest position which is initially $x = 0$.

Derive an expression for the total electrostatic force on the membrane when it has been displaced to position x and a signal voltage V is applied to the loudspeaker, stating any approximations made.

Comment on the form of this expression and the requirements for a high quality loudspeaker.

Calculate the value of σ required if the equilibrium displacement of the membrane is 100 μm for $V = 1$ V.

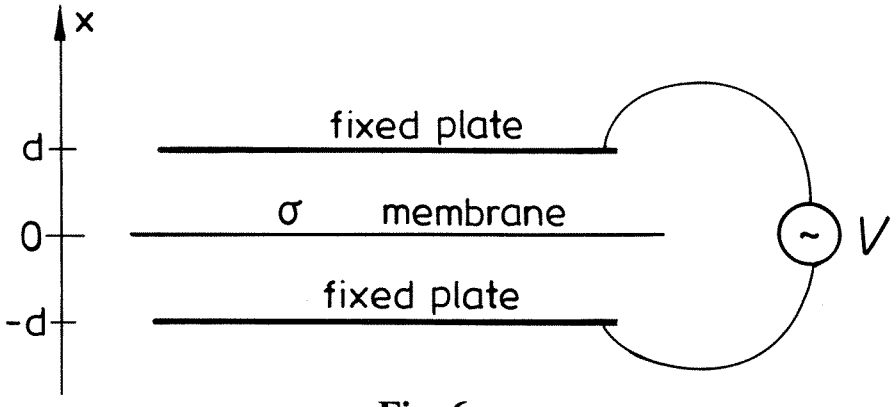

Fig. 6

10 (a) Explain briefly what is meant by Gauss' Law in electrostatics.

(b) The coaxial cable conductor shown in Fig. 7 comprises a central hollow tube outer radius r_1, metal thickness t_1, and a concentric tube outer radius r_2 made of metal thickness t_2. Calculate the capacitance per unit length if the space between the conductors is filled with an insulator of relative permittivity ε_1 to radius r_ε and an insulator of relative permittivity ε_2 otherwise.

(c) Calculate the capacitance per unit length for the case $r_1 = 2$ mm, $r_2 = 5$ mm, $t_1 = t_2 = 0.5$ mm, $r_\varepsilon = 3$ mm, $\varepsilon_1 = 10$ and $\varepsilon_2 = 5$.

(d) If the potential difference applied between the conductors is 100 V, make a sketch of the electric field versus radial distance from $r = 0$ to $r = 6$ mm. What is the maximum electric field strength?

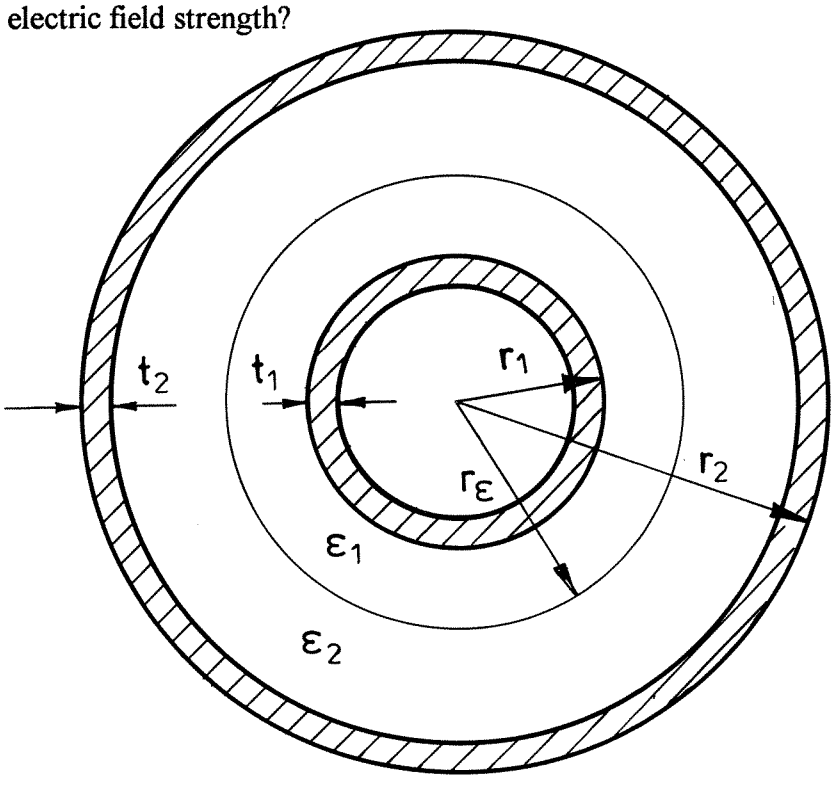

Fig. 7

11 (a) Describe what is meant by:

(i) magnetic flux;

and

(ii) magnetic flux density B.

How are these concepts relevant to flux in the electromagnet sketched in Fig. 8?

(b) Calculate the current required to produce $B = 0.1$ T in the air gap if $L_g = 1$ mm, $L_m = 50$ mm, $n = 100$ and the electromagnet is filled with a linear magnetic material with relative permeability 250, stating any approximations made. Comment briefly on what might happen if the current were to be increased by:

(i) a factor of 2;

and

(ii) a factor of 20.

(c) Explain briefly with a sketch how electromagnets are used in the heads of magnetic tape recorders. What are the design constraints on the size of the gap L_g ? What happens to the behaviour of the electromagnet at high frequency?

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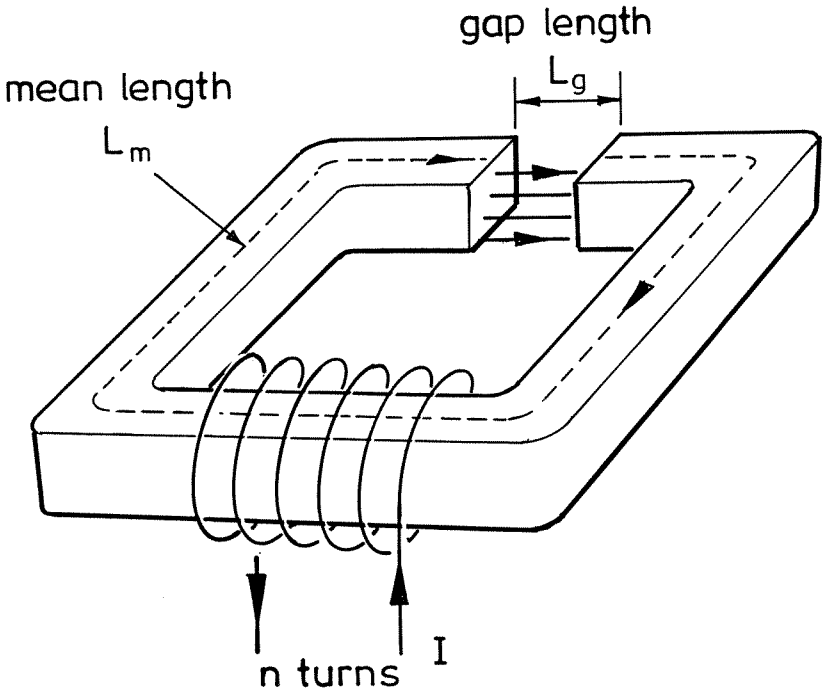

Fig. 8

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