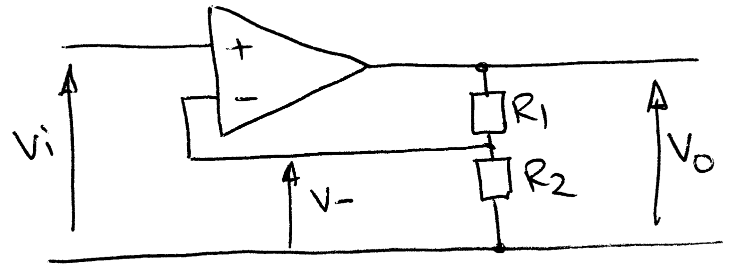
1a) Ideal op-amp has :- infinite input impedance, zero output impedance, infinite differential gain, zero common-mode gain, infinite bandwidth, zero offset voltages

b)



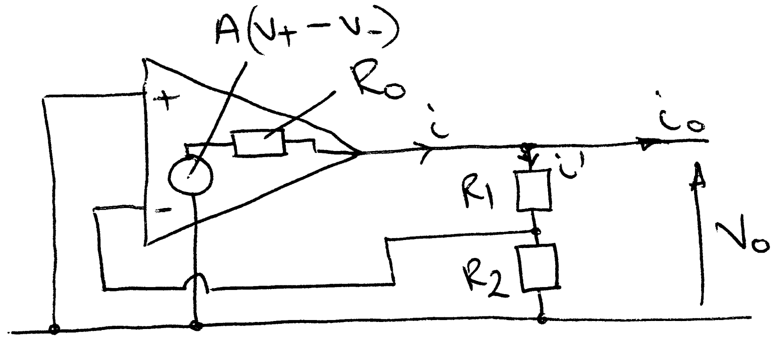
$V_- = \frac{R_2}{R_1+R_2} \cdot V_o$ • potential divider at output • i/p currents zero

$V_i = V_+ = V_-$ • for ideal op-amp

$\therefore V_i = \frac{R_2}{R_1+R_2} \cdot V_o$ $\therefore \frac{V_o}{V_i} = \left(1 + \frac{R_1}{R_2}\right)$ GAIN

non-inverting amplifier

c)



$R_{out} = \frac{V_o}{-i_o}$

$V_+ = 0$, $V_- = \frac{R_2}{R_1+R_2} \cdot V_o$

$V_o = -AV_- - iR_o$ where $i = i_o + i'$

$= i_o + \frac{V_o}{R_1+R_2}$

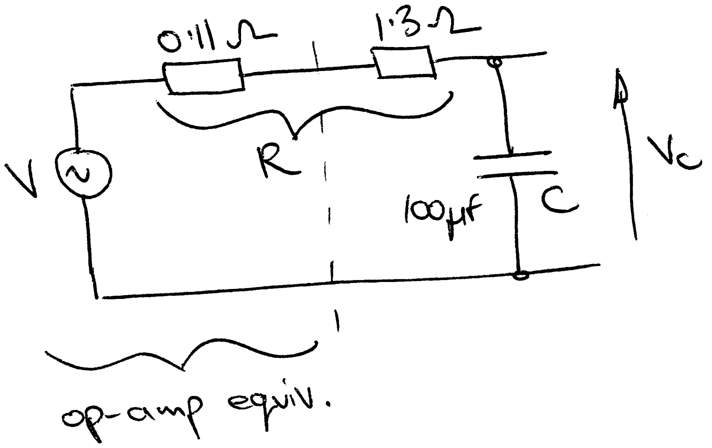
Hence :- $V_o = -A\frac{R_2}{R_1+R_2} \cdot V_o - i_o \cdot R_o - V_o \cdot \frac{R_o}{R_1+R_2}$

Re-arrange :- to give R_{out} $\frac{V_o}{-i_o} = \frac{R_o}{\left(1 + \frac{AR_2}{R_1+R_2} + \frac{R_o}{R_1+R_2}\right)} = \underline{0.11\,\Omega}$

1c) contd. with $R_1 = 10k\Omega$, $R_2 = 1k\Omega$
$R_0 = 100\Omega$, $A = 10^4$

This R_{out} is less than R_0 due to negative feedback effects.

d)



[see data book coupling circuits]

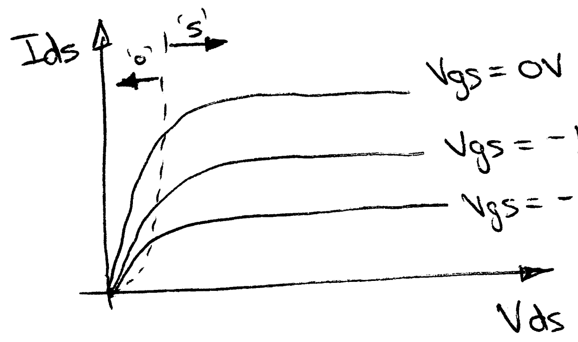
$$V_c = \frac{\frac{1}{j\omega C} \cdot V}{R + \frac{1}{j\omega C}} = \frac{V}{1 + j\omega CR} = \frac{V}{\underset{Re}{1} + j \underset{Im}{2\pi f CR}}$$

Vc drops to 70% of mid-band value when Re = Im

$$\therefore \; f_{-3dB} = \frac{1}{2\pi RC} = \frac{1}{2\pi \cdot 1{\cdot}41 \cdot 100 \times 10^{-6}} = \underline{1130 \text{ Hz}}$$

2a) JFET characteristics :-

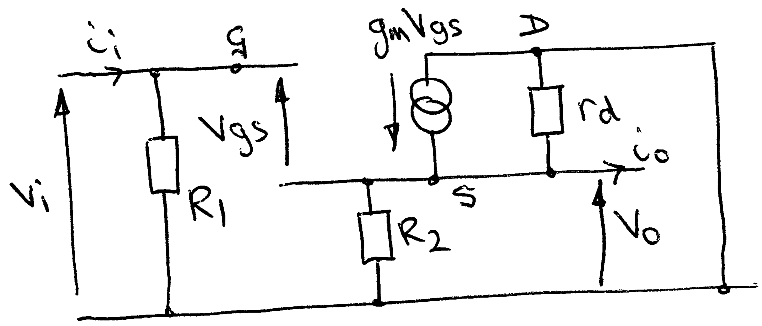
- voltage controlled resistance | current source where Vgs controls Ids
- negligible gate current flows



eg: n-channel device characteristics

'o' ⇒ ohmic region
's' ⇒ saturation region

b)



(i) $R_{in} = \dfrac{V_i}{i_i} = R_1$ as no gate current flows $\therefore R_{in} = 10M\Omega$

(ii) $V_{gs} = V_i - V_o$

parallel combination of R_2 and r_d $\equiv R$ say $(5k\Omega)$

$$V_o = (g_m V_{gs} - i_o) \cdot \frac{R_2 r_d}{R_2 + r_d}$$

$$\therefore V_o = (g_m V_i - g_m V_o - i_o) R$$

$$\therefore (1 + g_m R) V_o = g_m R V_i - i_o R$$

$$\therefore V_o = \underbrace{\frac{g_m R}{(1 + g_m R)}}_{\text{GAIN}} \cdot V_i - \underbrace{\frac{R}{(1 + g_m R)}}_{\text{OUTPUT IMPEDANCE}} \cdot i_o$$

GAIN $= \dfrac{10}{11} = 0.91$

OUTPUT IMPEDANCE $= 455\ \Omega$

2 b) contd.

ie: GAIN = $\dfrac{g_m R_2 r_d}{R_2 + r_d + g_m R_2 r_d}$

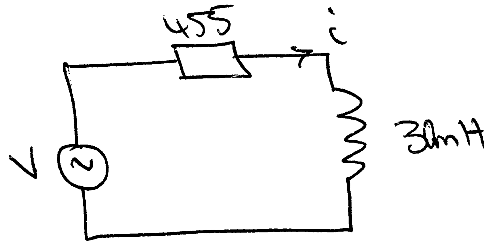
OUTPUT IMPED. = $\dfrac{R_2 r_d}{R_2 + r_d + g_m R_2 r_d}$

c) This circuit is a non-inverting buffer with: input impedance = $10M\Omega$
output impedance = $455\ \Omega$
gain ≈ 1

(source follower circuit)

Useful in pre-amplifier circuits eg: for a microphone where source impedance is very high and needs a buffer to drive lower impedance loads without severe attenuation.

d)



$$i = \frac{v}{\underbrace{455}_{Re} + j\underbrace{2\pi f\, 30\times10^{-3}}_{Im}}$$

70% of mid-band current when Re = Im then $|i| = \left|\dfrac{i_{max}}{\sqrt{2}}\right|$

$\therefore\ 455 = 2\pi f\ 30\times10^{-3}$

$\therefore\ f_{-3dB} = 2.41\ \text{KHz}$

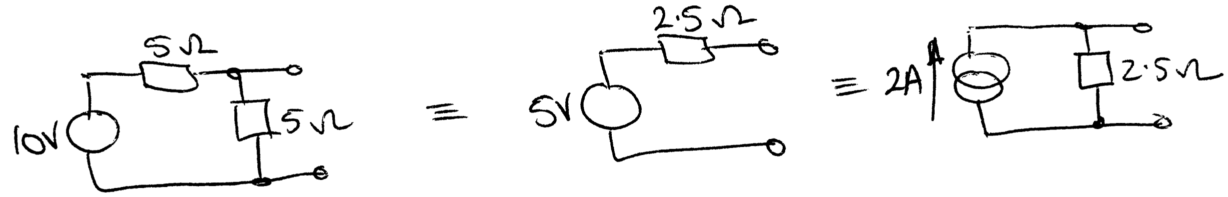
3a) Any network of linear components and voltage/current sources with 2 terminals can be represented by:-

Thevenin: a single voltage source in series with a resistor

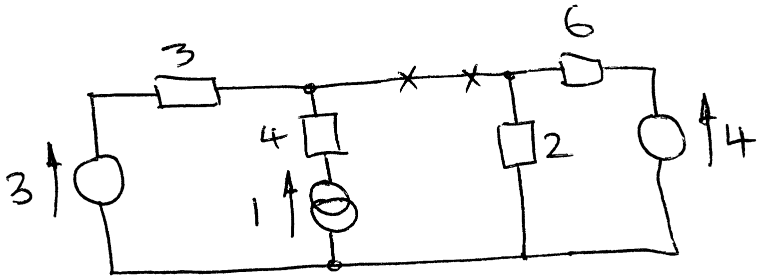
Norton: a single current source in parallel with a resistor (or conductance).

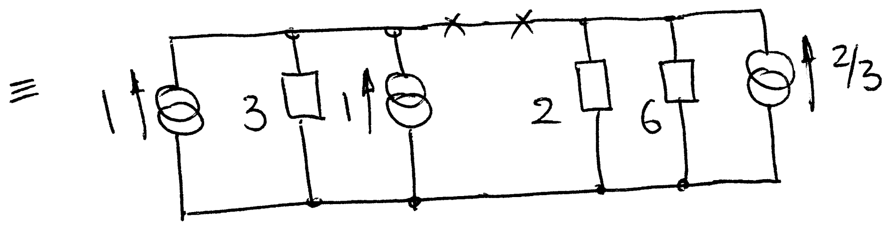
where $V = IR$

V is open circuit voltage, I is short circuit current

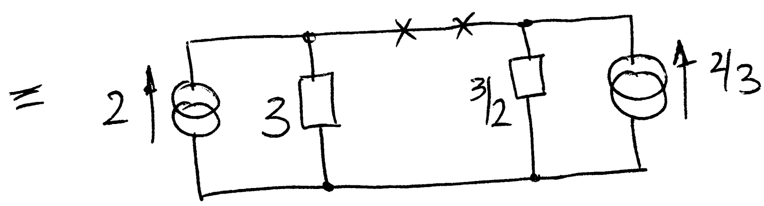


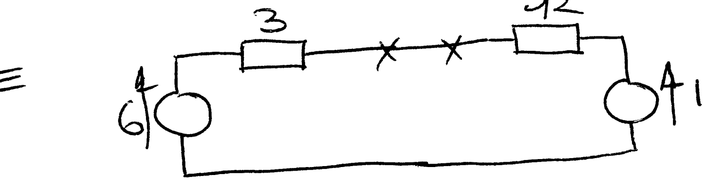
b)





(note 4Ω resistor has no effect in this part)





∴ current in X–X

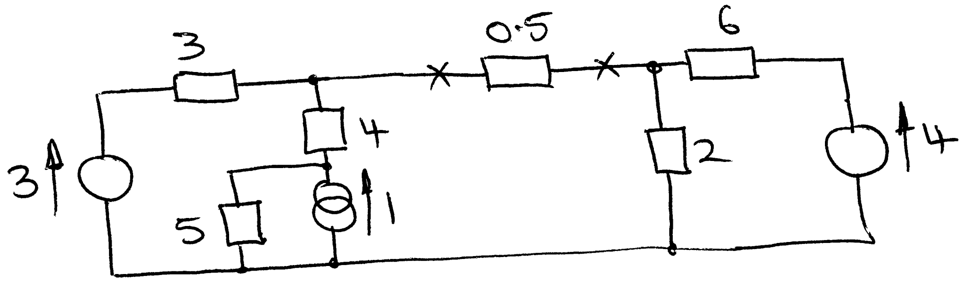
$$= \frac{6-1}{3+3/2} = \frac{10}{9}\,A$$

3c) Putting $0.5\,\Omega$ into x–x

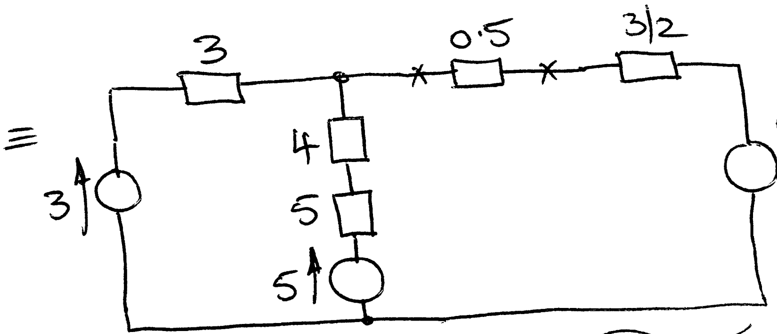
$\Rightarrow$ current $= \dfrac{6-1}{3+3/2+0.5} = \underline{1.0\text{ A}}$

power $= I^2R = \underline{0.5\text{ W}}$

d)

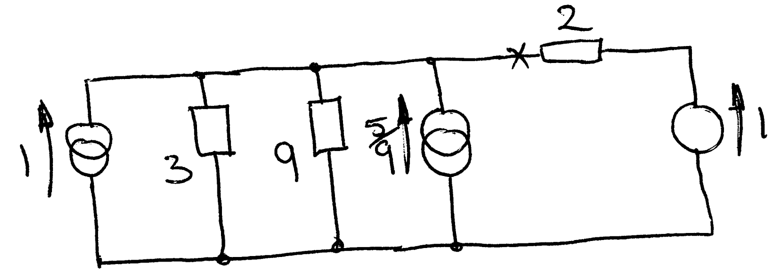


$\equiv$

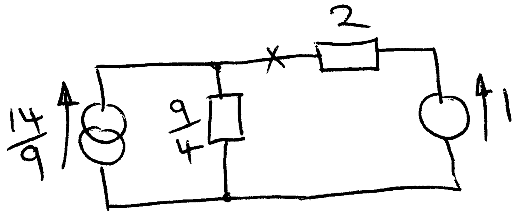


as before

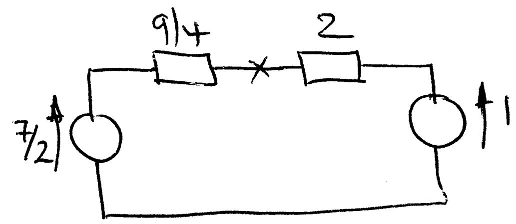
$\equiv$



$\equiv$



$\equiv$



$\therefore$ current in x–x $= \dfrac{7/2 - 1}{9/4 + 2} = \underline{\dfrac{10}{17}\text{ A}}$

$(= 0.588\text{ A})$

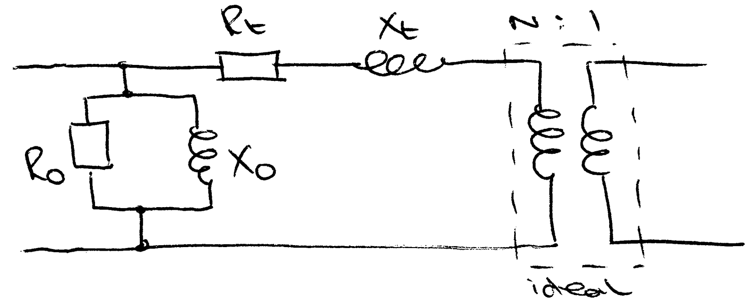
4a) Turns ratio, N = voltage ratio $= \frac{240}{30} = 8:1$

Impedance is transfered across $\times N^2$

$\therefore$ refered to H.V. side $Z_L' = (10 + j5) . 8^2$

$= 640 + j320 \ \Omega$

b)



R_t represents series resistance of windings ie: copper loss

X_t — " — leakage flux across transformer

R_o — " — hysteresis + eddy current losses in transformer core ie: iron loss

X_o — " — inductance of windings on core (finite due to reluctance of flux path)

c) open cct test :- ignore R_t, X_t

$V = 240V$
$I = 0.1A$
$P = 12W$

$$R_o = \frac{V^2}{P} = \frac{240^2}{12} = 4800 \ \Omega$$

$$X_o = \frac{V^2}{Q} , \quad Q^2 = (VI)^2 - P^2 \quad \therefore \quad Q = 20.8 \text{ VAR}$$

$$\Rightarrow X_o = 2771 \ \Omega$$

Short cct. test :- ignore R_o, X_o

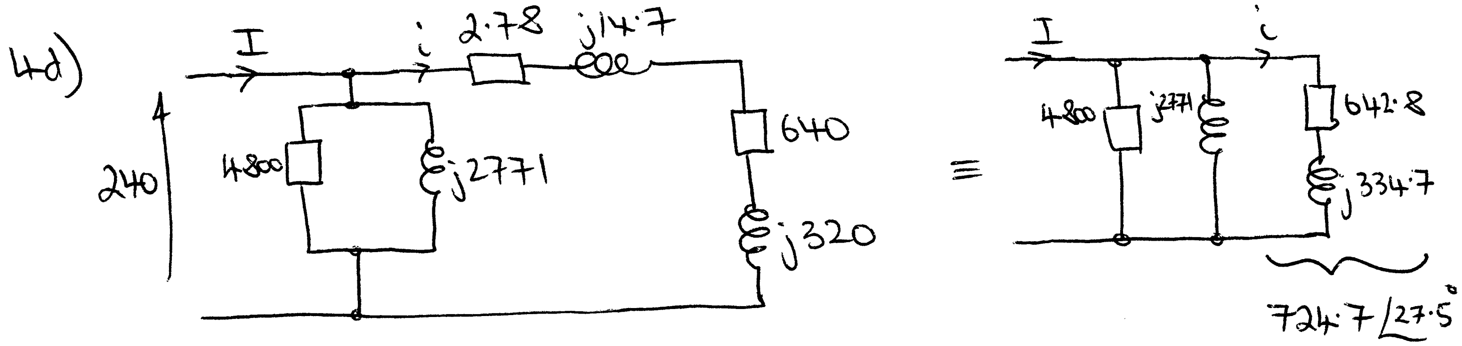
$V = 45V$
$I = 3A$
$P = 25W$

$$R_t = \frac{P}{I^2} = 2.78 \ \Omega$$

$$X_t = Q/I^2 , \quad Q^2 = (VI)^2 - P^2 \quad \therefore \quad Q = 132.7 \text{ VAR}$$

$$\Rightarrow X_t = 14.7 \ \Omega$$

4d)



$$i = \frac{240\angle 0}{724 \cdot 7 \angle 27 \cdot 5^\circ} = 0 \cdot 331 \angle -27 \cdot 5^\circ$$

for load and series components $\therefore$ $P = VI\cos\theta = 70 \cdot 5 \text{ W}$

$Q = VI\sin\theta = 36 \cdot 7 \text{ VAR}$

$$\therefore P_{total} = \frac{240^2}{4800} + 70 \cdot 5 = \underline{82 \cdot 5 \text{ W}}$$

$$Q_{total} = \frac{240^2}{2771} + 36 \cdot 7 = 57 \cdot 5 \text{ VAR} \quad (*)$$

$$\text{and } (VI)^2 = P^2 + Q^2 = 82 \cdot 5^2 + 57 \cdot 5^2 = (240\, I)^2$$

$$\therefore \underline{I = 0 \cdot 419 \text{ A}}$$

$$\text{Power factor} = P/VI = \frac{82 \cdot 5}{0 \cdot 419 \,.\, 240} = \underline{0 \cdot 82 \text{ lag}}$$

e)

To correct the power factor to unity at the mains the capacitor must 'generate' $-57 \cdot 5$ VAR from (*) to give 0 VAR net.

$$\frac{V^2}{1/\omega C} = 57 \cdot 5 = V^2 \omega C \quad \therefore C = \frac{57 \cdot 5}{240^2 \,.\, 2\pi \,.\, 50}$$

$$\Rightarrow \underline{C = 3 \cdot 18 \ \mu F}$$

5. **Main points:**

- The Karnaugh map is a graphical way of visualising logical expressions - it capitalises on the human eye's ability to detect clusters of similar items.
- Each cell corresponds to a particular combination of states of the input variables (logical AND).
- To map a function, place 1, 0 or X (don't care) in the cell corresponding to each combination of inputs.
- The possible input states are ordered such that combinations in cells which are adjacent horizontally or vertically differ in the value of one variable only, e.g. 00, 01, 11, 10. Hence groups of two cells (vertical or horizontal) are *independent of one variable*.
- The map is continuous - the rightmost column is adjacent to the leftmost; similarly with top and bottom rows.
- Thus groups of cells (2, 4, 8 or 16 cells arranged as squares or simple rectangles) may be identified by drawing loops; each loop thus corresponds to a simplified logical expression. The larger the loop, the smaller the number of input terms ANDed together.
- Several loops can be considered and ORed together to determine the complete function in the form of a sum of products. Loops may overlap a cell or cells more than once.
- The Karnaugh map is of greatest use in problems involving 2, 3, 4 or possibly 5 input variables.

Other points:

- It is sometimes useful to note that cells which are adjacent along a diagonal are related by the XOR of two input variables.
- The KM also facilitates the detection of static hazards, which are indicated on the map by loops which meet but do not overlap.

Two's complement is important in information engineering since it provides a consistent means of representing negative and positive numbers and a way to carry out subtraction using the same hardware used for addition.

Input				Output			
X3	X2	X1	X0	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1

Input				Output			
X3	X2	X1	X0	Y3	Y2	Y1	Y0
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

X_1X_0 / X_3X_2	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	0	0	0	0
10	1	0	0	0

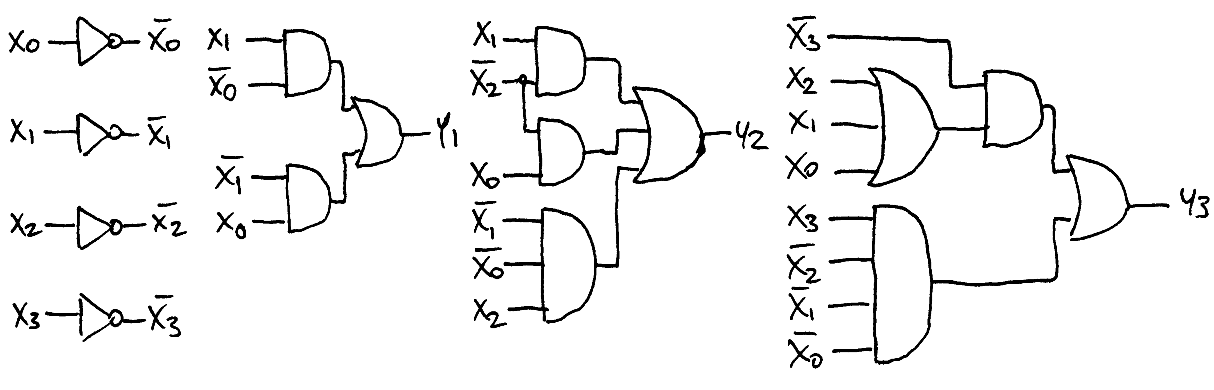
$Y_3 = \bar{X}_3(X_0 + X_1 + X_2) + \bar{X}_0\bar{X}_1\bar{X}_2X_3$

X_1X_0 / X_3X_2	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	1	0	0	0
10	0	1	1	1

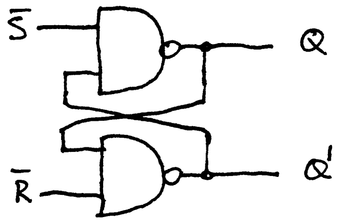
$Y_2 = \bar{X}_0\bar{X}_1X_2 + \bar{X}_2(X_0 + X_1)$

X_1X_0 / X_3X_2	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$Y_1 = X_1\bar{X}_0 + \bar{X}_1X_0$



6.



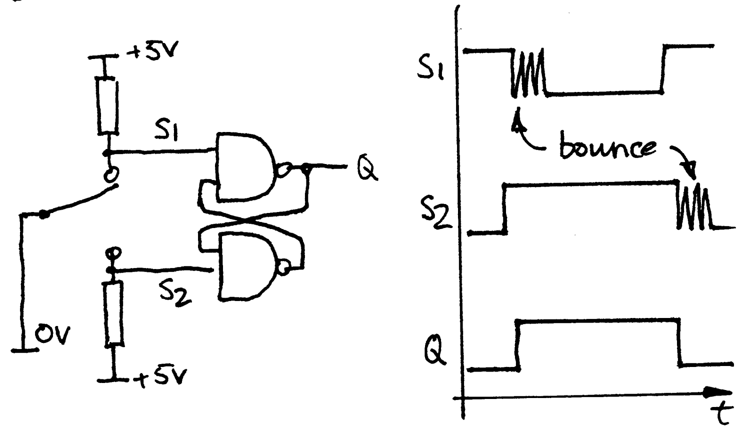
With inputs: $\overline{S}$ and $\overline{R}$ and outputs: Q and Q',

$$Q = \overline{\overline{S}\,.\,Q'} = S + \overline{Q'}$$
$$Q' = \overline{\overline{R}\,.\,Q} = R + \overline{Q}$$

The outputs obey the table below:

$\overline{S}$	$\overline{R}$	Q	Q'
0	0	not	allowed
0	1	1	0
1	0	0	1
1	1	no	change

Debounce circuit



Contact bounce due to wear etc in switch mechanisms gives rise to a sequence of rapid close-open-close events over a few ms. During these events, the other input remains HIGH, preventing Q from following these transitions.

In this instance the states: `0000, 0001, 0010, 1101, 1110` and `1111` are unused.

The *next* state of Q_A, Q_B, Q_C and Q_D is determined by their *present* state. The state transition table shows the permitted transitions. Unused states are assumed not to occur. The required values of J_A - K_D are determined by referring to the J-K excitation table in the Data Book.

Present state				Next state				J & K inputs							
Q_A	Q_B	Q_C	Q_D	Q_A	Q_B	Q_C	Q_D	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	0	1	1	X	0	1	X	X	1	X	1
1	1	0	0	0	0	1	1	X	1	X	1	1	X	1	X

J_B & K_B

Q_CQ_D / Q_AQ_B	00	01	11	10
00	U	U	1	U
01	X	X	X	X
11	X	U	U	U
10	0	0	1	0

Q_BQ_D / Q_AQ_B	00	01	11	10
00	U	U	X	U
01	0	0	1	0
11	1	U	U	U
10	X	X	X	X

Hence $J_B = Q_C Q_D$ $\quad$ $K_B = Q_A + Q_C Q_D$

Q_CQ_D / Q_AQ_B	00	01	11	10
00	U	U	X	U
01	0	1	X	X
11	1	U	U	U
10	0	1	X	X

J_C & K_C

Q_CQ_D / Q_AQ_B	00	01	11	10
00	U	U	1	U
01	X	X	1	0
11	X	U	U	U
10	X	X	1	0

Hence: $J_C = Q_AQ_B + Q_D$ $\qquad$ $K_C = Q_D$

Although J_A, K_A, J_D and K_D are not required, it can be seen immediately by inspection that:

$J_D = 1$ $\qquad$ $K_D = 1$

There are alternative (less efficient) ways of drawing the loops which will give different expressions for the J and K inputs.

If the counter enters the unused state 1111 at the moment of applying power, the equations given/derived above may be used to determine all four J/K inputs in terms of the corresponding Q values. From this can be deduced the states the counter will enter on subsequent clock pulses.

Present state				J & K inputs								Next state			
Q_A	Q_B	Q_C	Q_D	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D	Q_A	Q_B	Q_C	Q_D
1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1
0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0
0	0	1	0	0	1	0	0	0	0	1	1	0	0	1	1

In other words, after 4 clock pulses the counter reaches the state 0011 and enters the correct cycle. If the unused states were entered in the state transition table, it would be possible to allow for a quicker entry into the correct cycle from this and/or other unknown states; however, this would be expected to require additional logic gates.

7 (a) Fig. 4 shows a weighted-resistor DAC. With the OA assumed ideal, the inverting input terminal (summing junction) may be taken as a *virtual earth*. Voltage sources connected at S_0-S_3 contribute currents to the summing junction in inverse proportion to the value of the summing resistor. Hence the contribution of each source to the output voltage V_O is also in inverse proportion to the corresponding resistor. Hence S_0 is the LSB.
The sources need to be Thevenin voltage sources capable of being switched ON or OFF under the control of a digital signal. Typically MOS transistor switches are used for this purpose.

If the resistors are chosen to be in powers of 2, the output voltage is given by:-

$$V_O = \frac{R}{2}\left[\frac{S_0}{8R} + \frac{S_1}{4R} + \frac{S_2}{2R} + \frac{S_3}{R}\right]$$

(b) If $S_0 = S_1 = S_2 = S_3 = 5$V, the output voltage is: $\frac{5}{2}\left[\frac{1}{8} + \frac{1}{4} + \frac{1}{2} + \frac{1}{1}\right] = \frac{75}{16} = 2.6875V$

Since the inverting input to the OA is a virtual earth, the input resistance at S_1 is $4R = 4K\Omega$. The input resistance at S_3 is $R = 1K\Omega$.

(c) In the R-2R circuit, only two different resistor values are used. Each voltage source feeds through a resistance of $2R$, then the current splits, part going to the left, the remainder going to the right. If the voltages sources connected to S_1-S_3 are perfect Thevenin sources, and using superposition, it can be shown that at each split, exactly half the current input proceeds to the right (towards the OA inverting input). At each junction the current splits again, part bypassed to earth via $2R$. Hence the current contribution from S_0 is divided by 2 four times; that from S_3 only once. The LSB is thus S_0.

Again, assuming perfect voltage sources and assuming that the OA inverting input is a virtual earth, the input resistance at any input S_0-S_3 is $2R + (2R \parallel 2R) = 3R$.

For this design the output voltage V_O is:-

$$V_O = R_F\left[\frac{S_0}{16\times 3R} + \frac{S_1}{8\times 3R} + \frac{S_2}{4\times 3R} + \frac{S_3}{2\times 3R}\right]$$

This must equal 75/16 V.

Hence $\frac{75R_F}{48R} = \frac{75}{16}$, and $R_F = 3K\Omega$.

Some advantages of R-2R ladder

- Only two resistor values are required. Leads to ease of integration and compact design, since values can be quite low, say $1K\Omega$ and $2K\Omega$. Weighted resistor version may need a wide range of resistor values.
- Temperature stability is easier to achieve since all resistors being of similar values can use the same technology and be of similar dimensions.
- The input resistance seen by each voltage source is fixed. This simplifies design of voltage sources and enhances accuracy.

8. A register is a small memory within the CPU. As well as being available for storing information, registers may have additional functions - for example, some can be incremented or decremented, or can receive results from the arithmetic unit. Other registers may simply be a convenient way to group sets of bistables which determine the state of the CPU (e.g. CCR). The following exclude discussion of interrupts which are not covered in the IA course.

Seven registers are available in the 6800 microprocessor. These are shown diagrammatically in the Microprocessor Data Book.

Accumulators A, B
These are 8-bit data registers which can participate in virtually all arithmetic and logical operations, as well as being shifted or rotated, loaded and stored.

Index register X
A 16-bit register which can be loaded, stored, incremented or decremented. May thus be used as a 16-bit counter. Its main use is in indexed addressing where it holds the address of a block of data. INC/DEC instructions allow the address to be changed to reference each item of data conveniently.

Stack pointer SP
A 16-bit register which holds the address of a dedicated area of memory (the stack) used to hold the return address during function/subroutine calls and for access by the programmer using PSH/PUL instructions.

Program counter PC
A 16-bit register which holds the address of the next instruction to be executed. It is incremented automatically during each instruction, but can be changed by the programmer using Branch, JMP or JSR instructions.

Condition code register
An assembly of bistables which indicate the outcome of logic and arithmetic instructions. Used in Branch, arithmetic and other instructions.

C - Carry bit - used in arithmetic operations on signed numbers, when it represents the Carry out of Bit 7. Also required for unsigned binary addition and subtraction for numbers larger than 8 bits. Several of the Shift and Rotate instructions shift data via the Carry bit. This allows for easy testing.

V - 2's complement overflow - set to 1 whenever overflow is detected in 2s complement signed arithmetic. This is the logical XOR of the carries out of Bits 6 and 7.

Z - Zero - set 1 whenever an arithmetic operation generates a zero result.

N - Negative - set 1 when the MS bit of the result of an arithmetic or logical operation is 1.

H - Half-carry - set 1 when an arithmetic operation causes a carry to be generated out of bit 3. Used in BCD arithmetic.

(b)

(i) ASLB - Arithmetic shift left accumulator B (through the C bit of the CCR)

ACCA remains unchanged. ACCB becomes \$02. C becomes 1, Z becomes 0, N becomes 0.

(ii) ABA - Add accumulator B to accumulator A

ACCB remains unchanged. ACCA becomes \$00 (\$81+\$7F). C becomes 1, Z becomes 1, N becomes 0.

(iii) INCA - Increment accumulator A

ACCB remains unchanged. ACCA becomes \$80 (\$7F+\$01). C is unaffected (stays at 0), Z becomes 0, N becomes 1.

(c) When power is applied, C is initially discharged, holding v at 0 V and v_2 at logic 1. v will rise as C charges. When v reaches 2.5 V (see Schmitt trigger transfer function), v_2 will switch to logic 0. Hence the time constant formed by C with the 20 KΩ resistor must be adjusted so the C charges from 0 to 2.5 volts in 10 ms (or more).

Note that the output signal v_2 is in the wrong logical sense to hold the $\overline{RESET}$ pin low for 10 ms. Hence an inverter is needed to connect to the pin.

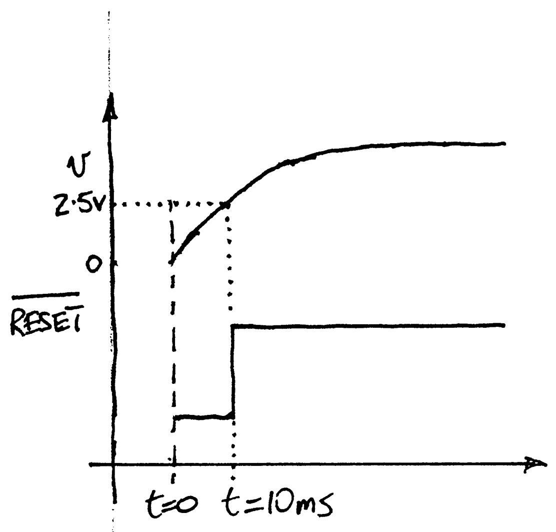
To determine a suitable value for C, assume the 5 volt rail rises abruptly at switch-on (t = 0); then:

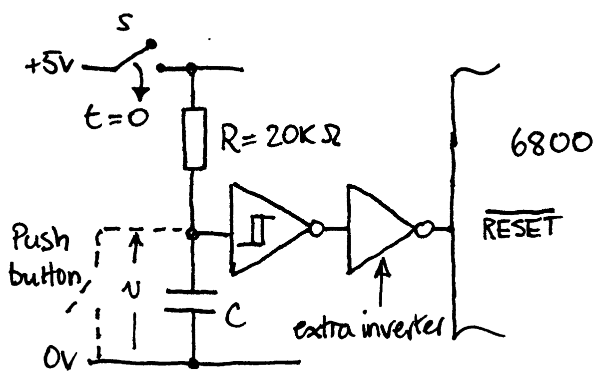
$2.5 = 5(1 - e^{-t/CR})$. Thus: $e^{-t/CR} = 0.5$.

Take logs to base e, then: $-\dfrac{t}{CR} = -0.693$

$$\text{Hence } C = \frac{t}{0.693} \cdot \frac{1}{R} = \frac{10^{-2}}{0.693 \times 2 \times 10^{4}} = 0.72 \times 10^{-6}\ F \quad = \quad 0.7\ \mu F \text{ (or greater)}$$

To allow the $\overline{RESET}$ signal to be generated manually, connect a push-button switch in parallel with C.





IA EXAM 1997

DJBM 22..97

Q9. Electric field due to a sphere radius a with charge Q

for $r \geq a$ $\quad E = \frac{Q}{4\pi\varepsilon_0 r^2}$

for $r < a$ $\quad E = 0$

Calulate capacitance. Let the potential be V

$$V = \int_a^\infty E\,dr = \left[-\frac{Q}{4\pi\varepsilon_0 r} \right]_a^\infty = -\frac{Q}{4\pi\varepsilon_0 a}$$

Capacitance $C = \frac{Q}{V} = \frac{Q}{Q/4\pi\varepsilon_0 a} = 4\pi\varepsilon_0 a.$

When the drop leaves the nozzle at $+30$ V it carries a positive charge and is therefore attracted towards plate B. But the high velocity of $-4\ ms^{-1}$ in the y direction ensures that the acceleration in the $+x$ direction only has a small effect on the motion.

Calculate force F on the ink drop. $\quad F = EQ$

Electric field between A and B is $\frac{V}{d} = \frac{1500}{10 \times 10^{-3}} = 1.5 \times 10^5\ Vm^{-1}$

Charge on the ink drop $\quad Q = VC = 30 \times 4\pi \times 8.85 \times 10^{-12} \times 35 \times 10^{-6}$

$$Q = 1.17 \times 10^{-13} \text{ Coulomb.}$$

Electrostatic force $F = 1.5 \times 10^5 \times 1.17 \times 10^{-13}$

$$= \underline{\underline{1.75 \times 10^{-8} \text{ Newton}}}$$

The force acts in the x direction

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Q9 (continued) DJfm 22.1.97

Approximate transit time between the plates A and B

$$\tau = \frac{\text{distance}}{\text{speed}} = \frac{30 \times 10^{-3}}{4} = 7.5 \times 10^{-3} \text{ seconds.}$$

During this time the ink drop suffers a constant acceleration in x direction.

Exit velocity component V_x = acceleration × time

$$= \frac{\text{force}}{\text{mass}} \times \text{time}$$

$$= \frac{1.75 \times 10^{-8} \times 7.5 \times 10^{-3}}{\frac{4\pi}{3} \times (35 \times 10^{-6})^3 \times 1000}$$

$$= 0.73 \text{ ms}^{-1}$$

The velocity component $V_y = 4 \text{ ms}^{-1}$ unchanged.

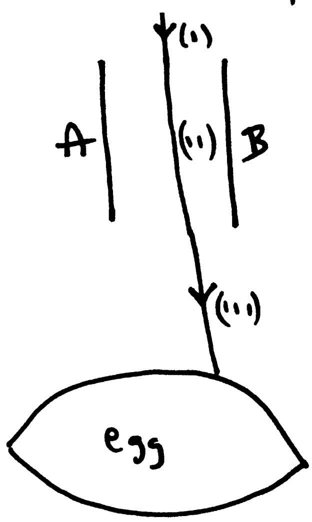
Hence direction is $\tan^{-1}\left(\frac{.73}{4}\right) = \underline{\underline{10^\circ}}$ to the y axis.

Doubling the diameter, capacitance doubles, mass eightfold; acceleration $\frac{1}{4}$ angle $\underline{\underline{2\frac{1}{2}^\circ}}$

The inkjet is operated by controlling the voltage applied to the exit nozzle for printing dots to form letters.

In the case of a curved surface such as an egg the printer works well because the ink is projected onto the object and some variation in the size of the letters can be tolerated.

The inkjet is high throughput and reliable



(i) straight trajectory

(ii) parabolic ..

(iii) straight ..

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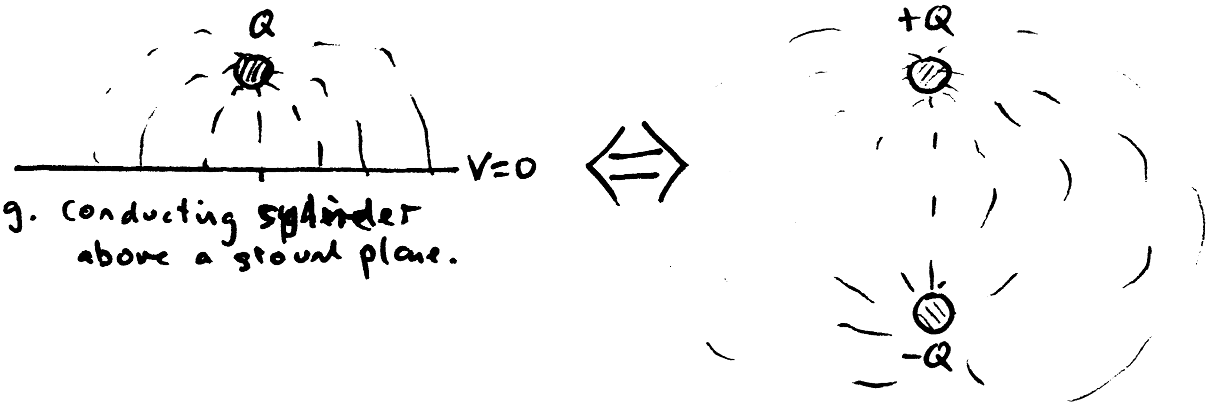
7.7.97

Q 10 Method of Images

An electrostatic problem is unchanged if an equipotential is replaced by a conductor. Apparently complex geometries can be simplified to standard easily solved problems if the initial symmetry is sufficiently high and if conducting surfaces are judiciously introduced or taken away.



e.g. conducting ~~sylinder~~ cylinder above a ground plane.

Simpler problem two cylinders

The other useful principle is superposition.

With linear materials the electrostatic problem can be solved with each of the individual charges alone and then the solutions added.

Person under power line experiences maximum field when half way between the two power lines. But the separation of 3 m is small compared with the height above the persons head of 10 m

Hence solve the single conductor problem and then by superposition add the second similar conductor i.e. double the field.

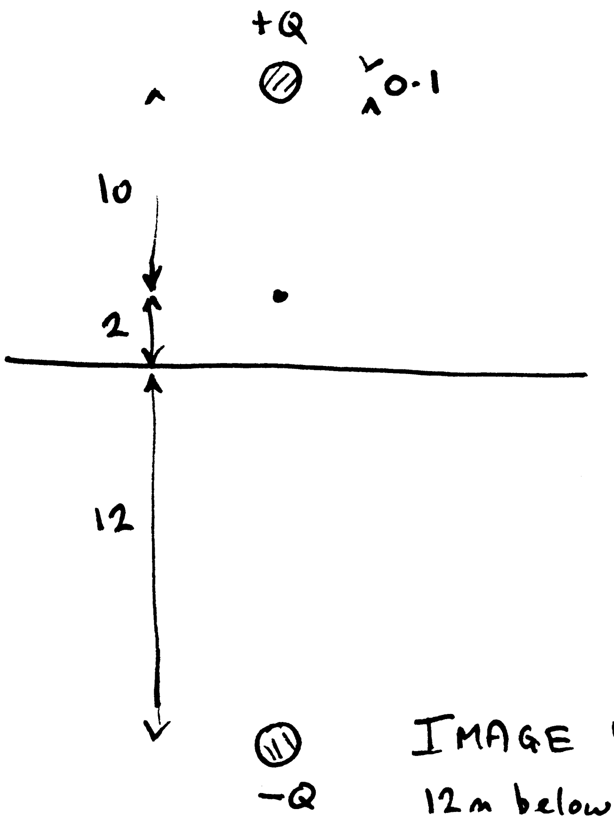


IMAGE WIRE
12 m below ground.

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Q10 (continued) 7.7.97

DKm

For an infinitely long wire carrying a charge Q per unit length the field at a distance r from the wire is $E = \frac{Q}{2\pi r \varepsilon_0}$

Hence the potential at a point a above the ground is $\int E.dr$

$$V = \int_0^a \frac{Q}{2\pi\varepsilon_0(12-x)} + \frac{Q}{2\pi\varepsilon_0(12+x)} \, dx$$

$$= \frac{Q}{2\pi\varepsilon_0}\Big[-\ln(12-x) + \ln(12+x)\Big]_0^a$$

$$= \frac{Q}{2\pi\varepsilon_0} \ln\left(\frac{12+a}{12-a}\right)$$

But for $a = 11.9$ m which is on the power line conductor $V = 300{,}000$

$$\therefore \frac{Q}{2\pi\varepsilon_0} = \frac{V}{\ln\left(\frac{23.9}{0.05}\right)} = \frac{300{,}000}{6.17} = 48600$$

Electric field at a above the ground is

$$E = \frac{Q}{2\pi\varepsilon_0}\left(\frac{1}{12-a} + \frac{1}{12+a}\right)$$

For the person's head $a = 2$

$$E = 48600 \times \left(\frac{1}{10} + \frac{1}{14}\right) = 8330 \ \mathrm{Vm^{-1}}$$

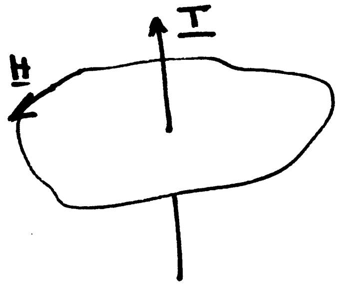
Total electric field is $2 \times 8330 = 16700 \ \mathrm{Vm^{-1}}$

This is a fair approximation since the separation of the conductors is only 3 m which is much smaller than the distance away.

Near the pylon tower the person would experience lower electric fields because the metal pylon is at earth potential and the field is increased near the conductor and correspondingly reduced near the ground. Anyway near the pylon the conductors are likely to be more than 12 m above ground and the field would be correspondingly lower.

1A EXAM 1997

Qu 11 Ampere Law



Dfm 22.1.97

$$\oint \underline{H}.\underline{dl} = I$$

path enclosing the wire — current enclosed

In the electromagnet there are n turns of wire

$$\oint \underline{H}.\underline{dl} = nI$$

The magnetic material is linear (and not saturated) $B = \mu_0 \mu_r H$

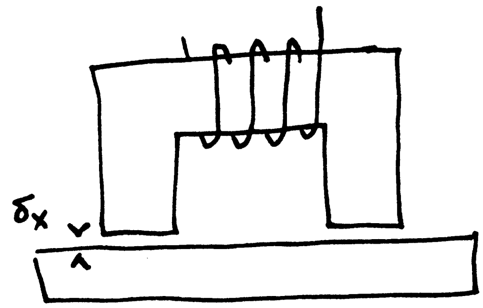
Approximate the geometry to constant cross section core and bar, neglect corner effects

$$BL = n \mu_0 \mu_r I$$

$$B = \frac{n \mu_0 \mu_r I}{L} = \frac{80 \times 1.26 \times 10^{-6} \times 1000 \times 0.5}{0.1}$$

$$= 0.50 \text{ Tesla}$$

Method virtual work



Mechanical work done = increase in magnetostatic energy.

When a small gap δ_x is opened the B in the magnetic circuit barely changes

Hence magnetostatic energy associated with the two gaps is the only change.

Given $W = \int_0^B H.dB$ per unit volume.

In the air $B = \mu_0 H$

$$W = \int_0^B \frac{B}{\mu_0} dB = \frac{1}{2}\frac{B^2}{\mu_0}$$

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Q11 (continued)   Df 22.1.97

Apply conservation of total magnetic flux

$$B_{gap} A = B A$$

Hence increase in magnetostatic energy is $2 \times \frac{1}{2} \frac{B^2}{\mu_0} A \,\delta x$

$$= \frac{B^2 A}{\mu_0} \delta x$$

$$\therefore \quad \underset{\uparrow}{F} \,\delta x = \frac{B^2 A}{\mu_0} \delta x$$

force on bar

$$F = \frac{B^2 A}{\mu_0}$$

$$= \frac{0.5 \times 0.5 \times 3 \times 10^{-5}}{1.26 \times 10^{-6}}$$

$$F = 6 \text{ newtons.}$$

If the current is doubled to 1 amp
the magnetic flux density becomes 1 Tesla and the force 24 newtons.

but if the current is increased to 5 amp
the soft iron core saturates, at possibly 1.5 Tesla
and the corresponding increase in the force is small.