ENGINEERING TRIPOS PART IA

Monday 9 June 1997 1.30 to 4.30

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

Answer not more than **eight** *questions, of which not more than* **three** *may be taken from Section A, not more than* **three** *from Section B, and not more than* **two** *from Section C.*

The **approximate** *number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

(TURN OVER

SECTION A

Answer not more than **three** *questions from this section.*

1 (a) State the assumptions made when describing an operational amplifier as ideal.

(b) Assuming that the operational amplifier shown in the circuit of Fig. 1 is ideal, derive an expression for the output voltage V_o as a function of the input voltage V_i.

(c) If the operational amplifier actually has an open loop gain of 10^4 and an output impedance of 100 Ω, what is the output impedance of the circuit shown in Fig. 1 with $R1 = 10\ k\Omega$ and $R2 = 1\ k\Omega$?

Why is this value less than that of the operational amplifier itself ?

(d) The circuit shown is used to drive an ac transducer, represented by a resistance of 1.3 Ω in series with a capacitance of 100 μF. At what frequency does the voltage across the capacitor drop to 70% of its mid-band value ?

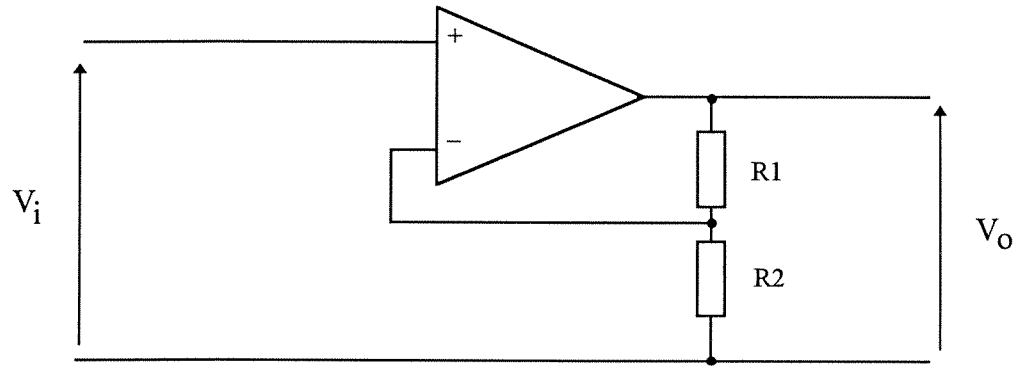

Fig. 1

2 (a) Briefly describe the electrical characteristics of a junction field effect transistor (JFET).

(b) Draw the small signal model for the source follower circuit shown in Fig. 2 and derive expressions for the:

(i) input impedance;

(ii) gain when no load is connected; and

(iii) output impedance.

Evaluate these parameters with $g_m = 2$ mS and $r_d = 10$ kΩ for the transistor, $R1 = 10$ MΩ and $R2 = 10$ kΩ.

(c) Describe the function of the circuit and suggest an application for which it would be useful.

(d) If the circuit is used to drive an inductive load of 30 mH, calculate the frequency at which the load current drops to 70% of its mid-band value.

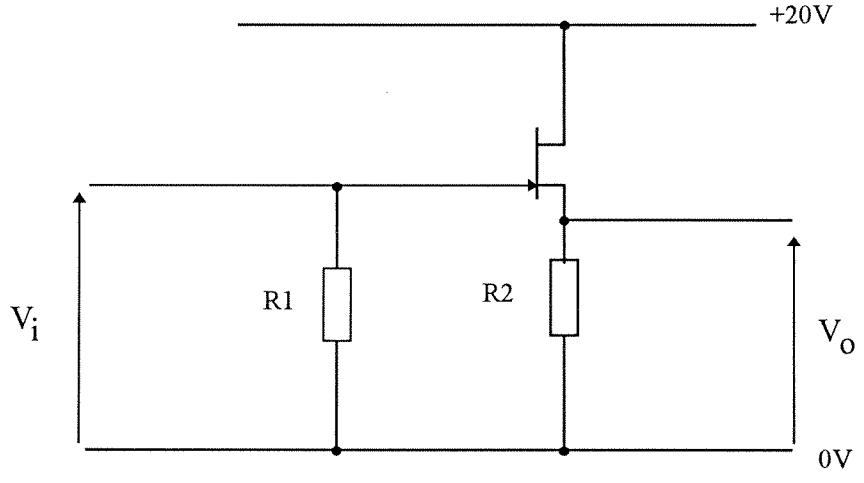

Fig. 2

3 (a) Describe Thevenin's theorem and Norton's theorem. Illustrate these by deriving an equivalent model in each case for the circuit shown in Fig. 3(a).

(b) Calculate the current in the link x-x for the circuit shown in Fig. 3(b).

(c) If a resistor of value 0.5 Ω is connected in place of the link x-x, what current would pass through it and how much power would it dissipate ?

(d) If a resistor of 5 Ω is now connected directly across the ideal current source shown in Fig. 3(b), what is the new value of current passing through the 0.5 Ω resistor connected in x-x ?

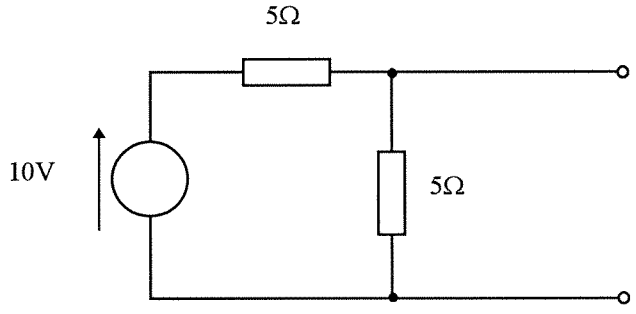

Fig. 3(a)

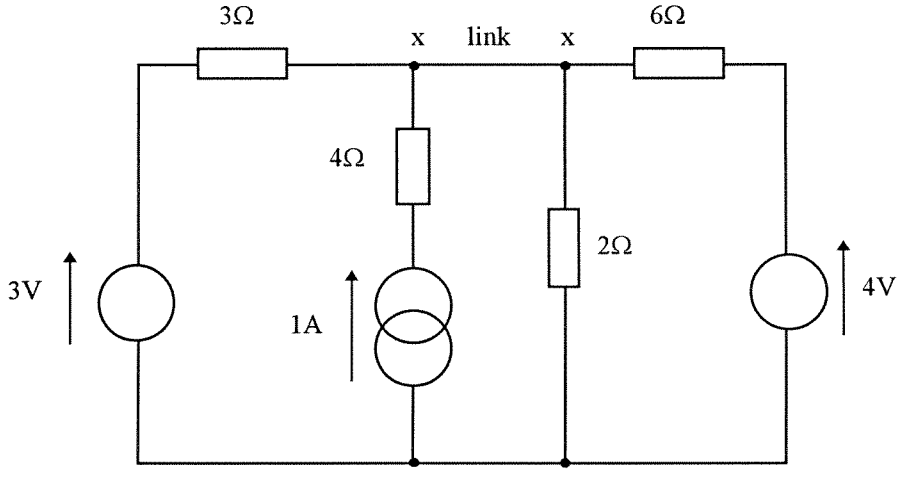

Fig. 3(b)

4 A 240 V, 50 Hz mains transformer is used to drive a load of $10 + j5\ \Omega$ with 30 V rms.

(a) Assuming the transformer is ideal, calculate the turns ratio of the windings and the impedance of the load when referred across to the high voltage (primary) side.

(b) Draw the equivalent circuit of a non-ideal power transformer and briefly explain the physical significance of each of the circuit elements.

(c) The transformer is open circuit tested and short circuit tested to measure its characteristics. The following test results are obtained:-

Open circuit test (low voltage winding open circuit)
$V_{primary} = 240$ V, $I_{primary} = 0.1$ A, $P = 12$ W

Short circuit test (low voltage winding short circuit)
$V_{primary} = 45$ V, $I_{primary} = 3.0$ A, $P = 25$ W

Determine the values of the equivalent circuit elements (referred to the primary, high voltage side) of the transformer.

(d) What is the power factor, current and power drawn from the mains when this transformer is connected to the load ?

(e) Calculate the value of the capacitor required to correct the power factor to unity at the mains.

SECTION B

Answer not more than **three** *questions from this section.*

5 (a) Describe the principles involved in the use of a Karnaugh map in the simplification of a logic function expressed as a *SUM OF PRODUCTS*. Your description should explain the reason for the special order of rows and columns in the Karnaugh map, and why the technique is of such value to the logic designer.

(b) Explain briefly why 2's complement representation is important in information engineering.

(c) An integer number N is expressed as a 4-bit binary number consisting of binary digits X_3, X_2, X_1 and X_0. The 2's complement of N, denoted N^*, may be defined as:

$$N^* = 2^4 - N$$

where N^* is expressed as a four bit code Y_3, Y_2, Y_1, Y_0. X_0 and Y_0 each correspond to the least significant digit of their respective codes.

Write out the truth table that describes how the input X_3, X_2, X_1, X_0 is related to the output code Y_3, Y_2, Y_1, Y_0 for the corresponding 2's complement. Hence by means of Karnaugh maps, devise efficient combinational logic using AND, OR and NOT gates that will convert a four-bit number directly into its corresponding 2's complement form, and draw the logic diagrams for the resulting networks required to implement outputs Y_3, Y_2 and Y_1 only.

(d) What problems are liable to occur with practical realisations of your solution, and how may they be cured?

6 (a) Explain how two NAND gates may be connected to form a simple bistable circuit. How could you use this circuit to eliminate the effects of contact bounce in a switch supplying an input to a logic circuit ?

(b) The state sequence for a particular form of binary coded decimal counter is shown in Table 1. The counter is to be implemented using four J-K bistables with outputs Q_A, Q_B, Q_C and Q_D. Construct a table in which each row shows the present state, the next state, and the J and K inputs required for each of the bistables. Using Karnaugh maps where necessary, determine simplified expressions for the inputs J_B, K_B, J_C and K_C, assuming that unused states do not occur.

(c) Explain carefully what happens if the counter takes up the state 1111 at the moment of switch-on. You may assume that inputs J_A, K_A, J_D and K_D are driven as shown below.

$J_A = Q_B.Q_C.Q_D$ $\qquad$ $K_A = Q_B$

$J_D = 1$ $\qquad$ $K_D = 1$

Q_A	Q_B	Q_C	Q_D
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0

Table 1

7 (a) The circuit in Fig. 4 shows a simple form of 4-bit digital-to-analogue converter. Briefly explain the principle of operation, and describe the nature of the circuitry that must be connected to the inputs S_0 - S_3. Which of these inputs represents the least significant bit?

(b) If the value of R is 1 kΩ, and the operational amplifier may be assumed to be ideal, determine the input resistance measured at terminals S_1 and S_3. If all four input terminals are connected to a voltage source of 5 V, determine the output voltage V_O.

(c) The circuit of Fig. 5 shows an alternative form of digital-to-analogue converter based upon an R–$2R$ ladder and an ideal operational amplifier. Identify the least significant bit in this design. Assuming R = 1 kΩ, determine the input resistance measured at terminals S_1 and S_3. Find the value of R_F required such that when all four inputs are connected to 5 V sources, the output voltage is the same as for the converter of Fig. 4.

(d) What are the advantages of the R–$2R$ ladder converter compared with the type of circuit shown in Fig. 4 ?

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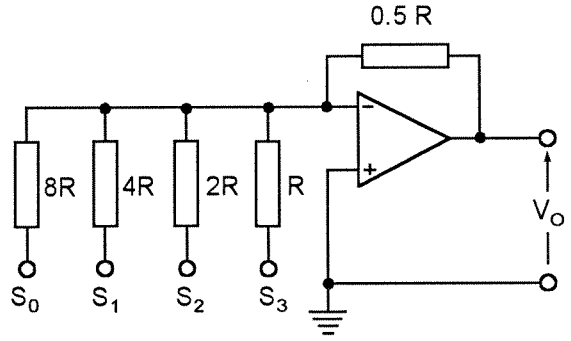

Fig. 4

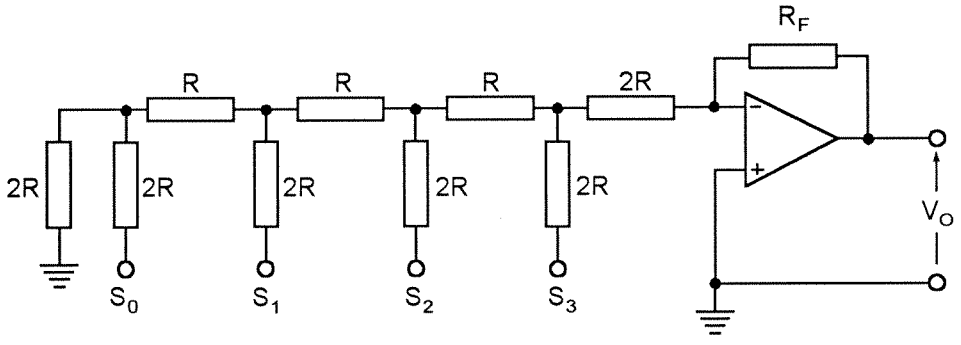

Fig. 5

8 (a) What is meant by a *register* in the context of microprocessor architecture? Explain briefly the functions of the various registers available to the programmer in the 6800 microprocessor.

(b) In a 6800 microprocessor, accumulator A contains hexadecimal 7F, accumulator B contains hexadecimal 81 and the condition code register flags are initially unset. Determine how the contents of the accumulators and flags N, Z and C are affected by the execution of each of the following machine instructions:

(i) ASLB

(ii) ABA

(iii) INCA

(c) Figure 6 shows part of a circuit intended to ensure that the $\overline{RESET}$ input of a 6800-based system is held low (less than 2.5 V) for a period of at least 10 ms after the 5 V power supply is switched on. Logic gate A is an inverter which includes a Schmitt trigger, and has the characteristic shown in Fig. 6. Explain the principle of operation of the circuit and sketch the voltages v and v_2 as a function of time after switch S closes. What additional circuitry, if any, is required to connect this unit to the $\overline{RESET}$ pin ? Determine a suitable value for C to achieve the required delay. How would you extend this circuit to include a push-button for resetting the microprocessor without switching off the power supply ?

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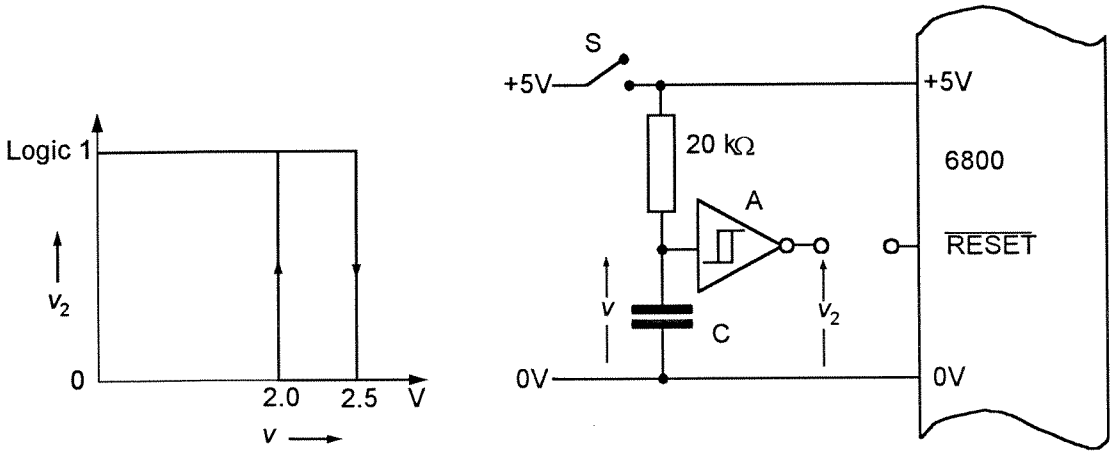

Fig. 6

SECTION C

Answer not more than **two** *questions from this section.*

9 (a) Write down an expression for the electric field E due to an isolated conducting sphere, radius r_S carrying a constant charge Q, as a function of the radial distance r from the centre of the sphere. Hence find the capacitance between the sphere and infinity.

(b) Figure 7 shows the schematic cross section of an inkjet printer in which drops of conducting ink leave the nozzle N at an electrostatic potential V with respect to the casing C and with an exit velocity 4 ms^{-1} in the negative y direction. A constant electrostatic potential difference is applied between the accelerator plates A and B with A 1500 V positive with respect to B.

Describe qualitatively the motion of a drop of ink for the case where it leaves the nozzle with an electrostatic potential of +30 V with respect to C.

(c) Calculate the magnitude of the electrostatic force acting on a droplet of diameter 70 μm while it is passing through the region between the plates A and B.

(d) What is the approximate direction of motion of the drop, with density 1000 kgm^{-3}, after it leaves the region between the plates A and B? How would the direction change if the drop diameter were to be doubled?

Describe briefly why such an inkjet printer is useful for putting the date on eggs.

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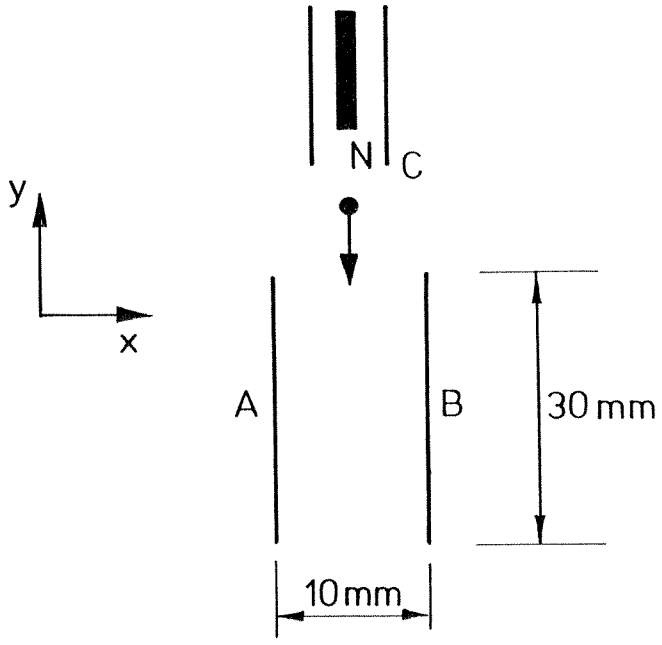

Fig. 7

10 (a) Explain how the method of images can be used for solving electrostatic problems where there is high symmetry.

What is meant by the principle of superposition and when can it be applied?

(b) Consider the two overhead dc power line conductors 3 m apart and 12 m above the ground as sketched in Fig. 8. Both have diameter 0.1 m and both are at potential +300 kV with respect to the ground. By using the method of images, and the principle of superposition or otherwise, estimate the approximate maximum electric field experienced by a person of height 2 m who walks past on the ground underneath the lines well away from any pylons, stating the approximations made.

If the person were to approach a steel pylon tower, explain whether your estimate of the field would be increased, decreased or unchanged.

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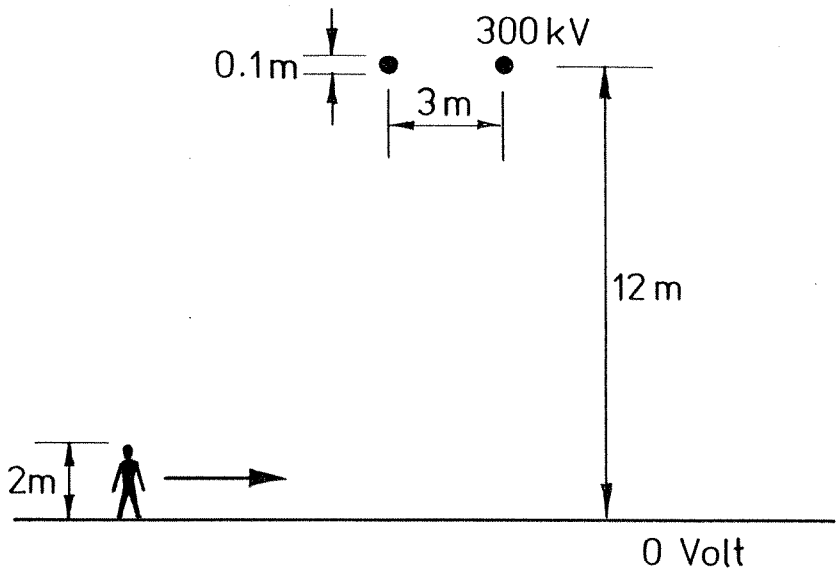

Fig. 8

11 (a) State Ampère's Law in integral form.

(b) Consider the electromagnet in Fig. 9 which has a soft iron core and is holding up a soft iron bar. It is wound with n turns of a wire carrying a dc current I. The length round the loop of magnetic circuit is ℓ. The cross-sectional area is A throughout and the relative permeability of the soft iron is μ_r.

Derive an expression for the magnetic flux density B in the core of the electromagnet, explaining any approximations made.

(c) Use the method of virtual work to calculate the total attractive force acting on the bar, stating the approximations made.

Evaluate the attractive force for the case ℓ = 0.1 m ; n = 80 ; μ_r = 1000 ; I = 0.5 A ; $A = 3 \times 10^{-5}$ m^2.

Estimate the change in force if the current in the wire were to be increased (i) by a factor of two and (ii) by a factor of ten.

Hint: The total magnetostatic energy per unit volume, where the symbols have their usual meanings, is

$$W = \int_0^B H.dB \quad .$$

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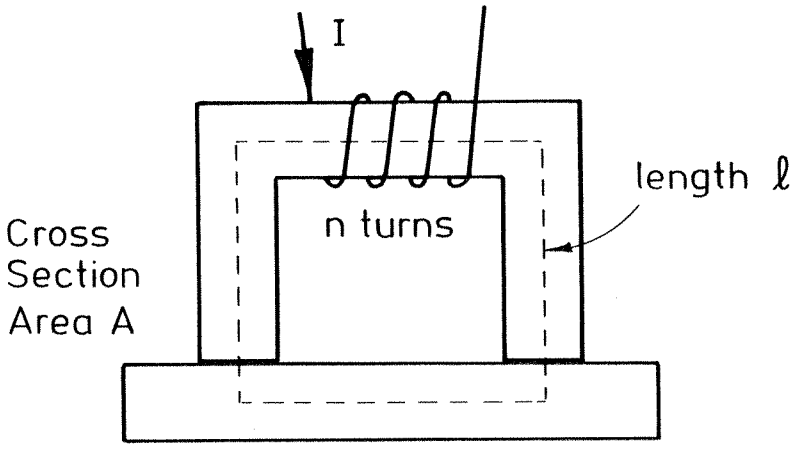

Fig. 9

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