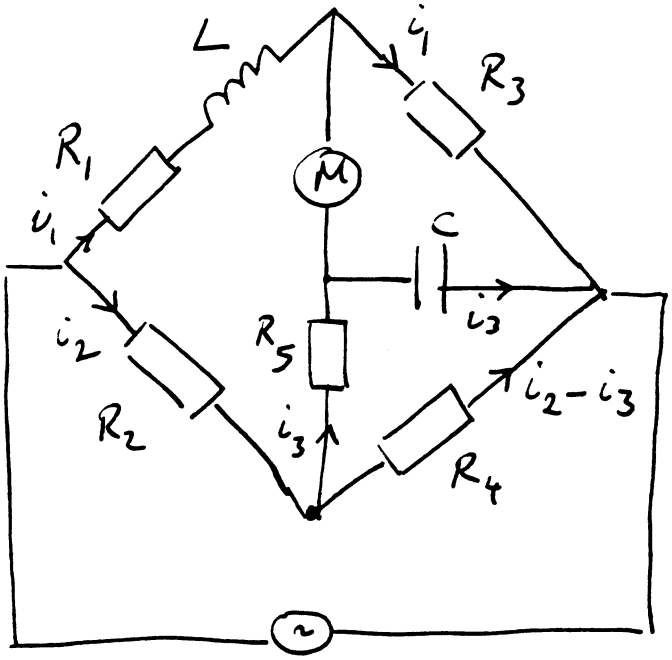
1.



Note analysis more difficult using current loops, but is an alternative metho

Apply KVL:

$$i_1 (R_1 + j\omega L) = i_3 R_5 + i_2 R_2 \qquad (1)$$

$$i_1 R_3 = i_3 \cdot \frac{1}{j\omega C} \qquad (2)$$

$$i_3 \left(R_5 + \frac{1}{j\omega C}\right) = R_4 (i_2 - i_3) \qquad (3)$$

from (2) $\quad i_3 = j\omega C R_3 \cdot i_1$

subst. into (1) and (3)

(1) → $\quad i_1 (R_1 + j\omega L - j\omega C R_3 R_5) = i_2 R_2 \qquad (4)$

(3) → $\quad i_1 \left(R_5 + R_4 + \frac{1}{j\omega C}\right) \cdot j\omega C R_3 = i_2 R_4 \qquad (5)$

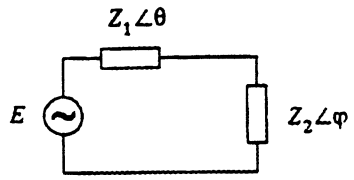
divide and x multiply (4) & (5) to get

$$j\omega C R_2 R_3 \left(R_5 + R_4 + \frac{1}{j\omega C}\right) = R_4 (R_1 + j\omega L - j\omega C R_3$$

equating real and imaginary parts gives

$$R_2 R_3 = R_4 R_4 \quad ; \quad \frac{L}{C} = \frac{R_3}{R_4} (R_2 R_5 + R_2 R_4 + R_4 R_5)$$

2.



(a) The current in the circuit is given by:

$$\tilde{I} = \frac{\tilde{E}}{\tilde{Z}_1 + \tilde{Z}_2} = \frac{\tilde{E}}{Z_1\cos\theta + \mathbf{j}Z_1\sin\theta + Z_2\cos\varphi + \mathbf{j}Z_2\sin\varphi}$$

$$\text{Hence } |\tilde{I}| = \frac{E}{\left(\left(Z_1\cos\theta + Z_2\cos\varphi\right)^2 + \left(Z_1\sin\theta + Z_2\sin\varphi\right)^2\right)^{\frac{1}{2}}}$$

Average Power P is given by $P = I^2R = I^2\,\mathrm{Re}(Z_2) = I^2Z_2\cos\varphi$

$$\text{Hence } P = \frac{E^2Z_2\cos\varphi}{Z_1^2 + Z_2^2 + 2Z_1Z_2\left(\cos\theta\cos\varphi + \sin\theta\sin\varphi\right)}$$

$$= \underline{\frac{E^2Z_2\cos\varphi}{Z_1^2 + Z_2^2 + 2Z_1Z_2\cos(\theta - \varphi)}}$$

Note that there is no factor of ½ here, because rms values are always used in electrical power problems.

(b) To find the maximum power as a function of Z_2, differentiate P with respect to Z_2 and set equal to zero.

$$\text{Thus } \frac{dP}{dZ_2} = E^2\left(\frac{\cos\varphi}{X} - \frac{Z_2\cos\varphi}{X^2}\left(2Z_2 + 2Z_1\cos\left(\theta - \varphi\right)\right)\right) = 0$$

where $X = Z_1^2 + Z_2^2 + 2Z_1Z_2\cos\left(\theta - \varphi\right)$

$$\text{Hence } \left(Z_1^2 + Z_2^2 + 2Z_1Z_2\cos\left(\theta - \varphi\right)\right)\cos\varphi - Z_2\cos\varphi\left(2Z_2 + 2Z_1\cos\left(\theta - \varphi\right)\right) = 0$$

and thus: $\left(Z_1^2 - Z_2^2\right)\cos\varphi = 0$ giving $\underline{Z_1 = Z_2}$.

Note that if $\varphi = \pi/2$ there is also a turning point. This actually corresponds to a minimum in P as a function of φ. Physically, this is because if $\varphi = \pi/2$, the load impedance is purely reactive and the average load power must as a result be zero.

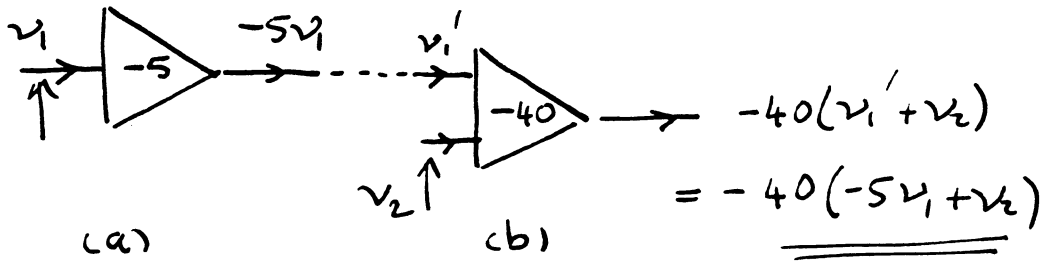
3/. First part – standard book work.

Given $v_1 = 10mV$, $v_2 = 50mV$, both $R_s = 20\Omega$.
Required output $v_{out} = 200v_1 - 40v_2$.

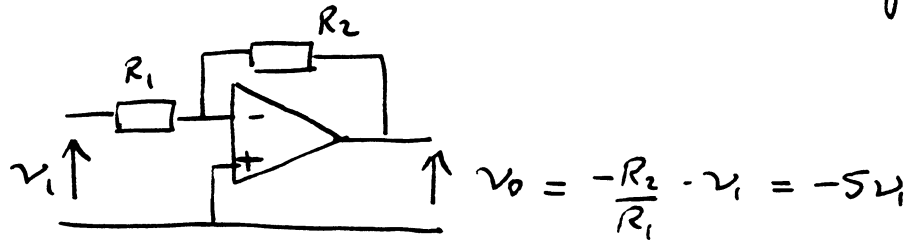
We can write v_{out} as follows:

$$v_{out} = 40\,(5v_1 - v_2)$$

This form for v_{out} suggests we need <u>two</u> amplifiers, configured as follows:



For amplifier (a) we use an inverting amplifier

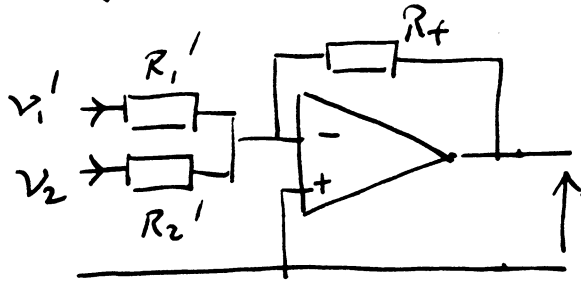


Need $R_2 / R_1 = 5$

Source resistance $R_s = 20\Omega$, so need $R_1 \gg 20\Omega$, so choose $R_1 = 10k\Omega$, giving $R_2 = 50k\Omega$.

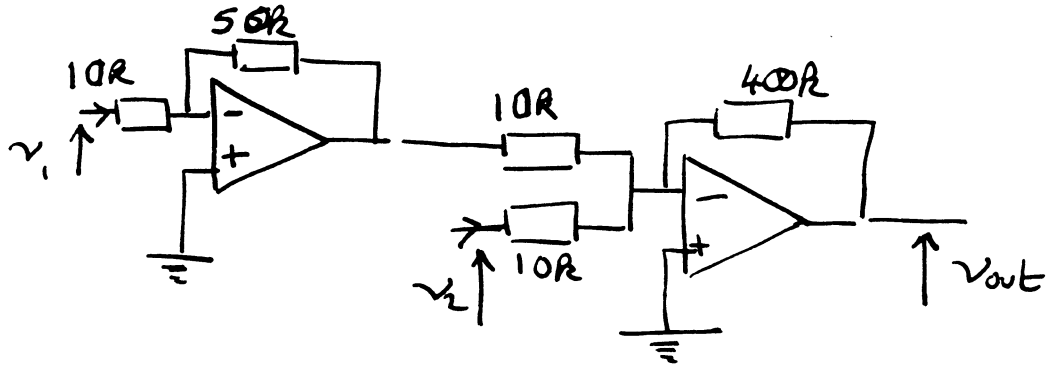
3/ (cont)

For amplifier (b) we need a summing amplifier with gain −40.



We require $R_f/R_1' = R_f/R_2' = 40$.
Again, R_s for $v_2 = 20\Omega$, so choose $R_1' = R_2' = 10k\Omega$
This gives $R_f = 400k\Omega$.

Final circuit:



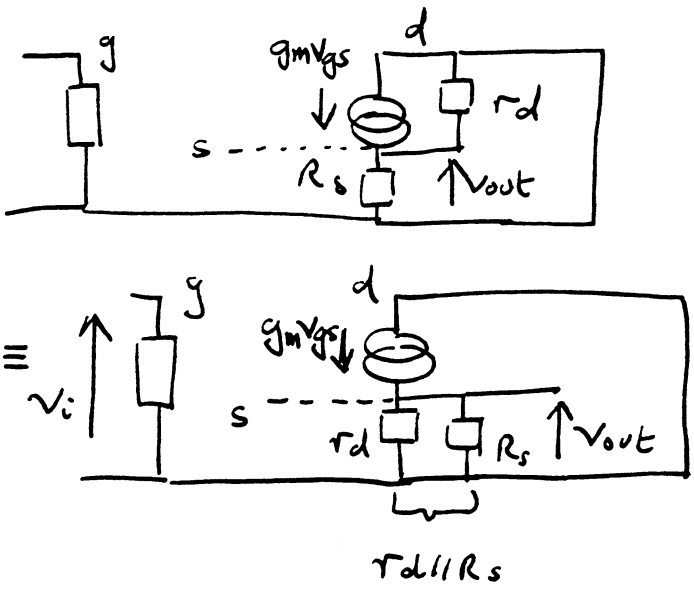
Maximum output voltage is

$$|V_{out}| = 200|v_1| + 40|v_2|$$

$$= 4 \text{ Volts}.$$

∴ Need a power supply voltage > 4 Volts.

4. (a) Small signal circuit can be drawn as:



$$\frac{V_{out}}{r_d // R_s} = g_m V_{gs}$$

$$V_i = V_{gs} + V_{out}$$

$$\therefore \frac{V_{out}}{r_d // R_s} = g_M (V_i - V_{out})$$

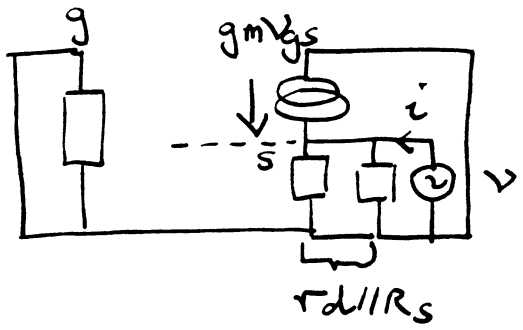
$$\therefore \frac{V_{out}}{V_i} = \frac{g_m r_d // R_s}{1 + g_m r_d // R_s}$$

$g_m = 4 \times 10^{-3}$, $r_d = 10^3$, $R_s = 4.7 \times 10^3$

$$\therefore \boxed{\frac{V_{out}}{V_{in}} = 0.93}$$

For R_{out} we s/c input, apply signal at output. Equivalent circuit becomes

4 (cont.)



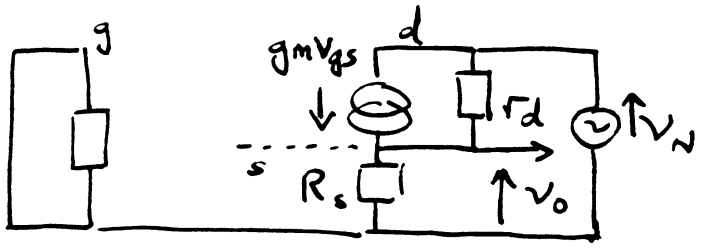
$$v = -v_{gs}$$

$$i = \frac{v}{r_d // R_s} - g_m v_{gs}$$

$$\therefore R_{out} = \frac{v}{i} = \frac{r_d // R_s}{1 + g_m r_d // R_s}$$

$$\boxed{R_{out} = 232\,\Omega}$$

(b) We want the contribution to the output made by the noise source v_N. Use superposition, with v_i s/c. Equivalent circuit:



$$v_o = -v_{gs} \qquad (1)$$

$$\frac{v_o}{R_s} = g_m v_{gs} + \frac{(v_N - v_o)}{r_d} \qquad (2)$$

from (1), (2) $\quad v_o = \dfrac{v_N}{r_d\left(\frac{1}{r_d} + \frac{1}{R_s} + g_m\right)} < 20 \times 10^{-6}$

$$\therefore \boxed{v_N < \text{max. } 0.86\,mV}$$

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(40)

5. Main points:

- In combinational logic, the state of the outputs is governed only by the present state of the inputs.
- In sequential logic, the state of the outputs is affected not only by the present state of the inputs, but also by their previous states
- Sequential logic typically contains bistables or memory elements in which 'states' or 'results' can be stored.
- Sequential logic can often be created by rearranging the connections to combinational logic in such a way as to cause *feedback*.

Construct a truth table ..

Input				Output
D	C	B	A	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

Input				Output
D	C	B	A	Y
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

.. and map the expression:-

BA / DC	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	1	1	0	1
10	1	1	1	1

For the NAND solution, encircle groups of 1s (or 0s), as shown, to deduce the minimum number of terms. Considering the 1s we get the expression:-

$Y = D.\overline{C} + D.\overline{B} + D.\overline{A} + \overline{D}.C.B$ which satisfies the requirements,

Note that no attempt has yet been made to eliminate static hazards. This can then be simplified:-

$Y = D.(\overline{C} + \overline{B} + \overline{A}) + D.C.B$ and rewritten using De Morgan:-

$Y = \overline{\overline{D.\overline{C}}.\overline{D.\overline{B}}.\overline{D.\overline{A}}.\overline{\overline{D}.C.B}}$, using two, three and four input NANDs.

For the NOR solution, we considering the encircled 0s (to get $\overline{Y}$), and apply De Morgan to the result:-

$$\overline{Y} = \overline{C}.\overline{D} + \overline{B}.\overline{D} + A.B.C.D = \left(\overline{D+C}\right) + \left(\overline{B+D}\right) + \left(\overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}\right)$$

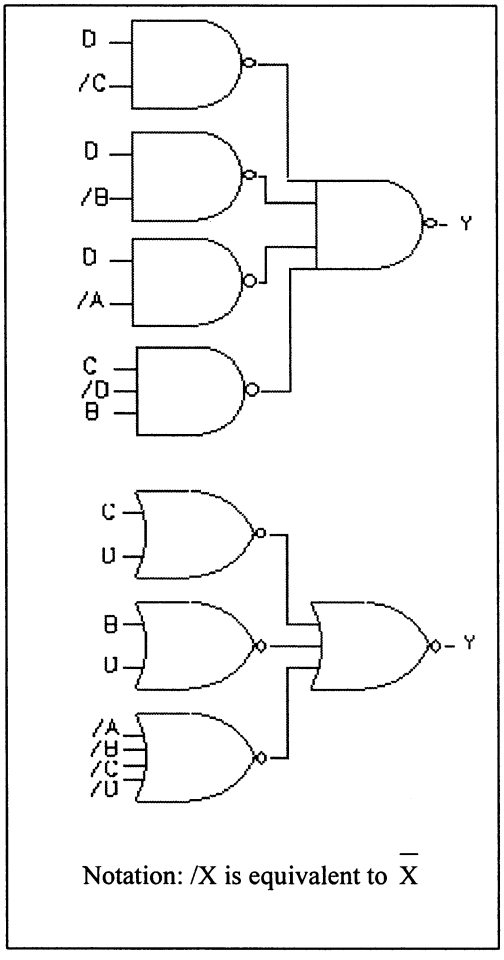
Hence we get:-

$Y = \overline{\overline{D+C} + \overline{B+D} + \overline{\overline{A}+\overline{B}+\overline{C}+\overline{D}}}$, using two, three and four-input NOR gates.

Static hazards can be detected in the Karnaugh map by identifying regions which touch but do not intersect. They can be overcome by summing additional product terms which intersect the touching region or regions. In the present case, the additional term $C.B.\overline{A}$ can be incorporated to counter the static hazard arising from touching terms $\overline{D}.C.B$ and $D.\overline{A}$.

The Karnaugh map technique is effective for minimising Sum of Product expressions, provided:-

- both 1s and 0s are considered when drawing loops;
- only a single output is required.



Notation: /X is equivalent to $\overline{X}$

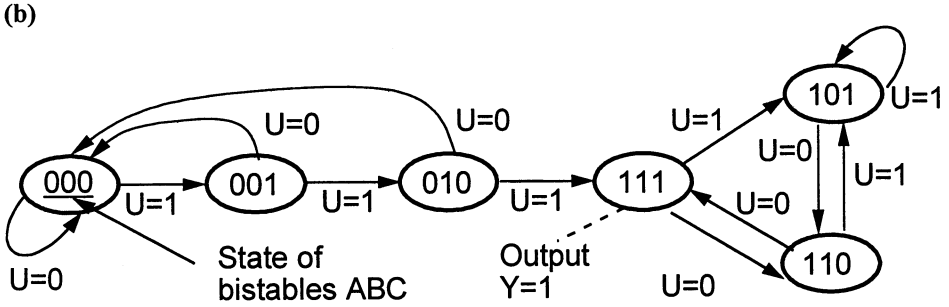
There is no simple way of identifying the economies that might arise if more than one output is to be generated, some of which may be able to share common terms. Also, it may be possible to find a more economical solution using fewer *packages* in ways not directly deduced from the map - for example, cells which are adjacent along a diagonal are related by the XOR of two input variables; use of an XOR gate can thus offer possible economies.

6 (a) The six states are:-

```
000   Initial state.  No U=1 has been received, i.e. U=0 repeatedly
001   A single U=1 has been received
010   A 2nd occurrence of U=1 has been received
111   *A 3rd occurrence of U=1 has been received forming the triple; output Y=1
110   Since the triple or the last U=1 following it, U=0 has been received
101   Since the triple or the last U=1 following it, U=1 has been received
111   *Since the triple an even number of 0s has been received, output Y=1
```

* Both definitions for the state 111 hold at different times.

(b)



Note that each state has two arrows leaving it, one corresponding to U=0, the other to U=1.

(c)

Present state				Next state				Required J-K inputs					
U	A	B	C	A	B	C	Y	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	0	0	0	X	0	X	0	X
1	0	0	0	0	0	1	0	0	X	0	X	1	X
0	0	0	1	0	0	0	0	0	X	0	X	X	1
1	0	0	1	0	1	0	0	0	X	1	X	X	1
0	0	1	0	0	0	0	0	0	X	X	1	0	X
1	0	1	0	1	1	1	0	1	X	X	0	1	X
0	1	1	1	1	1	0	1	X	0	X	0	X	1
1	1	1	1	1	0	1	1	X	0	X	1	X	0
0	1	1	0	1	1	1	0	X	0	X	0	1	X
1	1	1	0	1	0	1	0	X	0	X	1	1	X
0	1	0	1	1	1	0	0	X	0	1	X	X	0
1	1	0	1	1	0	1	0	X	0	0	X	X	0

J_B and K_B

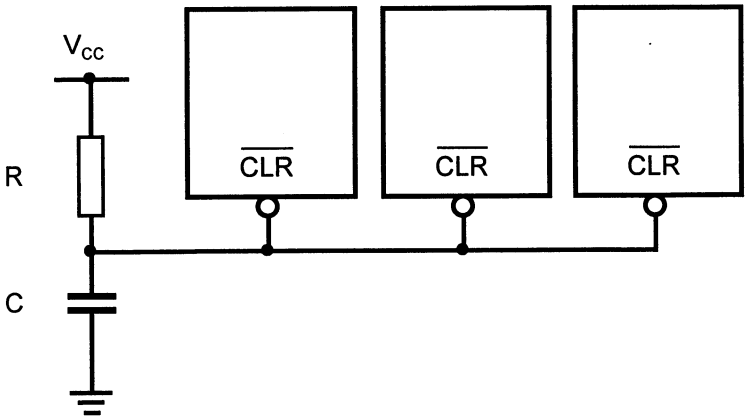
BC / UA	00	01	11	10
00	0	0	X	X
01	X	1	X	X
11	X	0	X	X
10	0	1	X	X

BC / UA	00	01	11	10
00	X	X	X	1
01	X	X	0	0
11	X	X	1	1
10	X	X	X	X

Hence $J_B = A\overline{U} + \overline{A}UC$ $\qquad$ $K_B = \overline{AU} + AU$

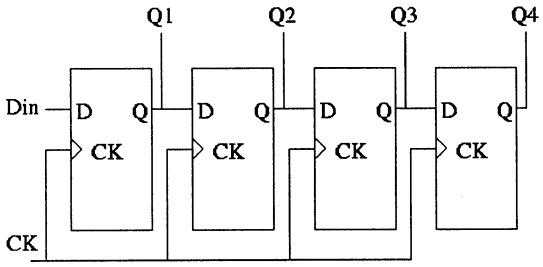
(d) First and foremost, this is a *clocked* synchronous system, so there should be no risk of static hazards on these grounds alone. Moreover, there are no abutting loops evident in these Karnaugh maps.

6 (e)



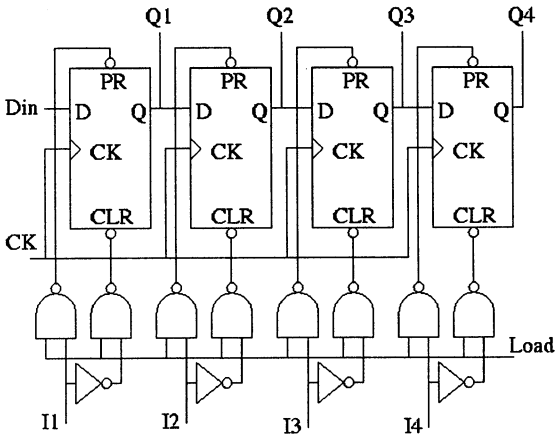
With this arrangement, at the moment the power is switched on, C is discharged, applying logic LOW to the three CLR inputs. C will charge to approximately 63% of the supply voltage V_{CC} after an interval RC seconds, and will continue to rise towards V_{CC}. Until this happens, the three bistables will be held in the cleared state with output Q=0. After the charge-up period, the CLR pins return HIGH and the Q outputs are free to change under influence of J, K and CLK.

7 (a)



A shift register is an assembly of D-type bistable devices in which the Q output of each stage is connected to the D input of the next stage. All clock inputs are driven simultaneously so that at each clock pulse, data contained in the register is 'shifted' one place.

The leftmost input may be driven with a series of ones and noughts at Din, synchronised to the clock. These will be presented in sequence at the successive Q outputs as the clock is toggled. This gives a means of converting serial data to parallel.



To convert parallel data to serial form, a means is required for *parallel loading* binary data into the bistable elements independent of the clock. This can be done by use of the Preset (PR) and Clear (CLR) inputs, controlled by NAND gates driven with a **Load** signal. When **Load** is taken to logic HIGH, signal I1 will cause the Preset and Clear signals to drive the Q output in the corresponding bistable 1 to the same state (as I1).

The rest of the signals I2, I3, .. control their corresponding bistables in a similar way. **Load** is then taken to logic LOW, so setting all Preset and Clear signals to logic HIGH (so they cannot affect the Q outputs), and the clock signal is pulsed. Data appears at Q4 as each clock pulse is applied, in reverse order, i.e. I4, I3, I2, I1. Q4 may thus be regarded as a *Serial Out* terminal. If eight stages (1-8) are concatenated in a similar way, an 8-bit parallel input (I1-I8) can be converted to serial data (at Q8), the data arriving in the sequence: I8, I7, I6, .. I1.

J-K bistables may be used instead. The Q output of each stage is taken to the following J, and Qbar to the following K. An inverter may be needed for the first stage.

7 (b). Twos complement representation is based on the idea that "adding the twos complement of a number" is equivalent to subtracting that number. In this system, negative numbers are indicated by binary numbers with the MSB set to 1; positive numbers have the MSB set to 0.

It is important in information processing because it means computers can add and subtract using the same hardware.

The largest positive 8-bit number is $0111\ 1111 = 127_{10}$
The largest negative (most negative) number is $1000\ 0000 = -128_{10}$

Using the method of successively dividing by 2 and tabulating the remainders we have:-

2	47_{10}	$= 0010\ 1111_2$
2	23 r 1	
2	11 r 1	
2	5 r 1	
2	2 r 1	
2	1 r 0	
	0 r 1	

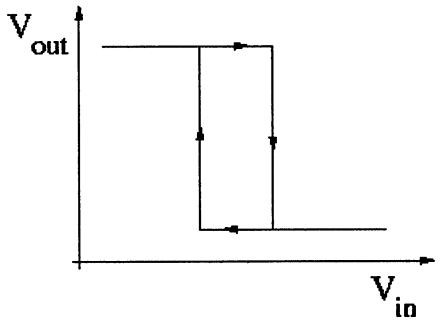
2	$+89_{10}$	$= 0101\ 1001_2$
2	44 r 1	To get -89_{10}
2	22 r 0	Form 2s complement
2	11 r 0	Negate each bit
2	5 r 1	$= 1010\ 0110$
2	2 r 1	Then add 1
2	1 r 0	$1010\ 0110$
2	0 r 1	$+0000\ 0001$
		$1010\ 0111 = -89_{10}$

2	68_{10}	$= 0100\ 0100_2$
2	34 r 0	
2	17 r 0	
2	8 r 1	
2	4 r 0	
2	2 r 0	
2	1 r 0	
2	0 r 1	

$0010\ 1111 = 47_{10}$
$1010\ 0111 = -89_{10}$
$0100\ 0100 = 68_{10}$
$(1)0001\ 1010 = +26_{10}$

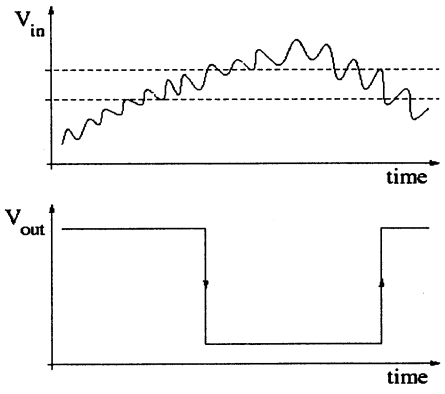
NB: this operation may give a result with fewer than 8 bits shown; leading zeros have been added where appropriate.

(c)



A Schmitt trigger is a form of comparator for which the reference level (at which switching happens) depends upon whether the input is rising or falling. This can be achieved by applying a small amount of positive feedback between the output of the device and its input.

The difference between the two switching levels is known as the *hysteresis*.



The diagram shows a typical input and output for a Schmitt trigger fed with a slowly changing, noisy signal. The Schmitt hysteresis ensures that only one transition occurs at the output as V_{IN} passes through the switching level, provided the superimposed noise is less in amplitude than the hysteresis.

Such slowly varying, noisy signals cannot safely be applied to logic gate inputs without spurious switching being observed. Logic gates with inbuilt hysteresis are available for such situations, e.g. Schmitt inverter 7414, etc.

8 (a). In microprocessors, memory-mapped I/O refers to the methods by which the programmer can control input and output of data between external devices and the microprocessor. In memory-mapped I/O, the external devices are connected via the data, address and control bus. Appropriate decoding of the address bus is arranged so that the devices appear as memory locations, data being transferred into the microprocessor by means of memory READ (or LOAD) instructions, and from the microprocessor to the device(s) by means of WRITE (or STORE) instructions.

Hence in the 6800, the basic instructions are:-

```
LDA A  or  LDA B        to input from a device to accumulator A or B
STA A  or  STA B        to output from accumulator A or B to the device.
```

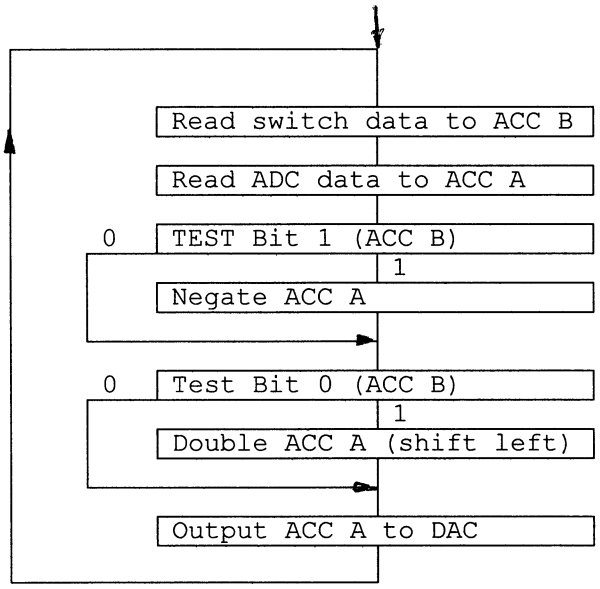
The address used must resolved to the port address defined for the device.
Other instructions may be used, provided their addressing modes are consistent. Thus: `ADD A` could be used to ADD the data input from the device to the value currently held in the accumulator A.

(b) Use register ACC A to load and manipulate the signal, as recommended. Use register ACC B to load and test the switches (bits 0 & 1). A repeating loop is required to inspect the switches and manipulate the data.

00H corresponds to 0.00 V
64H corresponds to +1.00 V
7FH corresponds to +1.27 V

FFH corresponds to –0.01 V.

80H corresponds to –1.28 V



Label	Mnemonic code	Cycles
start:	LDAB #F000	4
	LDAA #F000	4
	BITB 1	2
	BEQ test1:	4
	NEG A	2
test1:	BITB 2	2
	BEQ out:	4
	ASLA	2
out:	STAA #F001	4
	JMP start:	3
		31

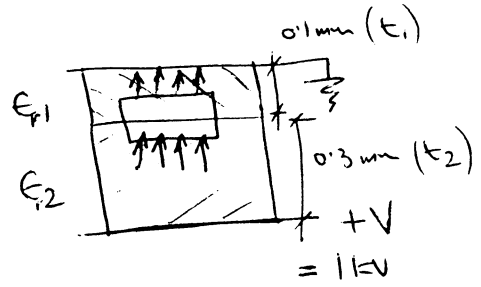
Note that alternative solutions exist, and that these would be expected to require different instruction sequences and hence different execution times. For example, a logical instruction ANDB or a compare instruction CMPB might alternatively be used to identify the state of the switches.

Arithmetic results must remain correctly within 8 bits if the values output are not to be in error. Since the output may swing between decimal -128 and +127, and since a multiply by two may be required, the input codes must lie within the range -64 to +63. These correspond to voltages of -0.64 and +0.635.

Time taken for program to execute = $31 \times \frac{1}{8 \times 10^6} s$. Hence number of samples/s = $\frac{8 \times 10^6}{31} = 258{,}000$.

9 a) Gauss' law states that the integral of the electric flux over a closed surface is equal to the charge enclosed within that surface. If there is no charge enclosed then the net flux in = flux out.

b)



from Gauss' law, flux in = flux out

$$\epsilon_{r_2} E_2 = \epsilon_{r_1} E_1$$

$$\therefore 5E_2 = 3E_1$$

$$\therefore E_1 = \frac{5}{3} E_2 \quad \text{also} \quad 0.1\times10^{-3} \times E_1 + 0.3\times10^{-3} E_2 = 1000V$$

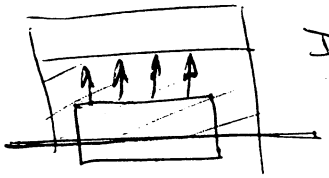
(flux voltage drop = field × thickness)

$$\therefore 1000 = \frac{5}{3} E_2 . 10^{-4} + E_2 . 3\times10^{-4} \quad \therefore \quad E_2 = 2.17\times10^{6}\ V/m$$

$$E_1 = 3.48\times10^{6}\ V/m$$

Hence, potential of interface $= E_1 t_1 = 348\ V$.

c)



$D_2 = \epsilon_{r_2} \epsilon_0 E_2$

charge Q / unit area

Gauss' law and $Q = D_2 = 5 . 8854\times10^{-12} . 2.17\times10^{6}$

$= CV = C . 1000$

$\therefore C = 96\ nf/m^2$

Assumptions:-
- no edge effects ie: all flux lines parallel
- no air gap between paper or dielectrics
- paper considered a conductor

d) For force on paper, use virtual work:-

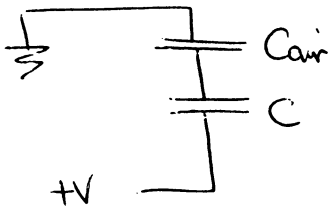
Energy stored, $E = \frac{1}{2} CV^2$

$$P\,\delta x = \tfrac{1}{2} V^2\, \delta C$$

$$\therefore P = \tfrac{1}{2} V^2 \frac{dC}{dx}$$

(continued).

Consider:- 2 capacitors in series



$C_{air} = \epsilon_0 / \delta x$

$$\therefore C_{total} = \left(\frac{1}{C_{air}} + \frac{1}{C}\right)^{-1} = C\left(C/C_{air} + 1\right)^{-1}$$

with C_{air} large (ie: δx is small) $\quad C_{total} \simeq C\left(1 - C/C_{air}\right)$

with $\delta C = C - C_{tot} = C^2/C_{air} = \dfrac{C^2 \delta x}{\epsilon_0}$

$$\therefore P = \tfrac{1}{2} V^2 \frac{dC}{dx} = \frac{\tfrac{1}{2} V^2 C^2}{\epsilon_0}$$

---

with $V = 10^3$ V
$C = 96$ nF/m^2
$\epsilon_0 = 8.854 \times 10^{-12}$ F/m

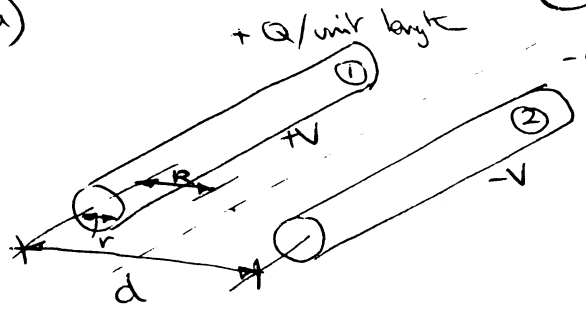
$P = 5.2$ kN/m^2

ie; 5% of an atmosphere

- a substantial pressure.

(47) cV potential midway

10 a)



Apply ±Q to conductors, voltage p.d. of 2V appears between them.

Gauss' Law $Q = 2\pi R D$

$= 2\pi R \varepsilon_0 E$ for conductor ① and by superposition from ② :-

$$\therefore \text{ total } E(r) = \frac{Q}{2\pi R \varepsilon_0} + \frac{Q}{2\pi (d-R)\varepsilon_0} \qquad \text{where } E = \frac{-dV}{dR}$$

$$\therefore \quad V = \frac{-Q}{2\pi\varepsilon_0} \int_{d/2}^{r} \frac{1}{R} + \frac{1}{d-R}\, dR$$

$$V = \frac{-Q}{2\pi\varepsilon_0} \left[\ln[R/d-R] \right]_{d/2}^{r} = \frac{-Q}{2\pi\varepsilon_0} \left[\ln\frac{r}{(d-r)} - \cancel{\ln\frac{d/2}{d/2}}^{\,0} \right]$$

and $Q = CV$, $V = \frac{+Q}{2\pi\varepsilon_0} \ln\left(\frac{d-r}{r}\right)$ $\therefore C = \frac{\pi\varepsilon_0}{\ln\left(\frac{d-r}{r}\right)}$

(as 2V is voltage across conductors)

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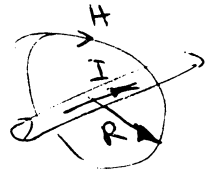
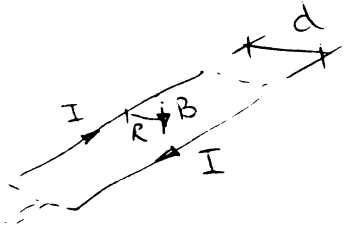
b) Ampere's law $\int \underline{H}.d\underline{L} = \int \underline{J}.d\underline{S} = N\underline{I}$



$2\pi R H = I$ and $B = \mu_0 H$

$$\therefore B = \frac{\mu_0 I}{2\pi R}$$

c)



$$B(R) = \frac{\mu_0 I}{2\pi R} + \frac{\mu_0 I}{2\pi (d-R)}$$ includes contribution from both by superposition.

$$\therefore \text{ flux linked/unit length} = \frac{\mu_0 I}{2\pi} \int_{r}^{d-r} \frac{1}{R} + \frac{1}{(d-R)}\, dR = \phi$$

$$= \frac{\mu_0 I}{2\pi} \left[\ln\frac{d-r}{r} - \ln\frac{r}{d-r} \right] = \frac{\mu_0 I}{\pi} \ln\left(\frac{d-r}{r}\right)$$

2c cont'd.
10c

Since $\Phi = LI$ $\therefore$ $L = \frac{\mu_0}{\pi} \ln\left(\frac{d-r}{r}\right)$

Approximations:
- neglect end effects i.e. wire ∞ long
- no flux coupled within conductor width

d) $L = \frac{\mu_0}{\pi} \ln\left(\frac{d-r}{r}\right)$, $C = \frac{\pi \epsilon_0}{\ln\left(\frac{d-r}{r}\right)}$

$\therefore \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} = 3 \times 10^8$ m/s $= c$ (speed of light). !

11 a) $\int H \cdot dL = \int J \cdot dS$ = current enclosed

or amp. turns = Σ H × length of path around magnetic circuit.

b) $NI = H_{steel}\,l + H_{air}\,[(r_2 - r_1) + x]$

$B_{steel} = \mu_0 \mu_r H_{steel}$ $\qquad g = r_2 - r_1$

$B_{air} = \mu_0 H_{air}$

and $B_{steel} = B_{air}$ $\therefore H_{steel} = H_{air}/\mu_r$ (flux conservation, A_{steel} area const A)

$\therefore NI = H_{air}\frac{L}{\mu_r} + H_{air}(g + x)$

$\therefore B_{air} = \frac{\mu_0 NI}{(L/\mu_r + g + x)}$ (0.25 T ✓)

c) now $\phi = BA$ & and $L = \frac{N\phi}{I}$

$\therefore L = \frac{\mu_0 N^2 A}{(L/\mu_r + g + x)}$

$= 2.04$ mH

$N = 300$
$A = 0.5 \times 10^{-4}$ m²
$g = 0.2 \times 10^{-3}$ m
$\mu_r = 1500$
$L = 50 \times 10^{-3}$ m
$x = 10^{-3}$ m

d) Energy stored $= \frac{1}{2} L I^2$

$\therefore$ by virtual work $F \cdot \delta x = \frac{1}{2} I^2 \delta L$

$L = \frac{\mu_0 N^2 A}{(L/\mu_r + g + x)}$ $\qquad \frac{\delta L}{\delta x} = -\frac{\mu_0 N^2 A}{(L/\mu_r + g + x)^2}$

~~*Bd cont~~ $\therefore F = -\frac{1}{2} I^2 \frac{L^2}{\mu_0 N^2 A} = \frac{-\frac{1}{2} I^2 \mu_0 N^2 A}{(\frac{L}{\mu_r} + g + x)^2}$

$\therefore F = \frac{-\frac{1}{2} 1.2^2 \mu_0 200^2 0.5\times10^{-4}}{(0.203\times10^{-3})^2} = 1.25\ N$

c). solve. into b) to find $B = 0.25\ T$ (linear)
with $I = 1.2A$

but will sat. @ 1.6T for $I \approx 10A$
$\therefore$ force will only go up by
$\times 5$ times.