ENGINEERING TRIPOS PART IA

Tuesday 9 June 1998 9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

*Answer not more than* **eight** *questions, of which not more than* **three** *may be taken from Section A, not more than* **three** *from Section B, and not more than* **two** *from Section C.*

*The* **approximate** *number of marks allocated to each part of a question is indicated in the right margin.*

*Answers to questions in each section should be tied together and handed in separately.*

**(TURN OVER**

SECTION A

*Answer not more than* **three** *questions from this section.*

1 Explain briefly how the techniques of *mesh current analysis* and *loop current analysis* are used in the analysis of d.c. and a.c. electrical circuits. [3]

Figure 1 shows the circuit for an a.c. bridge. At balance the voltage across the detector $M$ is zero. Under these circumstances show that three independent currents are needed to describe the behaviour of the circuit. [3]

Show that the conditions for achieving balance are

$$R_1 R_4 = R_2 R_3$$

and

$$\frac{L}{C} = \frac{R_3}{R_4} \cdot \left( R_2 R_4 + R_2 R_5 + R_4 R_5 \right)$$ [12]

Explain briefly the interpretation of each of these equations. [2]

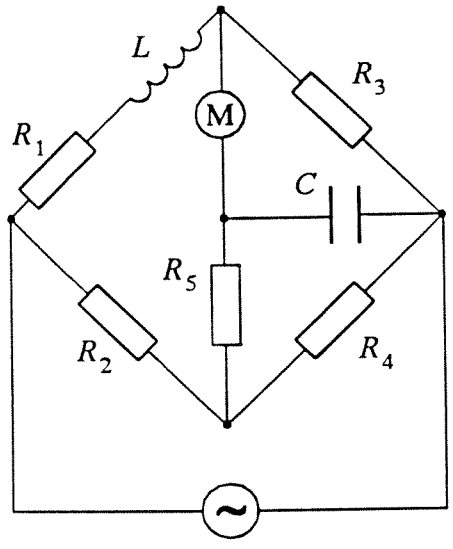


Fig. 1

2 An a.c. generator of r.m.s. voltage $E$ and internal impedance $Z_1\angle\theta$ is connected to a load of impedance $Z_2\angle\varphi$, as shown in Fig. 2.

(a) Show that the average power dissipated in the load is given by

$$P = \frac{E^2 Z_2 \cos\varphi}{Z_1^2 + Z_2^2 + 2Z_1 Z_2 \cos\ (\theta - \varphi)} \qquad [5]$$

(b) The phase $\varphi$ of the load is held constant, and the magnitude $Z_2$ of the load is varied. Show that the condition for maximum power to be transferred to the load is

$$Z_2 = Z_1 \qquad [6]$$

(c) The magnitude $Z_2$ of the load is kept constant, but the phase $\varphi$ is varied. Show that the condition for maximum power to be transferred to the load is now

$$\sin\varphi = -\frac{2Z_1 Z_2}{Z_1^2 + Z_2^2} \cdot \sin\theta \qquad [6]$$

(d) Using the results from (b) and (c), or otherwise, show that if the magnitude and phase of the load are both varied, then the condition for maximum power to be transferred to the load is

$$Z_2\angle\varphi = Z_1\angle -\theta \qquad [3]$$

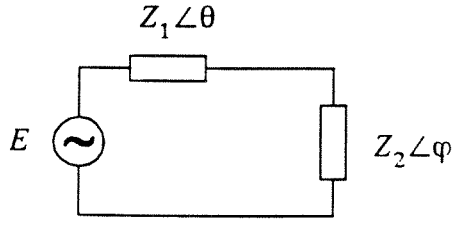


Fig. 2

3 Figure 3 shows the circuit for a summing amplifier. Assuming that the op-amp is ideal, show that $v_{out}$ is given by

$$v_{out} = -\left(\frac{R_f}{R_1} \cdot v_1 + \frac{R_f}{R_2} \cdot v_2\right) \qquad [5]$$

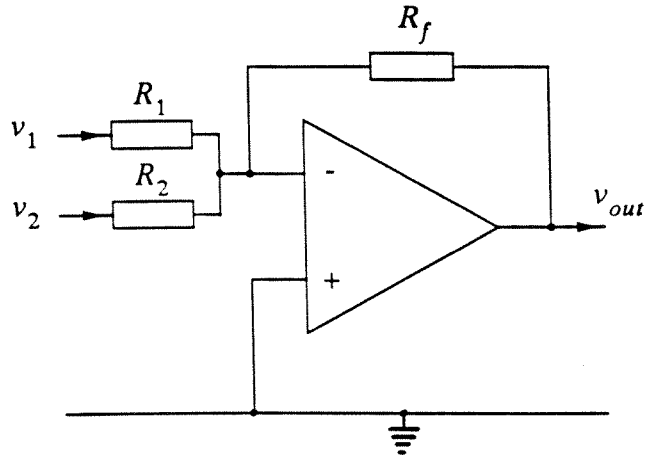


Fig. 3

Two signal sources, $v_1$ and $v_2$ , each have an output resistance of 20 Ω. Design a circuit that uses two op-amps to produce an output of $200\ v_1 - 40\ v_2$. If $v_1$ = 10 mV and $v_2$ = 50 mV, comment on the power supply voltage needed for your circuit. [15]

4 Figure 4(a) shows the circuit for a source follower amplifier. The FET has the small-signal parameters $g_m = 4$ mS and $r_d = 10$ kΩ; the source resistor $R_S = 4.7$ kΩ, and the gate resistor $R_G = 1$ MΩ. Calculate the gain and output impedance of the circuit. [8]

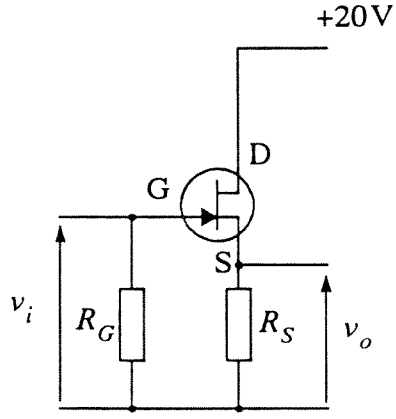


Fig. 4(a)

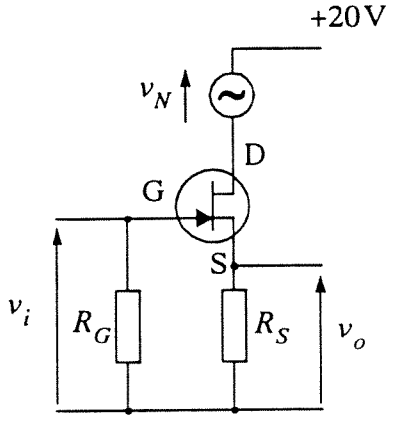


Fig. 4(b)

As a result of electrical interference, noise in the form of a small voltage of frequency 100 Hz is induced in the drain circuit of the FET. The presence of the 100 Hz noise can be modelled by the inclusion of a small signal source $v_N$ in the drain circuit as shown in Fig. 4(b).

Draw the small signal equivalent circuit for determining the component of the output voltage that arises as a result of the noise source. [4]

Determine the maximum amplitude of $v_N$ if the noise component of the amplifier's output is not to exceed 20 μV. [8]

SECTION B

*Answer not more than* **three** *questions from this section.*

5 Explain concisely the differences between combinational and sequential logic. [3]

Logic values A, B, C and D represent the four bits of a binary number in the range 0 to 15. A combinational logic circuit is to be devised which outputs 1 if the number is greater than 5 and less than 15; it is to output 0 otherwise. See Fig. 5 for details of the significance of the bits.

Using Karnaugh maps, show how to implement efficient logic systems to realise this function, using minimum numbers of:

(a) NAND gates and inverters;
(b) NOR gates and inverters. [12]

Explain how the Karnaugh map may be used to assist in identifying static hazards that might be present in your designs, and show how these may be corrected. [3]

It is often stated that the use of the Karnaugh map technique for simplifying logic functions leads to a solution requiring the minimum number of logic gates. Comment briefly on this proposition. [2]

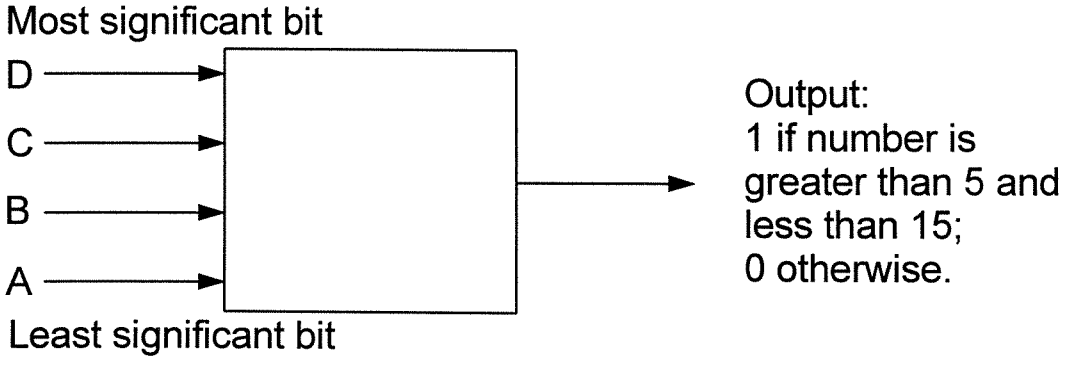


Fig. 5

6 A clocked sequential circuit has a single output $Y$ and is driven by a single input signal $U$, which passes through a series of binary states. The circuit is required to provide an output $Y = 1$ initially only when $U$ has taken the value 1 on three consecutive occasions. **From that moment on**, the circuit is to provide an output $Y = 1$ for each subsequent occasion on which the number of **consecutive** times $U$ has been low is **even**. Table 1 below shows an example of the required response $Y$ to the input $U$.

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U= | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Y= | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

Table 1

A partly completed state diagram from which to design the circuit is provided as Fig. 6. The design is to make use of three J-K bistables: A, B and C. Their state allocation is shown. The arrows linking the states are incomplete.

(a) Explain briefly to what actual conditions the six states shown correspond. [4]

(b) Copy and complete the state diagram, labelling it appropriately. [4]

(c) Draw a state transition table and construct Karnaugh maps to determine the simplest possible functions for inputs $J_B$ and $K_B$. [5]

(d) Is your design liable to be susceptible to static hazards? Comment. [2]

(e) Assuming each bistable is provided with a $\overline{CLR}$ input, suggest a means for ensuring that the circuit starts up in the state 000 immediately after power is applied. [5]

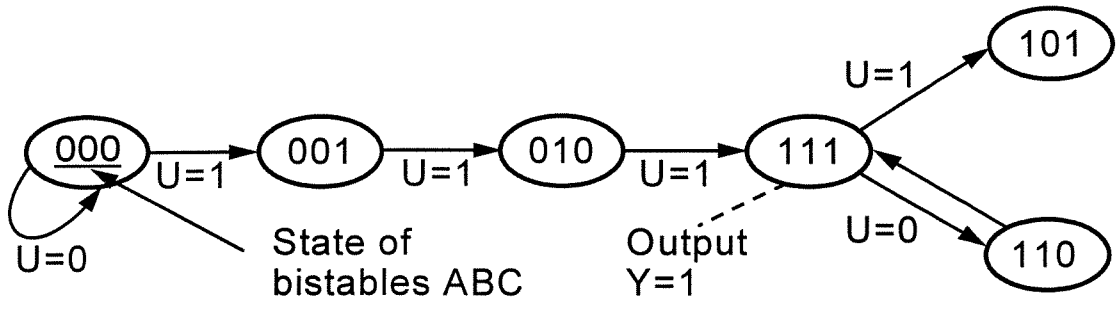


Fig. 6

7 (a) What is meant by a *shift register*? Describe briefly how clocked J-K bistables can be interconnected to form a shift register. [4]

Binary information is stored in a digital memory circuit in the form of 8-bit words. Explain in outline, with the aid of diagrams, how a shift register may be used to convert data from parallel to serial form for serial transmission. [3]

(b) What is meant by *2's complement* representation of negative numbers, and why is it important in information processing? [2]

In 8-bit 2's complement code what are the largest positive and largest negative numbers that can be represented? [2]

Derive the 8-bit binary equivalents for decimal +47, –89 and +68, explaining your working. Carry out binary addition to determine the sum of the three numbers, ignoring any carry beyond 8 bits. Show your working. [3]

(c) Explain concisely what is meant by the terms: *Schmitt trigger,* and *hysteresis*. Illustrate your explanation with a sketch of the transfer characteristic of a non-inverting Schmitt trigger. What useful purposes can a Schmitt trigger serve in processing slowly varying analogue signals for application to digital circuits? [6]

8 (a) What is meant by *memory-mapped input and output* in the context of microprocessor architecture? Which 6800 machine instructions are available to the programmer for performing transfer of input or output data between the microprocessor and a peripheral device? [4]

(b) In a 6800 microprocessor system, an 8-bit analogue to digital converter (ADC) is connected as an input device at memory location $F000, and an 8-bit digital to analogue converter (DAC) is connected as an output device at $F001. Both devices are adjusted to generate and respond to 2's complement signed binary codes. Data value $0_{10}$ corresponds to 0 volts, and $100_{10}$ to 1.00 volts. A second input port at address $F002 has its two least significant bits (D0 and D1) controlled by switches S0 and S1 which apply either logic 0 or logic 1 to the corresponding bit input. A time-varying signal in the range –0.5 volts to +0.5 volts is applied to the input of the ADC.

An efficient 6800 program is required to read samples from the ADC into Accumulator A, process them internally according to the settings of switches S0 and S1, and output the samples to the DAC. The actions to be taken in response to the switch settings are shown in Table 2 below.

Construct a flow diagram showing the movement of data required between registers and memory to implement the functions described above. Indicate appropriate 6800 instructions for the necessary arithmetic, data transfer and program control actions. [12]

With switches S0 and S1 both set to 1, what is the greatest range of input voltages that the system can effectively handle? If the 6800 microprocessor clock runs at 8 MHz, calculate the number of samples per second that your program can transfer. [4]

| **S1** | **S0** | **Action to be taken** |
|---|---|---|
| 0 | 0 | Output the sample unchanged |
| 0 | 1 | Scale the sample by ×2 before outputting to the DAC |
| 1 | 0 | Invert the sample (thus simulating an amplifier of gain –1) |
| 1 | 1 | Perform both the above actions (simulating an amplifier of gain –2) |

Table 2

SECTION C

*Answer not more than* **two** *questions from this section.*

9 Explain briefly what is meant by Gauss' Law in electrostatics. [3]

An electrostatic chuck for holding paper down on a flat bed plotter comprises a planar base electrode, with two layers of insulation and a top earthing electrode around its periphery. The paper rests on top of this, at earth potential, and may be considered to be an electrical conductor. To attract the paper down, a high voltage is applied to the base electrode. A cross-section of this arrangement is illustrated in Fig. 7.

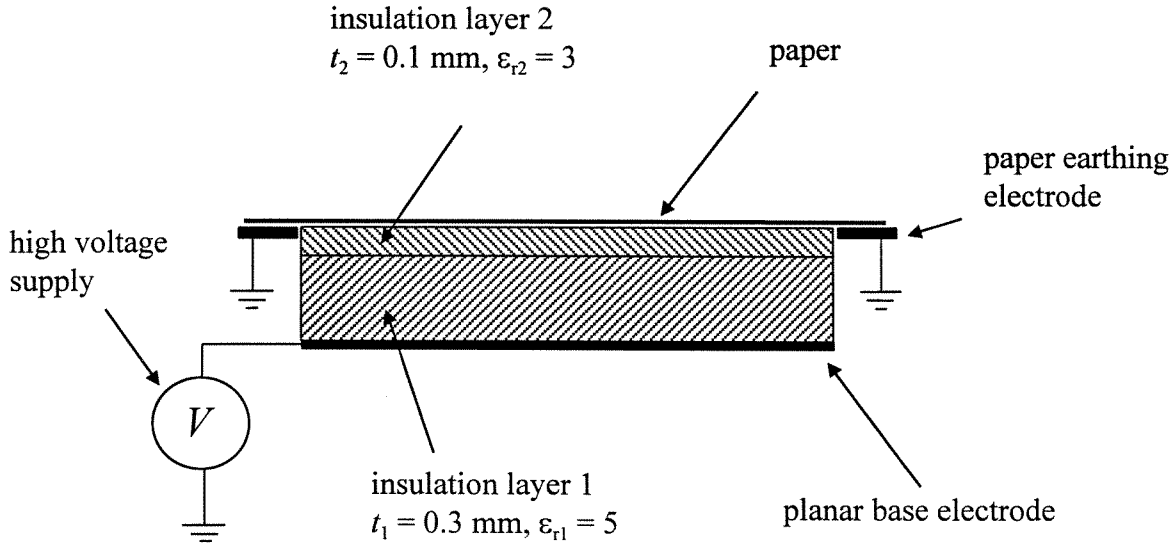


Fig. 7

The thickness and relative permittivity of insulation layer 1 are denoted by $t_1$ and $\varepsilon_{r1}$ respectively. For insulation layer 2 the corresponding values are $t_2$ and $\varepsilon_{r2}$.

(a) If $V = 1$ kV, what is the potential of the interface between the insulation layers? [4]

(b) Derive and evaluate an expression for the capacitance per unit area of the chuck when activated. State the assumptions made. [7]

(c) Using the method of virtual work, calculate the hold-down force per unit area on the paper when the chuck is activated. [6]

10 State Ampere's Law in integral form and briefly describe how it is used in analysing magnetic circuits. [2]

An electrically operated solenoid comprises a movable solid steel cylinder inside a coil of wire, where an outer steel sheath serves to concentrate the magnetic flux in a closed circuit. A cross-section of the device is shown in Fig. 8.

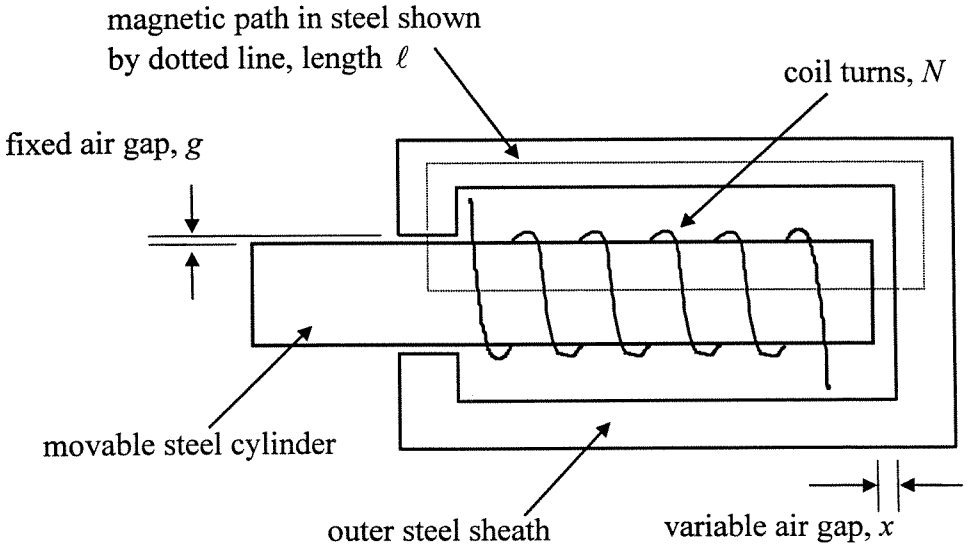


Fig. 8

Fixed air gap, $g = 0.2$ mm
Coil turns, $N = 200$
Average cross-section of magnetic flux path, $A = 0.5$ cm$^2$
Relative permeability of steel, $\mu_r = 1500$
Magnetic path length in steel, $\ell$, may be taken to be 50 mm, regardless of the air gap, $x$

(a) Derive an expression for the magnetic flux density, $B$, in the variable air gap as a function of the coil current, $I$, and the gap length, $x$. [4]

(b) What is the inductance of the coil when $x = 1$ mm? [6]

(c) Derive an expression for the force, $F$, exerted on the cylinder and evaluate this force when the coil current is 1.2 amperes and $x = 1$ mm. [6]

(d) How would you expect the force, $F$, to change if the coil current were increased by a factor of ten ? [2]

11 An isolated pair of long, parallel conductors of radius, $r$, have their axes separated by a distance, $d$, in air, where $d >> r$. This arrangement is shown in Fig. 9.

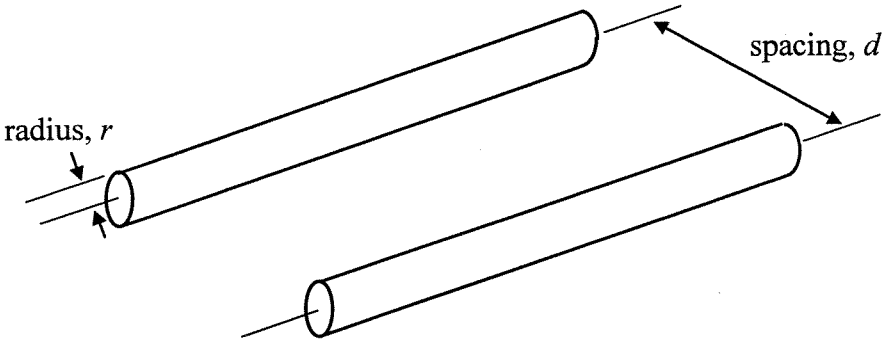


Fig. 9

(a) Derive an expression for the capacitance, $C$, between the conductors. [6]

(b) If one of the conductors carries a current, $I$, derive an expression, using Ampere's Law, for the magnetic flux density, $B$, as a function of distance from the conductor axis. [4]

(c) Considering the conductors to be two sides of a long, thin loop, derive an expression for the self inductance, $L$, per unit length of the conductors, stating the approximations made. [7]

(d) Evaluate the expression $(LC)^{-1/2}$. [3]

**END OF PAPER**