1.(a) $V_{gs} = -3V$, which must be voltage across
$R_2 = I_{ds} R_2$ ie $10^{-3} . R_2 = 3$ or $R_2 = 3k\Omega$.

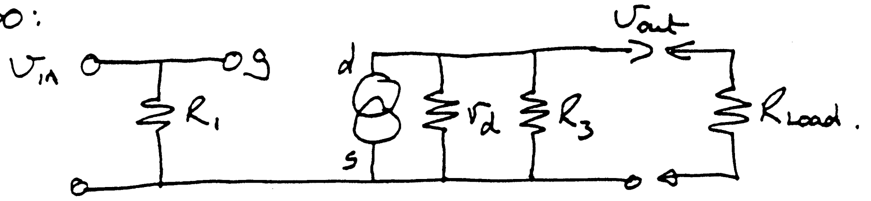
Voltage across : $R_2 = 3V$
FET $= 10V$
$R_3 = 10k\Omega . 1mA = 10V$

$\therefore V_{DD} = 23V$. $R_1 = $ e.g. $1M\Omega$

R_1 high to avoid absorbing signal, but low enough to take leakage.

(b) Capacitive impedances are negligible (ie 0)

so:



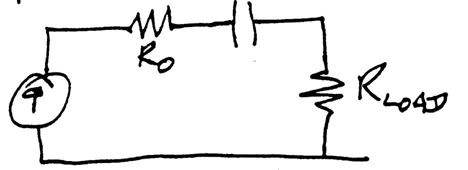
Input impedance $= R_1$ ($= 1M\Omega$)

$R_o =$ Output impedance $= r_d || R_3 = \frac{50.10}{50+10} k\Omega = 8.33k\Omega$

Gain $= g_m . R_o = -5 \times 8.33 . = 41.65$

c) For maximum power $R_{Load} = R_o = 8.33k\Omega$.

d) At 3dB point, Thevenin equivalent of load circuit :



$\therefore X_c = 2R_o$ or $\frac{1}{2\pi 100 . C} = 16.66 . 10^3$

or $C = \frac{1}{2\pi . 100 . 16.66 . 10^3}$

$= 95.5 nF$ ($= 95.5 . 10^{-9} F$).

Q2.

a) Perfect OP amp:

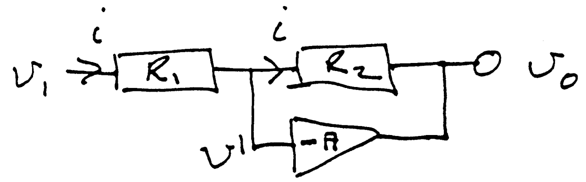
gain $= \infty$ (at all frequencies)

input impedance $= \infty$, output impedance $= 0$

(also input offset voltage $= 0$, but not really required here; also other minor things)

To regard an amplifier as perfect, the input circuit impedance must be << amplifier input impedance, output circuit impedance >> amplifier output impedance, and the circuit gain (with feedback) << amplifier gain at the operating frequency.

b)



$$i = \frac{v' - v_o}{R_2} = \frac{v'(1+A)}{R_2}$$

$$\text{or } v' = \frac{iR_2}{1+A} \quad \text{and } v_1 = iR_1 + \frac{iR_2}{1+A}$$

$$\text{or } R_{IN} = R_1 + \frac{R_2}{1+A} = 10^3 + \frac{10^4}{101} = 1099\,\Omega$$

$$v_o = -Av' = \frac{-iAR_2}{1+A}$$

$$v_1 = iR_1 + \frac{iR_2}{1+A}$$

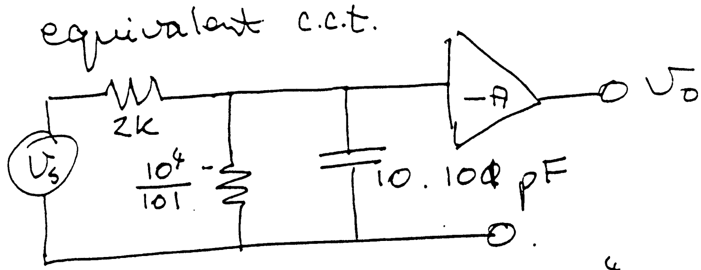
$$\therefore G = \frac{v_o}{v_1} = \frac{-AR_2}{R_1(1+A) + R_2} = \frac{-100.10^4}{10^3.101 + 10^4} = -9.01$$

c) Substitute $R_1 = 2\,k\Omega$ in above eq.n

$$\therefore v_o = \frac{-AR_2 v_s}{R_1(1+A) + R_2} = \frac{-100.10^4 v_s}{2.10^3.101 + 10^4} = -4.72\,v_s$$

Q2 (cont)

d) equivalent c.c.t.



Resistive impedance $= 2.10^3 \| \frac{10^4}{101} \doteq 2.10^3 \| 99$

$= 94.3\Omega$.

Capacitive impedance $= 1010\,pF$.

At 3dB point $R = \frac{1}{2\pi fC}$

or $f = \frac{1}{2\pi RC} = \frac{1}{2\pi . 94.3 . 1010 . 10^{-12}}$

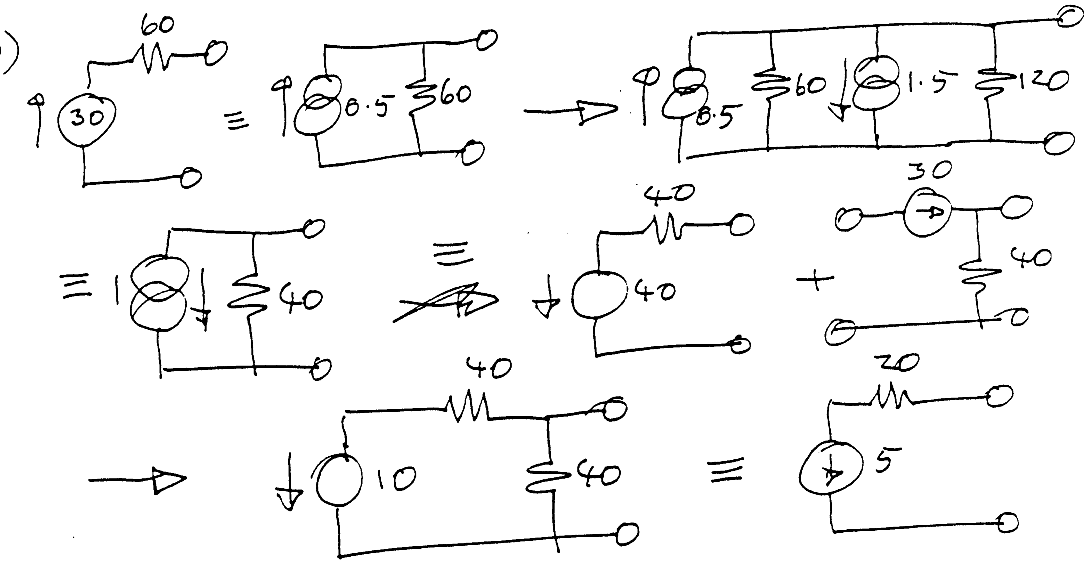
$= 1.67\,MHz$.

3(a) any linear network can be expressed as:

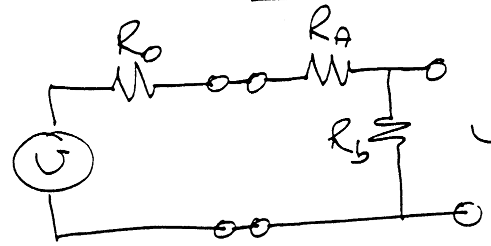
a resistance with a series voltage source (Thevenin)

a resistance with a parallel ~~current~~ source (Norton)

(b)



c)



$$v_o = \frac{v}{2} = v \cdot \frac{R_b}{R_o + R_A + R_B}$$

$$\text{or} \quad \frac{R_b}{R_o + R_A + R_B} = \frac{1}{2}$$

Also $Z_o = R_o = R_b \| R_o + R_A$

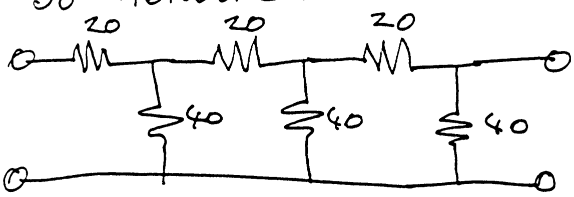
$$\therefore R_o = \frac{R_b(R_o + R_A)}{R_o + R_A + R_b} = \frac{R_o + R_A}{2} \quad \text{(using } \text{)}$$

$\therefore R_o = R_A = 20\,\Omega$.

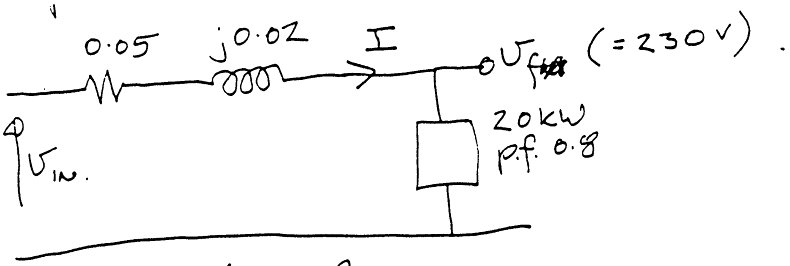
and $2R_B = R_o + R_o + R_B$ or $R_B = 2R_o = 40\,\Omega$

d). $8 = 2 \times 2 \times 2$, and Thevenin impedance = constant

So network :



4 (a)



$$230 \cdot I \cdot \cos\phi = P$$

$$\therefore I = \frac{20 \cdot 10^3}{230 \cdot 0 \cdot 8} = 108 \cdot 7\ A$$

$$\frac{Q}{P} = \tan\phi \quad \therefore Q_{LOAD} = P_{LOAD} \tan\phi = 20 \cdot 10^3 \cdot 0.75$$
$$= 15 \cdot 10^3\ VAr$$

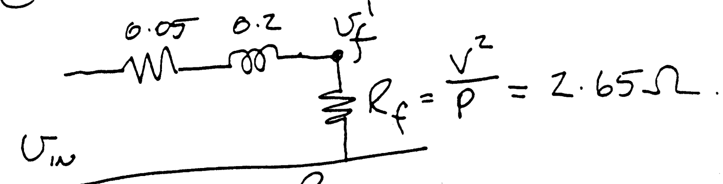
$$P_{LINE} = I^2 R = 108 \cdot 7^2 \cdot 0.05 = \underline{590 \cdot 8\ W}$$
$$Q_{LINE} = I^2 X = 108 \cdot 7^2 \cdot 0.2 = 2363\ VAr$$
$$\therefore \text{Input } P = 20 \cdot 10^3 + 590 \cdot 8 \doteqdot 20591\ W$$
$$\text{Input } Q = 15 \cdot 10^3 + 2363 = 17363\ VAr.$$
$$\text{But } (VA)^2 = P^2 + Q^2$$
$$\therefore \text{Input } VA = \sqrt{(20591^2 + 17363^2)} = 26934$$
$$\therefore \text{Input } V = \frac{VA}{I} = \frac{26934}{108 \cdot 7} = \underline{\underline{247 \cdot 8\ V.}}$$

b) Min. power in line when p.f. = 1

Cancel load VArs: $\frac{V_{LOAD}^2}{X_c} = Q_L$ or $X_c = \frac{V_{LOAD}^2}{Q_L} = 3.53\Omega$

$$\frac{1}{2\pi f C} = X_c \quad \text{or} \quad C = \frac{1}{2\pi f X_c} = \underline{\underline{902\ \mu F.}}$$

c)



$$R_f = \frac{V^2}{P} = 2 \cdot 65\Omega.$$

$$V_f' = V_{IN} \times \frac{R_f}{R_{Lin} + R_f + jX_L} = 241 \cdot 9 - j17 \cdot 9$$

$$\therefore |V_f'| = \underline{\underline{242 \cdot 6\ \text{volts.}}}$$

Section B

5.a) Truth table

Input	I_2	I_1	I_0	O_2	O_1	O_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	0	1
3	0	1	1	0	1	0
4	1	0	0	0	1	0
5	1	0	1	0	1	1
6	1	1	0	0	1	1
7	1	1	1	1	0	0

b) Draw a 3 variable Karnaugh Map for each output (groups for zeros and ones shown)

O_0

I_2 \ I_1I_0	00	01	11	10
0	0	1	0	1
1	0	1	0	1

O_1

	0	0	1	0
I_2	1	1	0	1

O_2

0	0	0	0
0	0	1	0

For sum of product use mapping 1s

$$O_0 = I_0\overline{I_1} + \overline{I_0}I_1 \quad (= XOR(I_0 I_1))$$
$$O_1 = \overline{I_1}I_2 + \overline{I_0}I_2 + I_0I_1\overline{I_2}$$
$$O_2 = I_0I_1I_2$$

Product of sums (from mapping zeros)

$$O_0 = (I_0+I_1).(\bar{I}_0+\bar{I}_1)$$
$$O_1 = (I_1+I_2).(I_0+I_2).(\bar{I}_0+\bar{I}_1+\bar{I}_2)$$
$$O_2 = I_0 I_1 I_2 \text{ (again)}$$

c) NAND gate implementation

First convert product of sums to NAND form (De Morgan)

$$O_0 = \overline{\overline{I_0\bar{I}_1}\,.\,\overline{\bar{I}_0 I_1}}$$

$$O_1 = \overline{\overline{\bar{I}_1 I_2}\,.\,\overline{\bar{I}_0 I_2}\,.\,\overline{I_0 I_1 \bar{I}_2}}$$

$$O_2 = \overline{\overline{I_0 I_1 I_2}}$$

Here only 2-input NAND available

Hence convert expression for O_1, O_2 to only require 2-input NAND gates.

$$O_1 = \overline{\overline{\overline{\overline{\bar{I}_1 I_2}\,.\,\overline{\bar{I}_0 I_2}}}\,.\,\overline{\overline{\overline{I_0 I_1}}\,.\,\bar{I}_2}}$$

and

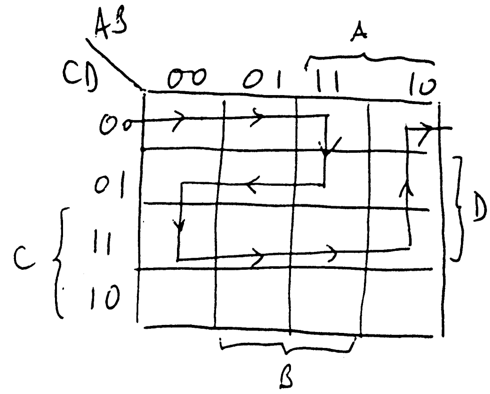
$$O_2 = \overline{\overline{\overline{\overline{I_0 I_1}}\, I_2}}$$

6 a) Unused states: states of bistables not taken up in the sequence used by the circuit. If the circuit initially enters such a state the subsequent behavior may be undefined unless the designer has taken this into account.

b) Unused states: 0010
0110
1110
1010

Draw state table & required J_A, K_A, J_B, K_B inputs

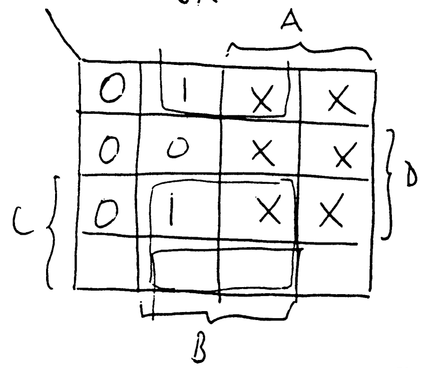
State A	State B	State C	State D	Next State A	Next State B	Next State C	Next State D	J_A	K_A	J_B	K_B
0	0	0	0	0	1	0	0	0	X	1	X
0	1	0	0	1	1	0	0	1	X	X	0
1	1	0	0	1	1	0	1	X	0	X	0
1	1	0	1	0	1	0	1	X	1	X	0
0	1	0	1	0	0	0	1	0	X	X	1
0	0	0	1	0	0	1	1	0	X	0	X
0	0	1	1	0	1	1	1	0	X	1	X
0	1	1	1	1	1	1	1	1	X	X	0
1	1	1	1	1	0	1	1	X	0	X	1
1	0	1	1	1	0	0	1	X	0	0	X
1	0	0	1	1	0	0	0	X	0	0	X
1	0	0	0	0	0	0	0	X	1	0	X



Use unit distance property of ~~[illegible]~~ code to make maps easier to draw

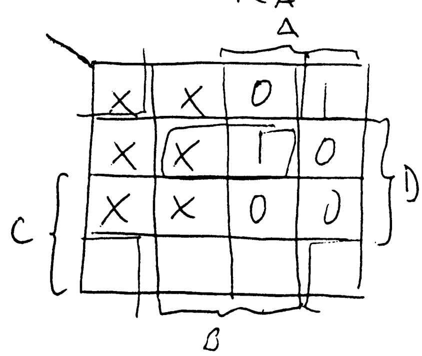
Bistable inputs

J_A



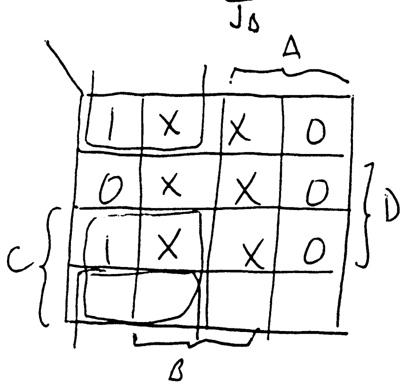
$J_A = Q_B Q_C + Q_B \bar{Q}_D$

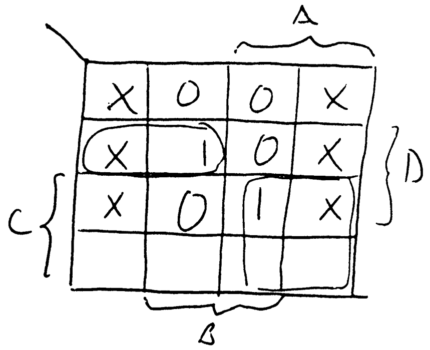
K_A



$K_A = \bar{Q}_B \bar{Q}_D + Q_B \bar{Q}_C Q_D$

J_B





$J_B = \bar{Q}_A \bar{Q}_D + \bar{Q}_A Q_C$

$K_B = \bar{Q}_A \bar{Q}_C Q_D + Q_A Q_C$

c) If unused states occur two possibilities to return to correct sequence:

i) At startup ensure that the clear input to all bistables is set so that they start in state 0000

ii) Add extra rows to the state table & ensure that count returns to 0000 (or some other point) on the next clock. This makes the expressions for the bistable inputs more complex since few don't care states.

7 a) CCR contains following bits

H - half carry
I - interrupt mask
N - negative (leading bit = 1)
Z - zero (all bits zero)
V - 2's complement overflow
C - carry

The bits are set as a result of various instructions often in a data dependent way (e.g. the result ~~of~~ overflowed 2's complement range, or all bits zero). Branches examine combinations of CCR bits (set previously) to determine whether to take the branch. Arithmetic instructions can use e.g. carry bit to perform multiple precision arithmetic.

b) i)

```
        CLC             ; carry cleared
        LDAB $0900      ; load number in range 1->15
                        ; to ACCB
        LDX #$0A00      ; load index reg with 0A00
LOOP:   LDAA $00,X      ; load A from address in X
        ADCA $10,X      ; A := A + value(X+10) + C
        STAA $20,X      ; store A in X+20
        INX             ; X = X+1
        DECB            ; B := B-1
        BNE LOOP        ; If B>0 GOTO LOOP
```

Carry is initially zero. ADCA will set it if carry from addition and other instructions leave carry unchanged.

ii) It can be seen that the program performs multi-byte addition (via carry) of 2 1-15 byte numbers. The first (LSByte) is at $0A00 & the second at

$ØA1Ø and the result at $ØA2Ø.

iii) Timing

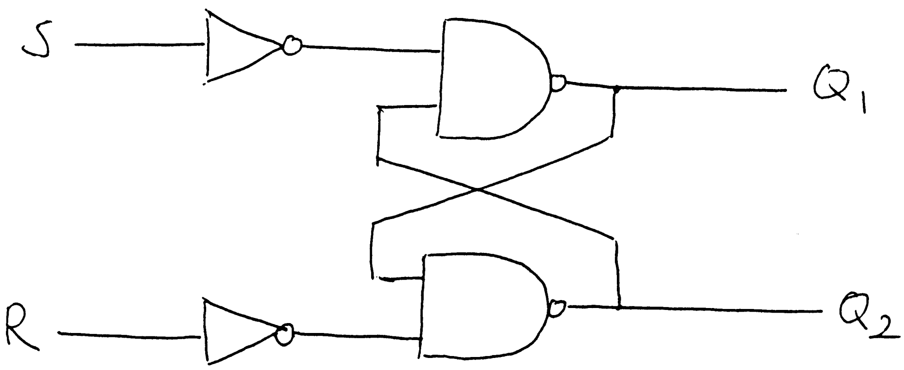
			# clock
	CLC		2
	LDAB	$Ø4Øa	4
	LDX	#$0A00	3
LOOP:	LDAA	$00,X	5
	ADCA	$10,X	5
	STAA	$20,X	6
	INX		4
	DECB		2
	BNE	LOOP	4

26 per loop

$$\text{total cycles} = 9 + 26 \times 3$$
$$= 87 \text{ cycles.}$$

$$\text{At } 8MHz \text{ clock} = \frac{87}{8} \mu s$$
$$= \underline{10.4 \mu s}$$

8a) i) S-R bistable



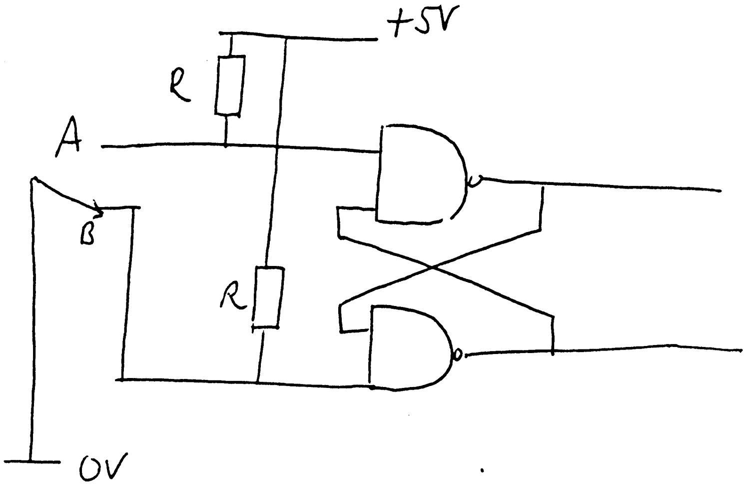
S = 1, R = 0 causes Q_1 to go high (NAND i/p low)
Q_2 to go low $\Rightarrow Q_2 = \overline{Q_1}$

S = 0, R = 1 causes Q_1 to go low
Q_2 to go high (NAND i/p low) $Q_2 = \overline{Q_1}$

S = 0, R = 0 no change Q_1, Q_2 at previous state

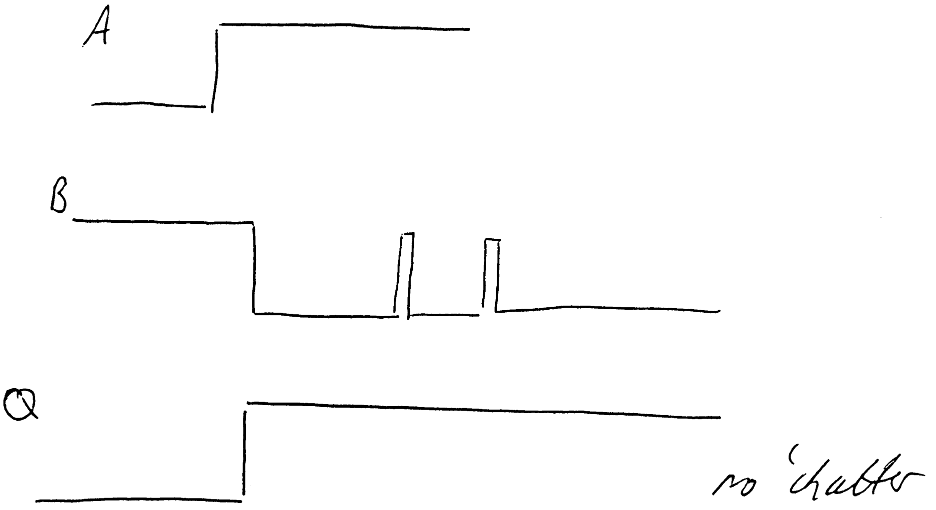
S = 1, R = 1 forces both outputs high
$\Rightarrow Q_2 \neq \overline{Q_1}$ & this state normally disallowed

For contact debouncing use the latter part of the above circuit



Typical waveform

Voltage at



b) $R/\overline{W}$ line : Describe the direction of the data bus (either reading from the device when high or writing to it when low)

$\overline{CS}$ line : This is an enable (chip select). It must be low for the device to be selected & is typically used in address decoding.

Need 1 bistable per memory cell (bit)
13 address lines $\Rightarrow 2^{13}$ locations $\times$ 8bits / location
Hence $2^{13} \times 2^3$ bits $= 2^{16}$ bistables
$= \underline{65536}$.

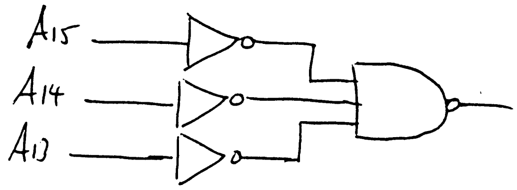
Number of addressable bytes is $2^{13} = 8192 = 8k$ bytes

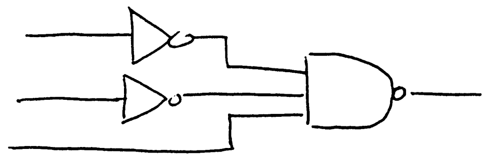
Hence to fill $0000H \rightarrow 7FFFH = 32k$ bytes need
$\frac{32k}{8}$ k $= \underline{4}$ packages

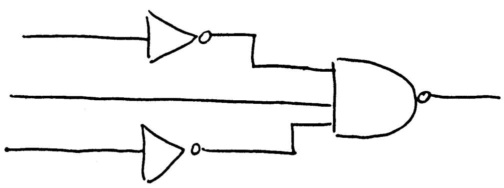
Assuming upper 3 lines for address decoding & fully decoded to lower 32k

		A_{15}	A_{14}	A_{13}
Package at	0000H	0	0	0
	2000H	0	0	1
	4000H	0	1	0
	6000H	0	1	1

For each of these packages typical circuitry (to connect to $\overline{CS}$ on memory package)

000


001


010


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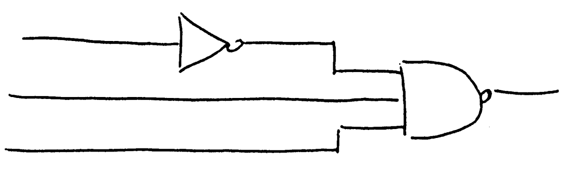


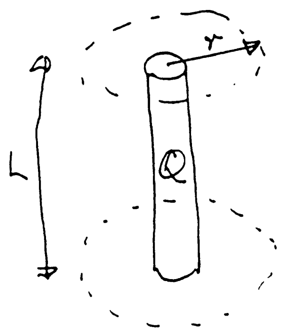
Other schemes possible.

Question 9.

a) Gauss' Law states $\oint D \cdot dS = Q$

or the electric flux leaving a volume is equal to the total enclosed charge.

b). Length L of rod, with charge Q on it:
(Radial field only: ignore end effects



Gauss: $2\pi r . D_r L = Q$

but assume linear dielectric of ϵ

$\therefore D_r = \epsilon E_r$

$\therefore \quad E_r = \frac{D_r}{\epsilon} = \frac{Q}{L 2\pi\epsilon} \cdot \frac{1}{r}$

But voltage between R_1 and R_2 = $\int_{R_1}^{R_2} E_r dr$

$\therefore V = \frac{Q}{2\pi\epsilon L}\Big[\log_e r\Big]_{R_1}^{R_2} = \frac{Q}{2\pi\epsilon L} \log_e \frac{R_2}{R_1}$

But $C = \frac{Q}{V} \quad \therefore C = \frac{2\pi\epsilon L}{\log_e \frac{R_2}{R_1}}$

air : $\epsilon = \epsilon_0 . 1 \rightarrow C = 8.03\,pF$
liquid : $\epsilon = \epsilon_0 . 2 \quad\quad C = 16.06\,pF$.

c). $C|_d = \left(8 + 8 . \frac{d}{200}\right) pF \quad$ (d in mm)
$= (8 + 0.04\,d)\ pF$

d) Virtual work : δ(Electrical Stored Energy) = δ(Potential Energy)
Applying volts will tend to "suck" liquid into tube.

$\delta U_E = \frac{\partial C}{\partial h} . \delta h . \frac{1}{2} V^2 \quad \left(\delta U_E = \frac{1}{2}\delta C . V^2\right)$

$\delta U_p = g . \rho . A . h . \delta h \quad\quad A$ = area in tube
$= \cancel{\frac{\pi}{4}\left((2R_2)^2 - (2R_1)^2\right) = \frac{\pi}{4}(8 - 1)\,mm^2}$
$= \pi(R_2^2 - R_1^2) = \pi . 15\ mm^2$

$\therefore \frac{\partial C}{\partial h} . \frac{1}{2} V^2 = g \rho A h$

$\left[\frac{\partial C}{\partial h} = 40\,pF/m,\ g = 9.81,\ \rho = 10^3,\ A = 15 . \pi . 10^{-6}\right]$

$h = \frac{\frac{\partial C}{\partial h} . \frac{1}{2} V^2}{g \rho A} = 4.3 . 10^{-5}\,m$ or $0.043\ mm$

Question 10.

a) Assumptions: lines of flux circular
: all flux travels in toroid (none in air).
: linear materials so:

$$\oint H.dl = NI \quad \text{and} \quad B = \mu H$$

So at radius ~~R~~ r

$$N_1 I = \pi r . H_1 + \pi r H_2$$

but $B = \text{const.}$ $\therefore$ $H_1 = \frac{B}{\mu_1}$, $H_2 = \frac{B}{\mu_2}$

$$\therefore NI = \pi r B_r\left(\frac{1}{\mu_1} + \frac{1}{\mu_2}\right)$$

or $$B_r = \frac{N_1 I}{\pi r\left(\frac{1}{\mu_1} + \frac{1}{\mu_2}\right)}$$

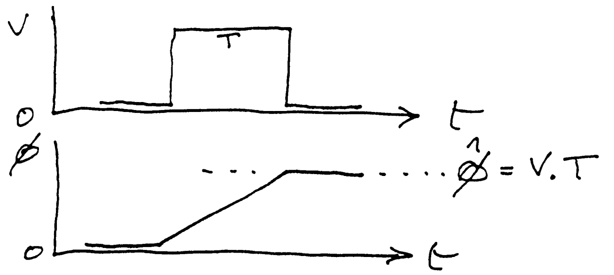
$$\Phi = \int_S B\,dA = \frac{N_1 I}{\pi\left(\frac{1}{\mu_1} + \frac{1}{\mu_2}\right)} \cdot d \cdot \int_{R_1}^{R_2} \frac{1}{r}\,dr$$

$$= \underline{\frac{N_1 I d}{\pi\left(\frac{1}{\mu_1} + \frac{1}{\mu_2}\right)} \log_e \frac{R_2}{R_1}}$$

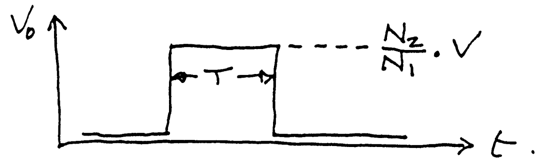
but $\Phi = LI$ so Inductance $L = \frac{\Phi}{I} = \frac{N_1 d}{\pi\left(\frac{1}{\mu_1} + \frac{1}{\mu_2}\right)} \log_e \frac{R_2}{R_1}$

Makes no difference if coil shifted.

b) $\Phi = LI$ and $V = L\frac{dI}{dt}$ $\therefore$ $V = \frac{d\phi}{dt}$.



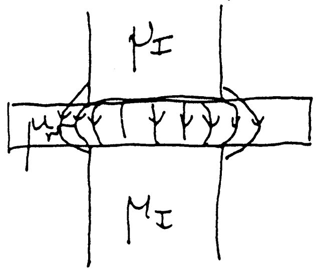
c)



d) If $\mu_1; \mu_2 \gg 1$ as stated, all the flux is in the toroid, and none will be in the centre. (For uniformly wound toroid, any residual fields at the centre will cancel as well.)

Question 11

a) If $\mu_r < \mu_I$ (ie the relative permittivity of the yoke & poles) then fringing is where the magnetic field lines "bulge" between the pole pieces, with consequent loss of uniformity for the field over the pole area.



Gets worse if:

(i) t increases
(ii) A decreases
(iii) μ_r decreases.

(proportionately).

b) Ampere's law: $NI = H_I L + H_s t$

but $B_I = B_s$ and $B_s = \mu H_s$.

so $H_s = \dfrac{B_I}{\mu_0 \mu_r}$

Assume:
(i) All field in yoke etc.
(ii) Uniform field
(iii) Constant mag. path

$\therefore NI = H_I L + \dfrac{B_I . t}{\mu_0 \mu_r}$

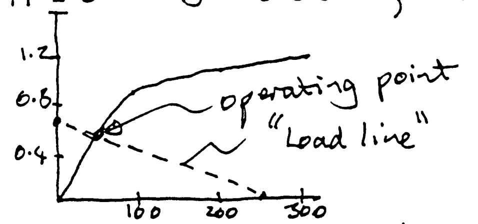
or $B_I = NI \dfrac{\mu_0 \mu_r}{t} - H_I . \dfrac{L}{t} . \mu_0 \mu_r$.

$= \dfrac{500 . 0.1 . 4\pi . 10^{-7} . 100}{10^{-2}} - H_I . \dfrac{0.2}{0.01} . 4\pi . 10^{-7} . 100$

$= 0.628 - H_I . 2.51 . 10^{-3}$

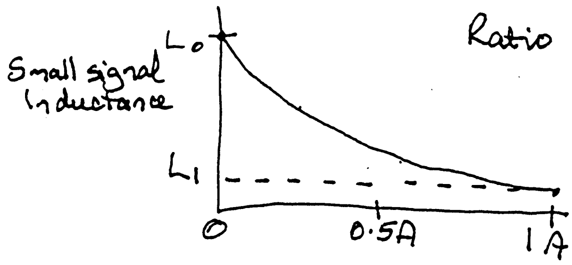
Use 4% Si : Fe curve in data book:

$H = 0$: $B = 0.63$ Tesla $B = 0$: $H = \dfrac{0.63}{2.5 . 10^{-3}} = 251$ A/m



$B_{sample} = B_{iron} = 0.53$ Tesla

c) If yoke + sample are doubled, ϕ doubles (constant NI) hence L doubles (non linearity doesn't matter).



Ratio $\dfrac{L_0}{L_1} = \dfrac{\text{B-H Slope at } H=0}{\text{B-H Slope}, H = \text{large}}$.

Could calculate new H as in part b)