ENGINEERING TRIPOS PART IA

Tuesday 8 June 1999 9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

Answer not more than **eight** *questions, of which not more than* **three** *may be taken from Section A, not more than* **three** *from Section B, and not more than* **two** *from Section C.*

The **approximate** *number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

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SECTION A

Answer not more than **three** *questions from this section.*

1 An FET is configured in an amplifier as shown in Fig.1. The impedances of C_{in}, C_{out}, and C_s are negligible at mid-band frequencies. The small signal parameters of the FET are g_m = -5 mA/V and r_d = 50 kΩ, and its operating point is given by V_{ds} = 10 V, V_{gs} = -3 V, and I_{ds} = 1 mA.

(a) At the given operating point, calculate values for R_2 and V_{DD} given that R_3 = 10 kΩ. Also suggest a suitable value for R_1 and justify your choice. [5]

(b) For the circuit of Fig. 1, (without R_{load} connected) draw, and carefully label, a small signal equivalent circuit, and hence calculate its voltage gain, and also its input and output impedances, all at mid-band frequencies. [7]

(c) What value of external load resistance, R_{load}, should be connected between the output terminal of the amplifier and ground in order to maximise the signal power in this load? [3]

(d) If the lower 3dB cut-off frequency of the amplifier is 100 Hz and is dominated by the effect of C_{out}, calculate the value of this capacitor, assuming that R_{load} of part (c) is connected. [5]

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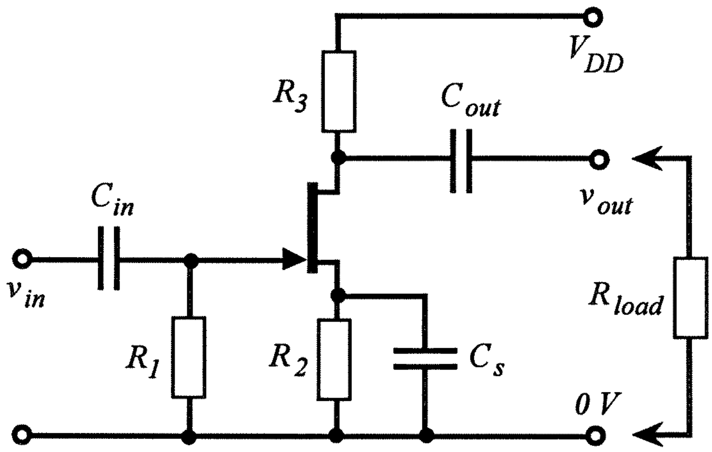

Fig. 1

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2 (a) What are the parameters that describe an ideal operational amplifier, and under what circumstances may real amplifiers be regarded as ideal? [4]

(b) The operational amplifier shown in Fig. 2 is ideal, except that it has a gain, A, of 100. Calculate the input impedance and voltage gain of the circuit, given that the signal source is not connected, and neglecting the effects of C_f. [7]

(c) What is the output voltage v_o in terms of v_s if the signal source as shown in Fig. 2 is connected to the circuit? [4]

(d) With the signal source connected, and if C_f is now significant, with a value of 10 pF, what is the frequency at which the output voltage, v_o, falls to 70% of its low frequency value? [5]

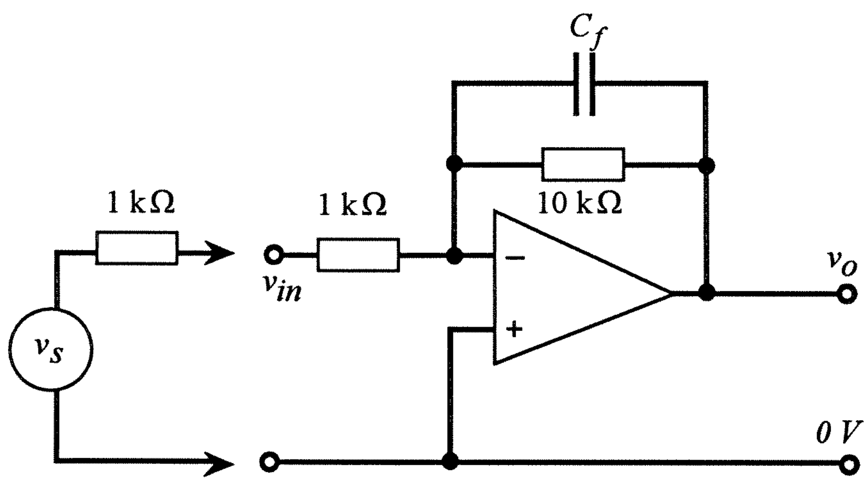

Fig. 2

3 (a) State Thevenin's and Norton's Theorems. [4]

(b) Calculate the Thevenin equivalent circuit of the left hand circuit shown in Fig. 3. which has output terminals A and B. [6]

(c) The right hand circuit in Fig. 3 is to be arranged so that terminal C is connected to A, and B to D, so that a new output voltage appears between terminals E and F. The Thevenin equivalent impedance associated with terminals E and F is to be the same as between A and B in part (b) and the output voltage should be halved. Calculate the values of resistors R_a and R_b. [6]

(d) A new additional circuit is now required to produce an output voltage 1/8th of that between terminals A and B in part (b), while retaining the same Thevenin impedance. Using your results from part (c), suggest a suitable network to connect to terminals A and B. [4]

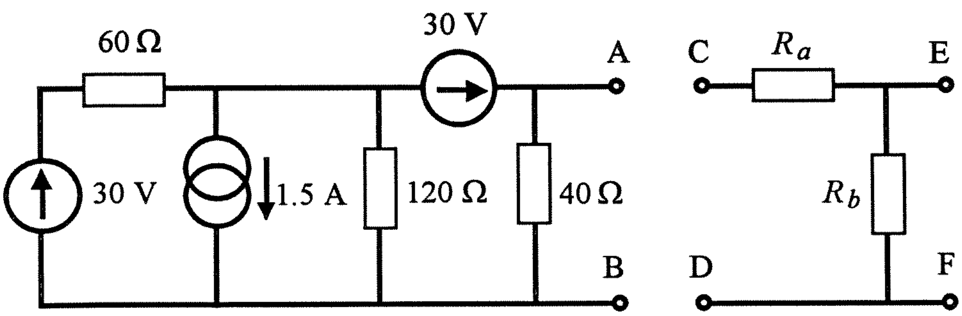

Fig. 3

4 A small factory consumes 20 kW at 230 V with a lagging power factor of 0.8 and the line supplying the factory has an impedance of $0.05 + j0.2\ \Omega$.

(a) Draw a circuit diagram for the above system, and then calculate the power lost in the line, and the voltage at the supply end of the line. [8]

(b) What is the minimum power lost in the line if power factor correction is employed at the factory, and the factory voltage remains at 230 V? What capacitance value should be added to the load to achieve this, and where on your circuit diagram should it be connected? [7]

(c) If power factor correction is employed as in part (b), but the voltage at the supply end of the line remains at the value of part (a), what is the new voltage at the factory? [5]

SECTION B

Answer not more than **three** *questions from this section.*

5 A combinational logic circuit has three inputs and three outputs. The input variables I_0, I_1, I_2, represent the three bits of a binary number n in the range 0 to 7 (I_2 is the most significant bit). The outputs of the circuit O_0, O_1, O_2 are the binary representation of $(n + 1)/2$ rounded down to the nearest integer.

(a) Draw a truth-table to describe the operation of the circuit. [4]

(b) Using Karnaugh maps, find simplified sum-of-products and product-of-sums expressions for each output variable O_0, O_1, O_2. [10]

(c) Show how the circuit could be implemented using only two-input NAND gates. [6]

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6 (a) What is meant by an unused state in synchronous sequential logic circuits? Describe how unused states can cause improper operation. [4]

(b) The state sequence for a count-of-12 unit distance code is shown in Fig. 4. The counter is to be implemented using four clocked J-K bistables.

(i) List the unused states. [3]

(ii) Assuming the unused states do not occur, determine the required J and K inputs for the bistables A and B. [10]

(iii) Suggest methods for returning the counter to the correct sequence if an unused state occurs. [3]

A	B	C	D
0	0	0	0
0	1	0	0
1	1	0	0
1	1	0	1
0	1	0	1
0	0	0	1
0	0	1	1
0	1	1	1
1	1	1	1
1	0	1	1
1	0	0	1
1	0	0	0

Fig. 4

7 (a) Explain the role of the condition-codes register in programming the 6800 microprocessor. How is it used in both arithmetic and branch operations? [4]

(b) A fragment of a 6800 program is shown below. It can be assumed that a number in the range 1 to 15 is stored at address `0900H`.

```
       CLC
       LDAB    $0900
       LDX     #$0A00
LOOP:  LDAA    $00,X
       ADCA    $10,X
       STAA    $20,X
       INX
       DECB
       BNE     LOOP
```

(i) Write out this code segment. For each instruction, state the effect and indicate how the carry bit is used or affected. [5]

(ii) Briefly explain the function of the program segment. [4]

(iii) Given that the 6800 uses an 8MHz clock, calculate the time taken to execute the program segment when the value stored at `0900H` is 3. [7]

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8 (a) (i) Show how an S-R bistable circuit with outputs Q and $\overline{Q}$ can be constructed from NAND gates. Clearly explain the operation of the circuit for each combination of the two inputs. [6]

(ii) Describe how an S-R bistable could be used to construct a contact debouncing circuit. [4]

(b) A memory chip which uses bistables for the internal memory devices has 8 pins for data lines, pins for $R/\overline{W}$ and $\overline{CS}$ signals and 13 address lines.

(i) What is the function of the $R/\overline{W}$ and $\overline{CS}$ lines? [2]

(ii) Estimate the total number of bistables in the package. [2]

(iii) How many packages of this type are required to fill the memory map from 0000H to 7FFFH? [2]

(iv) Describe the address decoding circuitry that is necessary for each of the packages. [4]

SECTION C

Answer not more than **two** *questions from this section.*

9 An electromagnet is constructed of 4% Silicon-Iron as shown in Fig. 5. It has magnetic path length L and yoke cross-sectional area S, in order to apply a magnetic field to a sample of a linear magnetic material with a relative permeability, μ_r, of 100. The sample is also of area S and fits precisely between the poles of the electromagnet which have separation t.

(a) Explain what is meant by *fringing* associated with the poles of an electromagnet, and indicate qualitatively how it varies with S, t, and μ_r as defined above. [4]

(b) If $L = 200$ mm, $t = 10$ mm, $N = 500$ and $I = 0.1$ A, what is the magnetic flux density in the sample? You may assume zero fringing, but state any other approximations made. [11]

(c) How will the inductance of the coil vary if the area of the yoke and sample is doubled? Also sketch approximately what happens to the inductance of the coil as the d.c. current I is varied between 0 and 1 A. [5]

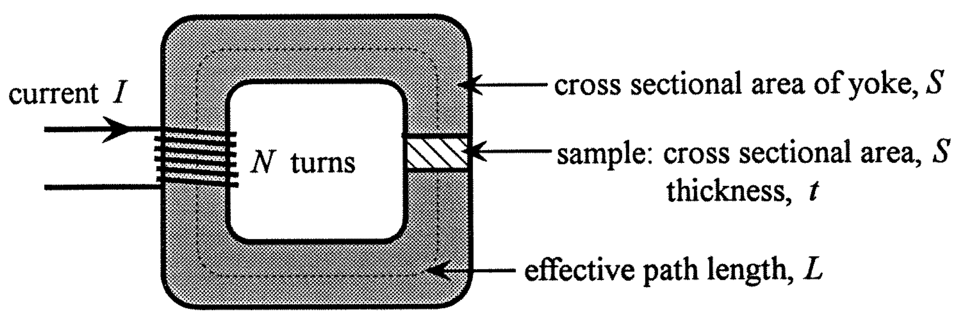

Fig. 5

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10 (a) State Gauss' theorem for electrostatics, and explain what it means. [5]

(b) A vertical metal rod of radius R_1 = 1 mm is fixed concentrically inside an open ended tube of inside radius R_2 = 4 mm as shown in Fig. 6. Rod and tube are both of length L = 200 mm. Starting from Gauss' theorem, find the capacitance between rod and tube

(i) when the intervening dielectric is air, $(d = 0)$

(ii) when the dielectric is a fluid of relative permittivity 2, $(d = L)$.

You should neglect the effects of surface tension and end effects. [7]

(c) What is the capacitance of the rod in tube as a function of liquid depth, d, from the bottom of the tube? [3]

(d) If the rod and tube are held so that the dielectric liquid enters the tube by a few millimetres, and then a potential difference of 1 kV is applied between them, does the liquid level rise or fall? Given that the density of the liquid is 1000 kg/m^3, use virtual work to estimate the change in level. [5]

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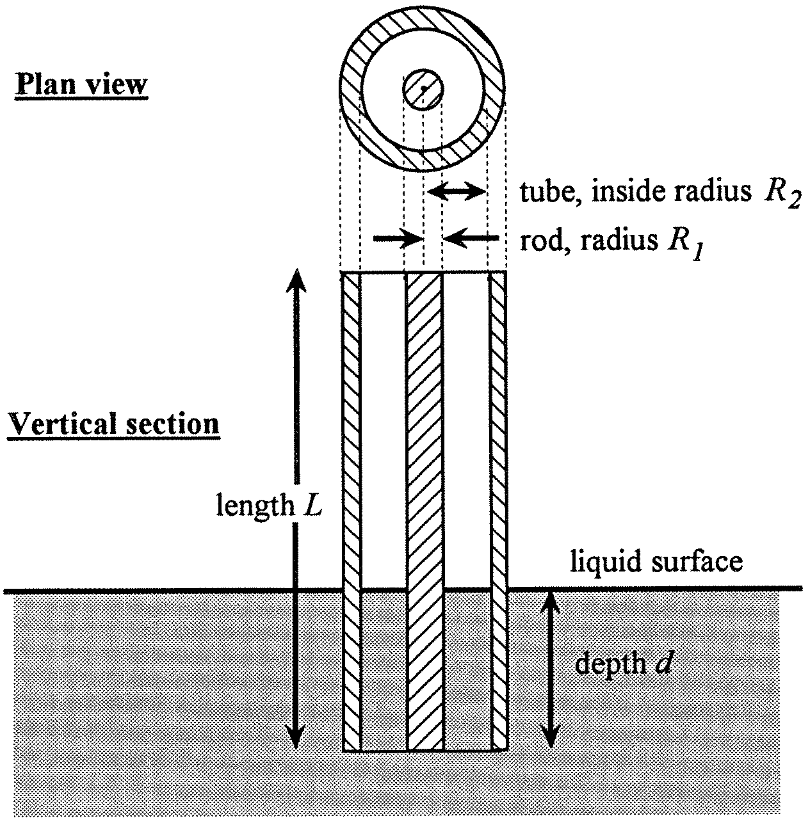

Fig. 6

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11 A toroidal inductor is constructed as shown in Fig. 7 with inner radius R_1 and outer radius R_2 which is significantly greater than R_1. Half A has relative permeability μ_A and half B has relative permeability μ_B (μ_A >>1 and μ_B >> 1). A coil of N_A turns is wound onto half A, both halves are of depth d and they fit perfectly together.

(a) Calculate the inductance of the unit as described, and state any approximations made. What would be the inductance if the coil were shifted onto half B of the toroid? [9]

(b) A rectangular pulse of voltage V and duration T is applied to the coil. Calculate the peak flux circulating in the toroid, and mark this on a sketch of flux circulating in response to the voltage pulse. Assume that the initial flux is zero. [4]

(c) Another coil of N_B turns is added to half B of the toroid, and connected to a high impedance oscilloscope input. Sketch the voltage waveform observed in response to the voltage pulse of part (b). [4]

(d) If a steady current I_A is applied to the coil on half A, what is the approximate flux density at point O in the centre of the toroid, and why is this so? [3]

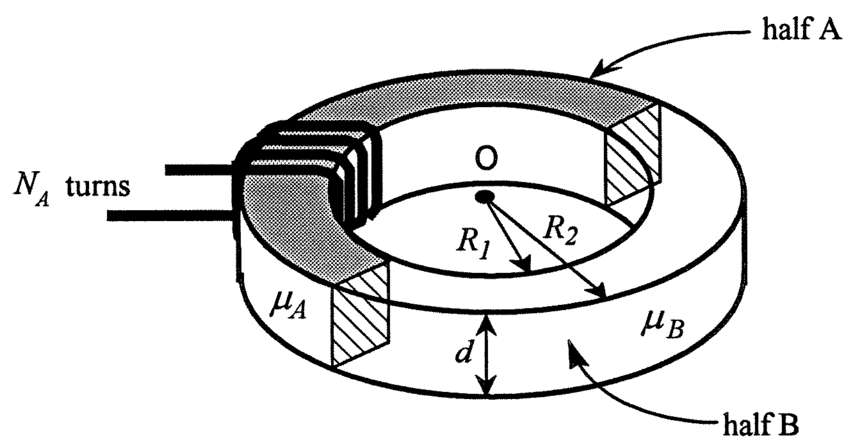

Fig. 7

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