Question 1.

1(a). The circuit denotes a buffer amplifier which converts a signal from high to low impedance with a voltage gain of slightly less than unity. It could be used as a microphone pre-amplifier, or anywhere that a high impedance source occurs.

1(b) Note that the bias conditions are for d.c. only, and have nothing to do with the small signal parameters or circuit.
If the supply is 20 V and 7 V is dropped from drain to source, then the 13 V remaining must be dropped across R_3. However, R_3 must have 2.6 mA flowing through it, so its value is 13/2.6 V/mA = 5.0 kΩ.
V_s has been calculated as 13 V, and the question gives V_{gs} as – 3 V, so V_g must be 13 – 3 = 10 V , so by inspection $R_1 = R_2 = 2$ MΩ.

1(c) Small signal circuit:
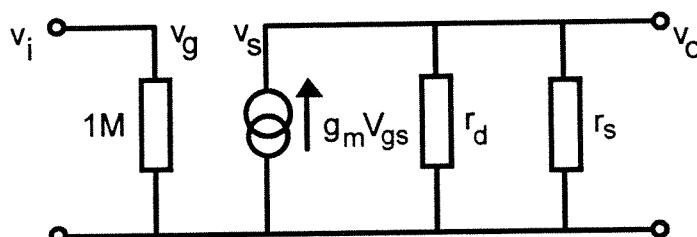
For simplicity in calculations let (r_d in parallel with r_s) = R' = 4.55 kΩ.
Then: $\qquad g_m(v_i - v_o)R' = v_o$

$$\frac{v_o}{v_i} = \frac{g_m R'}{1 + g_m R'} = \text{voltage gain} \qquad \text{(note this must be + ve)}$$

$$= 0.958.$$

$$I_{out} \text{(short circuit)} = g_m v_i \qquad V_{out} \text{(open circuit)} = \frac{g_m R' v_i}{1 + g_m R'}$$

$$\text{Output impedance, } Z_o = \frac{V_o \text{ (open circuit)}}{I_o \text{ (short circuit)}} = \frac{R'}{1 + g_m R'}$$

$$\text{Input impedance} = 2 \text{ M}\Omega \; || \; 2 \text{ M}\Omega = 1 \text{ M}\Omega$$

1(d) At the 3 dB point: Real Impedance = Imaginary Impedance, so

$$1 \text{ M}\Omega = \frac{1}{2\pi f C} = \frac{1}{2\pi 159 C}$$

$$\text{or } C = \frac{1}{100.10^8} = 0.01 \mu F$$

1(e) Maximum output power is *not* with a matched load: that gives the maximum power for a given input, and in this case we can choose any input we like.

The maximum power at a single frequency is given by the maximum pure sine wave than can be generated by the circuit, i.e. twice 7 = 14 V peak-to-peak or 7 V peak. The rms output voltage is then $\sqrt{7}$ V, and the maximum power into a 10 kΩ load is :

$$P_{max} = \frac{v_o^2}{R_{load}} = \frac{\sqrt{7}^2}{R} = \frac{7}{10.10^3} = 0.7 \text{ mW}$$

Question 2.

2(a) Using simple expression for ideal amplifier gain:

$$v_o = -\frac{R_f}{2R} = -5$$

2(b) Circuit *for mid-band purposes only*. (i.e. coupling capacitors are short circuited, and shunt capacitors open circuited).
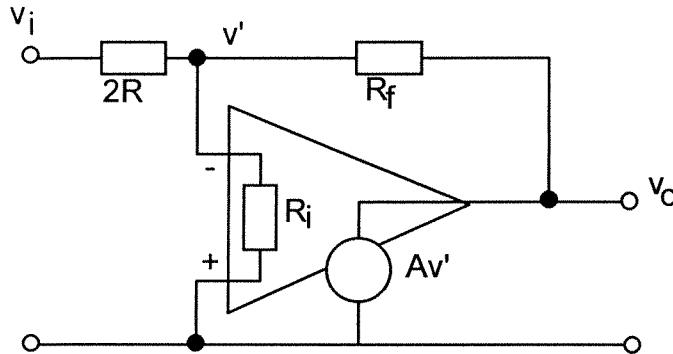
Start with nodal analysis at inverting input of amplifier, and then re-arrange to eliminate v'

$$v' = -\frac{v_o}{A}$$

$$\frac{v_i}{2R} + \frac{v_o}{R_f} = v'\left[\frac{1}{R_i} + \frac{1}{2R} + \frac{1}{R_f}\right]$$

$$\frac{v_i}{v_o} = -\frac{2R}{R_f}\left[1 + \frac{R_f}{A}\left(\frac{1}{R_i} + \frac{1}{2R} + \frac{1}{R_f}\right)\right]$$

$$\frac{v_o}{v_i} = G = -\frac{R_f}{2R}\left[1\Big/1 + \frac{1}{A}\left(\frac{R_f}{R_i} + \frac{R_f}{2R} + 1\right)\right]$$

Then substitute values: $R_f = 10^4$, $R = 10^3$, $R_i = 10^4$, $A = 10^4$, giving:

$$G = -5.\left[\frac{1}{1 + 10^{-4}.(1 + 5 + 1)}\right] = -4.9965$$

Note this is almost equal to the approximate value of section (a) : the sign is the same, and the numerical value is slightly less.

(c) Lower 3_{dB} point is determined by the series capacitor and the resistances effectively in series with it, noting that the parallel capacitor may be ignored, and that the amplifier input is a virtual earth, so:

$$\text{Lower } f_{3dB} = \frac{1}{2\pi.C_1.2R} = \frac{1}{4\pi * 7.96 * 10^{-6} * 10^3} \approx 10 \text{ Hz}$$

Upper 3_{dB} point is determined by the *parallel* capacitor, and the effictive resistance across it. In this case the resistor on the input side is fed from a low impedance,

Question 3

3(a) $v_A = 0.5 - j0.5$
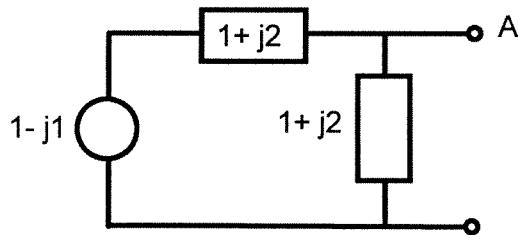
$v_B = j3$ V   (Z_4 is in parallel with a voltage generator: therefore no effect)

3(b)   Thevenin equivalent circuits:

0.5 + j1

3 = j2
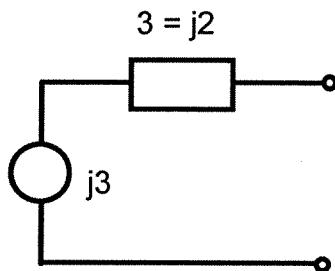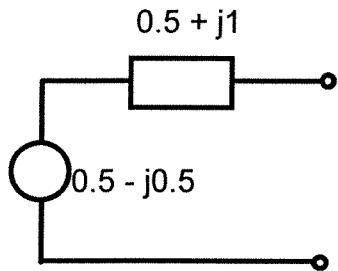
I(short circuit) = - 0.2 - 0.6j

I(short circuit) = 0.46 + 0.69j

Norton equivalent circuits:
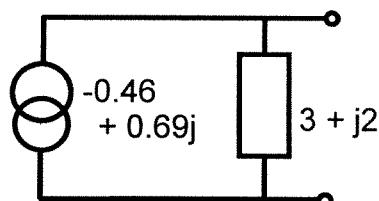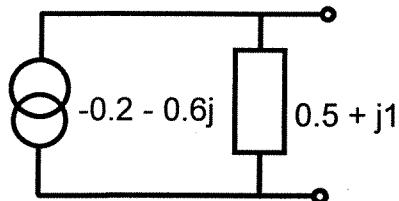
Note: It is possible to do all these and other real and imaginary calculations by hand, but it's *very* much easier to use a calculator in complex mode. *Do* write down intermediate answers and keep a mental check though, because it is all too easy to press the wrong button and get a completely silly answer.

3(c)   This is very much like the examples paper question set early in the Michaelmas term, except that the current sources are complex: ie having converted all the branches of the circuit into their Norton equivalents, add the complex currents and convert the parallel impedances into their single equivalent.

Adding parallel impedances:

$$\frac{1}{0.5 + j1} + \frac{1}{3 + j2} + \frac{1}{3 + j2} = 0.8615 - j1.107$$

so voltage at ABC (when connected) = 0.063 + 0.1856j

3(d) The voltage at ABC relative to V_1 is what would be measured by a vector voltmeter referenced to V_1 : ie the vector subtraction $V_{ABC} - V_1$. This is easiest done by subtracting the real and imaginary parts, and then using the calculator to convert back to polar form, giving the result, $V_{rel} = 1.51$ V $\angle$ 128°

and that on the amplifier side goes to a virtual earth, so the two resistances are effectively in parallel to earth, and so the 3_{dB} frequency is given by:

$$\text{Upper } f_{3dB} = \frac{1}{2\pi * C_2 * \frac{R}{2}} = \frac{1}{\pi * 31.8 * 10^{-9} * 10^3} \approx 10^4 \text{ Hz}$$
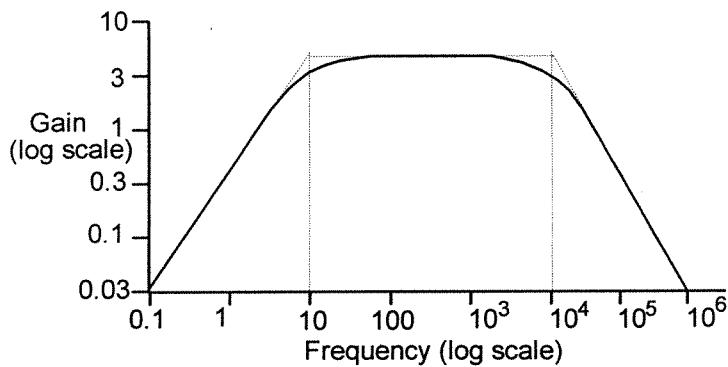

d) No extra phase shift in mid band, but amplifier inverts, so phase is $180°$
At lower 3dB point, phase comes forward by $45°$, i.e. $180 - 45 = 135°$
At upper 3dB point, phase lags by an extra $45°$, i.e. $180 + 45 = 225°$.

Question 4

4(a) High voltage insulators are easy to arrange, and involve negligible power losses, so transmission losses due to resistance can be minimised by operating at very high voltage. Transformers are then necessary to drop the voltage to a value convenient and safe for domestic purposes. Furthermore, various larger industrial machines and processes require power at a variety of voltages, and all of these may be convieniently and efficiently arranged via transformers.

As well as being necessary for transformers, a.c. is good for power switching (arc extinction), safety (usually "thrown off" rather than "frozen on" which can happen with d.c.), switching via thyristors, and also rotating magnetic fields are possible without the use of brushes or commutators.

4(b)   Copper loss: resistance of windings + leakage inductance of windings
Iron loss: hysteresis in iron magnetisation curves cause power loss, and the shape also causes some apparent inductive loss. Eddy currents also cause similar effects (distinguishable by changing frequency).
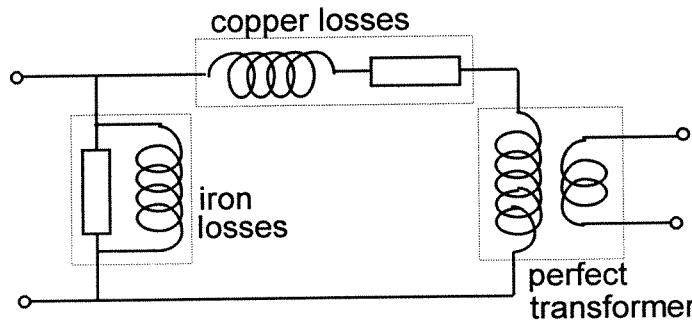
Measure iron losses at rated voltage but open circuit output (when copper losses $\to$ 0).
Measure iron losses at rated current, but short circuit output (when iron losses $\to$ 0).

4(c)
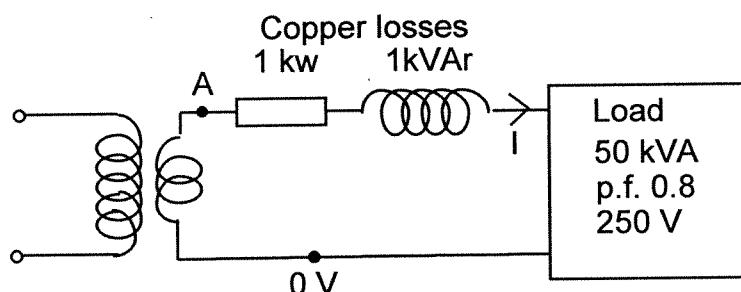
$P_{load} = 50 * 0.8$ kW $= 40$ kW
$Q_{load} = 50 * 0.6$ kVAr $= 30$ kVAr
$I = 50 * 10^3 / 250$ A $= 200$A

Losses are split equally between copper and iron, for voltage calculations the iron losses may be negelected, since in the simple model they occur in parallel with the transformer input. The copper losses are then 1 kW and 1 kVAr respectively.

At point A,　　total power, $P_{tot} = (40 + 1)$ kW

　　　　total reactive power, $Q_{tot} = (30 + 1)$ kVAr

But $P^2 + Q^2 = S^2 = 1681 + 969 = 2642$

and　　　$S = \sqrt{(2642)} = 51.4$ kVA

but I = 200A,

so $V_A = 51,400 / 200 = 257$ Volts

This will be the no-load voltage, since with no load the copper losses have no effect.

SECTION B — DIGITAL CIRCUITS

5. a) Karnaugh maps — simplify logic expressions up to 5 var.
   - Array of cells, each cell represents one combination of all the logic variables
   - Neighbouring cells vary by one variable value only & hence edges labelled by a unit distance code
   - combining pairs of cells eliminates 1 var, 4 cells 2 vars, 8 cells 3 vars.

The combined groups that "cover" the logic function (with arbitrary assignment to don't care cells) directly lead to a sum of products expression.
A sum of product for the logic 0 function can be used to derive a product of sums expression by de Morgan.

b) o/p high if at least 2 of ABC are high also D, E
   or if all of ABC are high.
   Hence maps for is

Mapping zeros (groups of 0)

$$\bar{Z} = \bar{A}\bar{B} + \bar{A}\bar{D} + \bar{A}\bar{E} + \bar{A}\bar{C} + \bar{B}\bar{C} + A\bar{B}\bar{D} + \bar{C}\bar{D} + \bar{D}\bar{E} + \bar{C}\bar{E}$$

$$Z = \overline{\bar{A}\bar{B} + \bar{A}\bar{D} + \bar{A}\bar{C} + \bar{A}\bar{E} + \bar{B}\bar{C} + \bar{B}\bar{D} + \bar{B}\bar{E} + \bar{C}\bar{D} + \bar{C}\bar{E}} \quad \text{(non}$$

$$Z = (A+B).(A+D)(A+C)(A+E)(B+C)(B+D)(B+E)(C+D)(C+E) \quad \text{Product of Sums}$$

Circuit implementation is straightforward from NOR expression but note that to make 7-input NOR gate use 2×5 inputs + 2 inverters
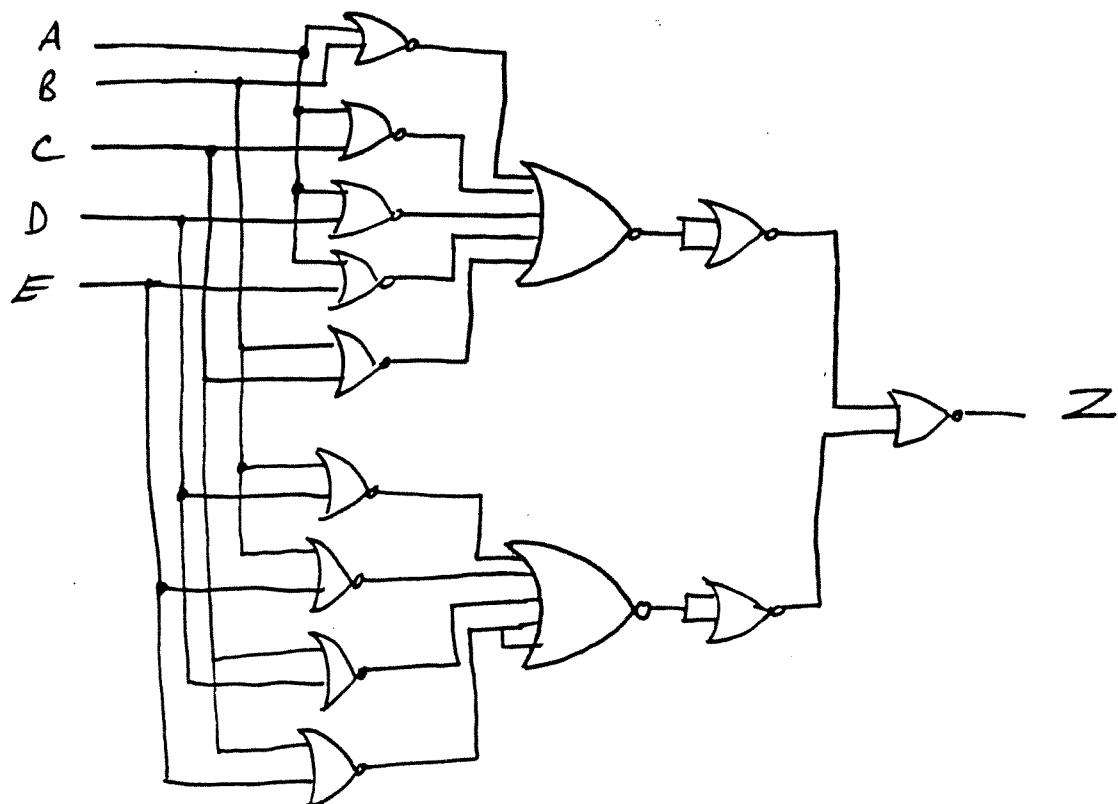
6 a) Sychronous : uses single clock for all sequential
logic elements, circuit operates at clock speed

Asynchronous : outputs from various stage clock other
stage, speed of operation depends on
circuit delays

Synchronous logic is much easier to design for
large circuits but is slower (uses more power) than
asynchronous.

b) i)

Current	Next	J_A	K_A	J_B	K_B	J_C	K_C
A C B A	C B A						
0 0 0	0 0 1	0	X	0	X	1	X
0 0 1	0 1 0	0	X	1	X	X	1
0 1 0	0 1 1	0	X	X	0	1	X
0 1 1	1 0 0	1	X	X	1	X	1
1 0 0	1 0 1	X	0	0	X	1	X
1 0 1	0 0 0	X	1	0	X	X	1
1 1 0	0 0 0	X	1	X	1	0	X
1 1 1	0 0 0	X	1	X	1	X	1

J_A

B			
A-0 | 1 | 1 | 0 | 1 |
A-1 | X | X | X | X |

C

K_A

X	X	X	X
1	1	1	1

J_B

0	X	X	0
1	X	X	0

K_B

X	0	1	X
X	1	1	X

J_C

0	0	X	X
0	1	X	X

K_C

| X	X	1	0
X	X	1	1

For NOR map 0's

$\overline{J_A} = BC \Rightarrow J_A = \overline{\overline{B} + \overline{C}}$ $\qquad K_A = 1$

$\overline{J_B} = \overline{A} + C \qquad J_B = \overline{\overline{A} + C} \qquad \overline{K_B} = \overline{A}.\overline{C} \qquad K_B = \overline{\overline{A} + C}$

$\overline{J_C} = \overline{A} + \overline{B} \qquad J_C = \overline{\overline{A} + \overline{B}} \qquad \overline{K_C} = \overline{A}.\overline{B} \qquad K_C = \overline{\overline{A} + \overline{B}}$

Assuming $\overline{A}, \overline{B}, \overline{C}$ available $\Rightarrow$ 5 NORs + 2 inverters (2 NOR)

iii) Circuit
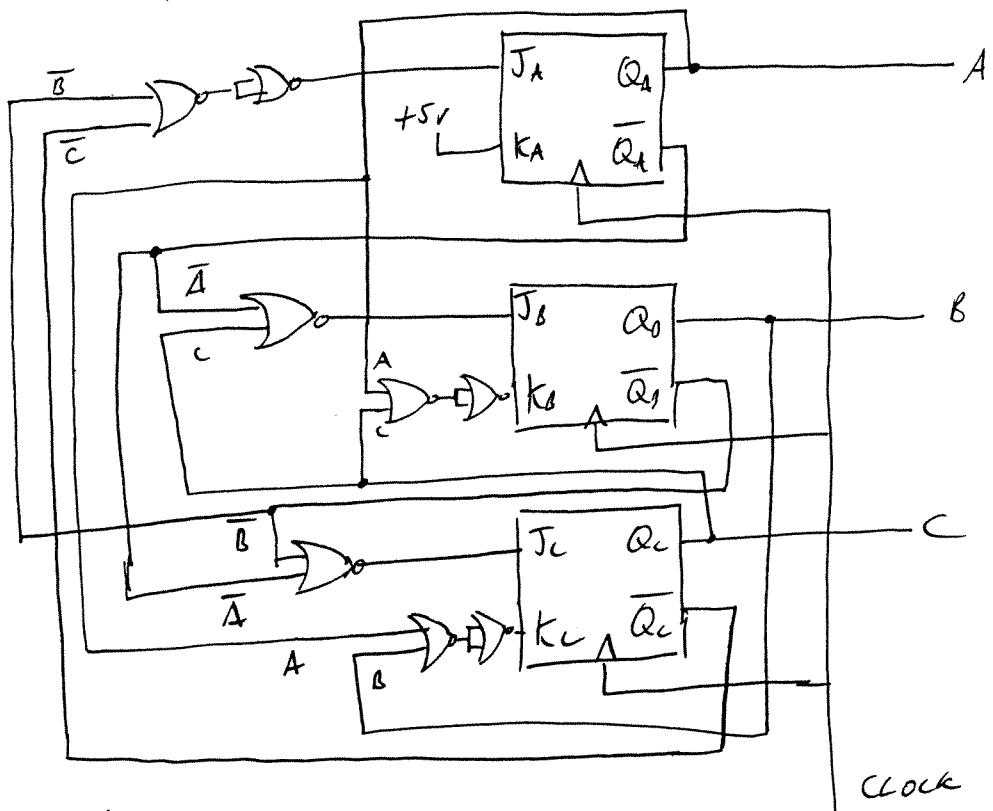
iv) MAP 1's from K-MAP.

$J_A = \overline{B} + \overline{C} \quad , \quad K_A = 1$

$J_B = A\overline{C} \quad , \quad K_B = A + C$

$J_C = A.B \qquad K_C = A + B$

2 AND , 3 OR (5 total) v's 7 NOR

7 a) Register - stores /manipulates data, addresses, status to access, process, store results of calculations.
- acts as memory inside the microprocessor.

SP - points to top of stack (grows downward).
Stack used to store temporary variables + subroutine return addresses etc

PC - stores address of next instruction to be executed. Manipulated directly in branch, jump etc instructions.

b) i)

	Comment	Addressing Mode	~
LDAA #8	00001000 → Acc A	Imm.	2
STAA $0203	→ $0203	Extd	5
CLRA	00000000 → Acc A	Implied	2
LDAB $0201	Number 1→15 in Acc B	Extd	4
LOOP: ASLA	shift left Acc A 1 bit	Implied	2
BITB $203	AND B with value in 0203 + set flags	Extd	4
BEQ 03	if result zero jump next inst.	Rel.	4
ADDA $0202	Add value of $0202 into A	Extd	4
ASR $0203	shift 0203 right 1 bit	Extd	6
BNE LOOP	if result not zero loop	Rel.	4

ii) Program repeatedly tests to see if a bit in Acc B is set & if so it adds the values stored in Acc A & then shifts Acc A
This works to multiply the values initially stored in $0201 & $0202

Example: 0000 0001 → Acc B   1000 0111 → $0202

Iteration #	Acc A	Acc A after Add	#$0203
1	0	7	8
2	14	14 } add	4
3	28	28 } skipped	2
4	56	63	1

iii) For values given (from example above) take 4 iterations through loop. On 2 iterations executes add instr & on two it doesn't.

Total cycle (from commented program)

Before loop   = 13
Loop incl Add   = 24
Loop n. incl Add = 20

$$Total = 13 + 2 \times 24 + 2 \times 20$$
$$= 101 \text{ cycles}$$

At 8MHz take $\dfrac{101}{8 \times 10^{6}} \mu s = \underline{12.625 \mu s}$

Note:

Program performs a 4 bit multiplication with result in Acc A.

If # in $0202 is > 15 then Acc A may overflow & need to store a high byte of result.

Can do this by adding any carry from result & ADDA instr. to the high byte & after the ASLA instruction also shifting left the high byte & the result using ROL.   NOT REQD

8 a) Dual of a Boolean law :

For any law in Boolean algebra there is another law, it's _dual_ formed by interchanging or, And and interchanging 0, 1

b)

$$\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = A \oplus B \oplus C$$

$$A \oplus B = A\bar{B} + \bar{A}B \qquad A \oplus B \oplus C = \overline{(A.\bar{B} + \bar{A}B)}.\bar{C} + \overline{(A.\bar{B} + \bar{A}B)}.C$$

Expanding

$$A \oplus B \oplus C = A.\bar{B}.C + \bar{A}BC + \overline{(A.\bar{B})}\overline{(\bar{A}.B)}.C$$

$$A\bar{B}C + \bar{A}BC + (\bar{A} + B)(A + \bar{B})C$$

$$A \oplus B \oplus C = A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + ABC \qquad \text{as req}^d.$$

c) 2's complement.

For an N bit number the Representation for positive numbers in range $0 \le x \le 2^{N-1} - 1$ is std binary

For negative numbers in range $-2^{N-1} \le -x < 0$ use Representation

$$2^N - x$$

To convert from decimal

   i) convert to binary representation of positive number if >0 or $-x$ if <0

   $\frac{ii}{}$ If $-ve$

   ii) Complement all the bits and add $\underline{1}$.

To convert to decimal

   i) if MSB set ($-ve$ number) complement and add $\underline{1}$

   ii) binary $\rightarrow$ +ve number. If originally negative then $-ve$.

Q8 cont'd

So

d)

-7 $7 = 0000\ 0111$

Compl. $1111\ 1000\ +1 = 1111\ 1001$

-42 $42 = 0010\ 1010$

Compl $1101\ 0101\ +1 = 1101\ 0110$

$63 = 0011\ 1111$

Adding

$$
\begin{array}{rll}
0011 & 1111 & (63) \\
1101 & 0110 & (-42) \\
\hline
(1)\ 0001 & 0101 & (21)
\end{array}
$$

Ignore high bit & add

$$
\begin{array}{ll}
0001 & 0101 \\
1111 & 1001 \\
\hline
(1)\ 0000 & 1110 \qquad (14)
\end{array}
$$

the MSB is zero — hence +ve. Ignore the leading 1.

Convert to decimal as $0 \times 2^0 + 1 \times 2^1 + 1 \times 2^2 + 1 \times 2^3 + 0$.

$= \underline{14}$.

e) Tristate logic has 3 states $0, 1$, open circuit

It is used for multiple bus access. When the tristate buffer is enabled, the access to the bus is allowed & any logic 0 or logic 1 at the buffer input is transferred to the bus.

When the tristate buffer is not enabled, then the buffer output is open circuit & it no longer appears on the bus.

This allows multiple memory devices to be connected to the bus & enabled for an appropriate range of addresses

7) $128 k\,bit = 16k\,byte$ or $2^{14}\,byte$

$\Rightarrow$ 14 memory address line (8 data)

15th line $(A14)$ used to select bank
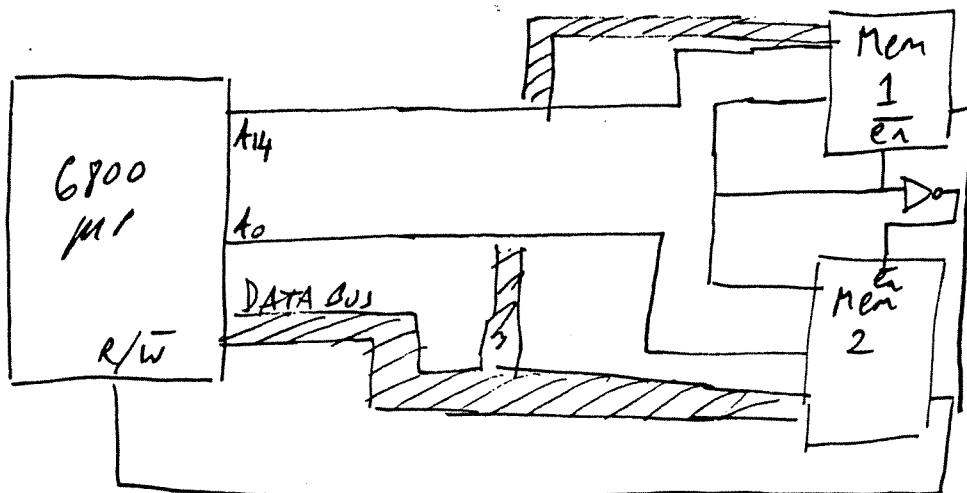
9(a) $\int_S \overline{D}.\overline{dS} = Q$ (or in words)

For capacitance $\epsilon \overline{E_r}.\overline{A_r} = Q$

or $E_r = \dfrac{Q}{\epsilon.4\pi r^2}$

So $V = \displaystyle\int_R^{\infty} \dfrac{Q}{4\pi\epsilon}.\dfrac{dr}{r^2} = \dfrac{Q}{4\pi\epsilon}\left[-\dfrac{1}{r}\right]_R^{\infty}$

$= \dfrac{Q}{4\pi\epsilon R}$

But $C = \dfrac{Q}{V}$ so $C = 4\pi\epsilon R$.

9(b)
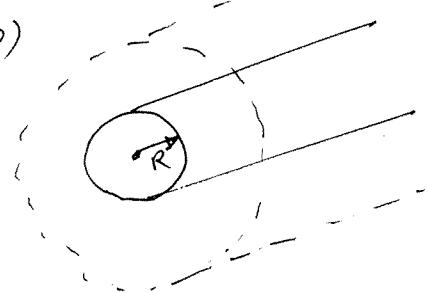
$Q = $ charge/unit length

$\epsilon \overline{E_r}.2\pi\overline{r} = Q$

$\therefore E_r = \dfrac{Q}{2\pi\epsilon}.\dfrac{1}{r}$

Note for interest: try capacitance of isolated wire

$V = \displaystyle\int_R^{\infty} \dfrac{Q}{2\pi\epsilon}.\dfrac{dr}{r} = \dfrac{Q}{2\pi\epsilon}\left[\ln r\right]_R^{\infty}$

ie $V \to \infty$, so not physically meaningful.
You can't have an isolated infinite single
wire in space!

9(c) If several charges are introduced into
a region, their effect is the sum of
their individual effects.

9(c) continued

Using superposition, for just $+Q$ on wire A, voltage between wires is (neglecting charge on second wire)

$$V_+ = \int_R^{d-R} \frac{Q_+}{2\pi\epsilon} \cdot \frac{dr}{r} = \frac{Q_+}{2\pi\epsilon} \cdot \left[\ln r\right]_R^{d-R}$$

$$= \frac{Q_+}{2\pi\epsilon} \cdot \ln\frac{d-R}{R}$$

But the wires are symmetric, and $-Q$ must be induced on wire B, and result in a similar partial voltage.

So: $V_{AB} = 2 \cdot \frac{Q}{2\pi\epsilon} \cdot \ln\frac{d-R}{R}$

or $C_{AB} = \dfrac{\pi\epsilon}{\ln\frac{d-R}{R}}$

9(d) $C/\text{unit length} = \dfrac{\pi\epsilon}{\ln 199} = 5.25 \, pF/m$.

Max. field is at surface of either wire, where

$$\hat{E} = \bar{E}_+ + \bar{E}_- = \frac{Q}{2\pi\epsilon}\left[\frac{1}{R} + \frac{1}{d-R}\right]$$

$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad$ neglect.

$$\therefore \quad \hat{E} = \frac{1}{2\pi\epsilon} \cdot \frac{1}{R} \cdot \frac{\pi\epsilon \hat{V}}{\ln\frac{d-R}{R}}$$

or $\hat{V} = 2R \ln\left(\frac{d-R}{R}\right)\hat{E}$

$\qquad \approx 53 \, kV$.

10 (a) $\oint \overline{H} \cdot \overline{dl} = I$

$\therefore \oint H_I L = I$ or $B_I = \dfrac{\mu_0 \mu_r I}{L}$

$\therefore \phi = \dfrac{\mu_0 \mu_r A I}{L}$

(b) $V = \dfrac{d\Phi'}{dt}$ where $\Phi' = $ flux linkage $= N\Phi$

$\therefore V = N\dfrac{d\Phi}{dt}$.

Let $I = I_0 e^{j\omega t}$

then $\dot{I} = j\omega I$

and $|\dot{\Phi}| = \dfrac{\mu_0 \mu_r A}{L} \cdot \omega \cdot I$

$\therefore V_{rms} = N \dfrac{\mu_0 \mu_r A}{L} \cdot \omega \cdot I_{rms}$

(substituting) $= \pi^2 \cdot 4$

$= 39 \checkmark$

$\mu_0 = 4\pi \cdot 10^{-7}$	$\omega = 2\pi \cdot 50$	$\mu_r = 1000$
$L = 100\,mm$	$N = 100$	$A = 10^{-4}\,m^2$
$I = 1A$		

(c) With dust: $H_I' L + H_A' t = I$

but areas are equal, so $B_I = B_A$, or $\mu_I H_I = \mu_A H_A$

so $H_I' \left[L + \dfrac{\mu_I}{\mu_A} t \right] = I$

or $H_I' = \dfrac{I}{L + \mu_r t}$ $\boxed{c.f. \text{ before} : H = \dfrac{I}{L}}$

$\therefore \%\ error = \dfrac{\mu_r t}{L} \cdot 100 = \dfrac{1000 \cdot 0.01}{100} \cdot 100 = 10\%$

If $\mu_r = 100$, error would be 1%

or could introduce a fixed air gap.

(d) position of wire in yoke is immaterial.

11 (a) $\oint \overline{H} \cdot \overline{d\ell} = NI$

$\boxed{\begin{array}{l} c \equiv \text{Colomax} \\ p \equiv \text{Plastic} \end{array}}$

But if $I = 0$

$H_c L_c + H_p \cdot t \cdot 2 = 0$

But $B_p \doteq B_c$ and $B_p = \mu_0 H_p$

$\therefore H_c L_c + \dfrac{B_c \cdot 2t}{\mu_0} = 0$

or $B_c = - \dfrac{\mu_0 L_c}{2t} \cdot H_c$

$\quad\quad = -3.948 \cdot 10^{-5} H_c$

$(\mu_0 = 4\pi \cdot 10^{-7}, \quad L_c = 0.1\pi, \quad t = 5 \cdot 10^{-3})$

Plot this line on Colomax graph in data book

It crosses the Colomax line at $B_c = 1.29$ Tesla

(b) Using virtual work : $\delta E = F \delta x$

Energy per unit vol. of B_c in air $= \frac{1}{2} B_c H_A$

$\quad\quad\quad\quad\quad\quad\quad = \dfrac{B_c^2}{2\mu_0}$

$\therefore \dfrac{B_c^2}{2\mu_0} \cdot A \cdot \delta x = F \delta x$

$\therefore F = \dfrac{1.29^2 \quad 10^{-4}}{8\pi \cdot 10^{-7}} = 66.2$ Newtons.

c) $\oint \overline{H} \cdot \overline{d\ell} = NI$ again

$\therefore H_c L_c + H_p 2t = NI$

But $B = 0 \Rightarrow H_p = 0$

$\boxed{\begin{array}{l} \text{From graph} \\ H_c = 5.9 \cdot 10^4 \\ \text{when } B_c = 0 \end{array}}$

$\therefore I_{release} = \dfrac{H_c \cdot 0.1 \cdot \pi}{10^4}$

$\quad\quad\quad = 5.9 \cdot 0.1 \cdot \pi$

$\quad\quad\quad = 1.85 A$

d) If I is increased beyond release current, the flux will increase again, and hence the keeper attracted again.

Yes, the current direction does matter.