ENGINEERING TRIPOS PART IA

Tuesday 11 June 2002 9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

*Answer not more than **eight** questions, of which not more than **three** may be taken from Section A, not more than **three** from Section B, and not more than **two** from Section C.*

All questions carry the same number of marks.

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the invigilator

(TURN OVER

SECTION A

Answer not more than three questions from this section.

1 (a) (i) State what assumptions have to be made in order to be able to describe a transformer as ideal. [3]

(ii) An equivalent circuit for a non-ideal transformer is shown on page 20 of the Electrical data book. Explain carefully the origin of the reactance term X_2. [2]

(iii) Identify the magnetising branch on the primary side of the transformer. [2]

(b) The characteristics of a non-ideal transformer are determined by performing tests with the low voltage secondary open and short circuited. The results of one such test are shown below.

Open circuit test

$V_{primary} = 240$ V, $I_{primary} = 0.3$ A, $P = 25$ W, $V_{secondary} = 120$ V

Short circuit test

$V_{primary} = 45$ V, $I_{primary} = 5$ A, $P = 40$ W

Determine the values of the equivalent circuit parameters (referred to the primary side of the transformer). [6]

(c) Operating at mains voltage (240 V, 50 Hz) the transformer in (b) is used to drive a load with resistance of 15 Ω in series with an inductance of 50 mH.

(i) Including these two additional elements draw the overall equivalent circuit for the transformer (with all the elements referred to the primary side). [3]

(ii) Calculate the total VARS and hence or otherwise calculate the size of capacitor required to increase the power factor to unity. [4]

2 (a) State Thevenin's and Norton's Theorems [2]

(b) A voltmeter with an input resistance of 1 kΩ (and calibrated to read RMS directly) is used to measure the voltage between the terminals A and B of the circuit shown in Fig. 1.

(i) Derive the Thevenin equivalent for the circuit. [4]

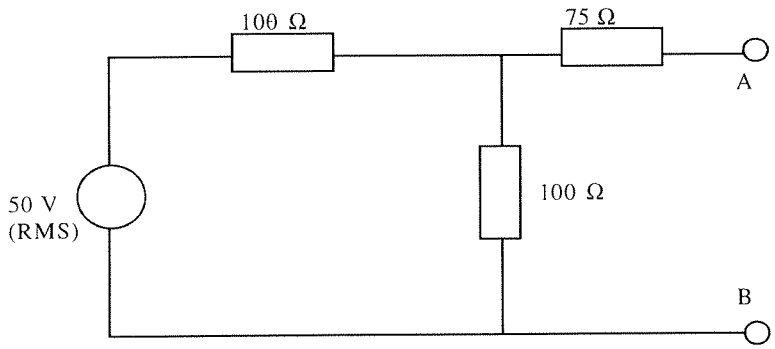

Fig. 1

(ii) Calculate the open circuit voltage (i.e. without the voltmeter in place). [2]

(iii) Hence or otherwise calculate what the measured voltage would be. [2]

(iv) Calculate what the input impedance of the voltmeter would need to be in order to reduce the error to less than 0.5 %. [5]

(c) A stray capacitance of 50 pF is found to exist in parallel with the original voltmeter. Calculate the error in the voltage reading if the voltage source is now 50 V, 0.50 MHz. [5]

3 Consider the amplifier circuit shown in Fig. 2. Assume that the small signal resistance and transconductance of the FET are r_d = 20 kΩ and g_m = 5 mA/V.

(a) What is the role of the coupling capacitors C_1 and C_2? [2]

(b) Draw the small signal equivalent circuit for the amplifier valid at mid-band frequencies. [4]

(c) Assume that the effect of C_1 and C_2 is negligible. Derive expressions for the following quantities in terms of R_1, R_2, R_S, g_m and r_d.

(i) The input impedance, Z_{in}.
(ii) The output impedance, Z_{out}.
(iii) The amplifier gain, v_{out}/v_{in}. [6]

(d) Determine values for R_1, R_2 and R_S, such that Z_{in} = 1 MΩ and Z_{out} = 180 Ω. [6]

(e) The gain of the amplifier is close to 1. Briefly discuss possible uses for this circuit. [2]

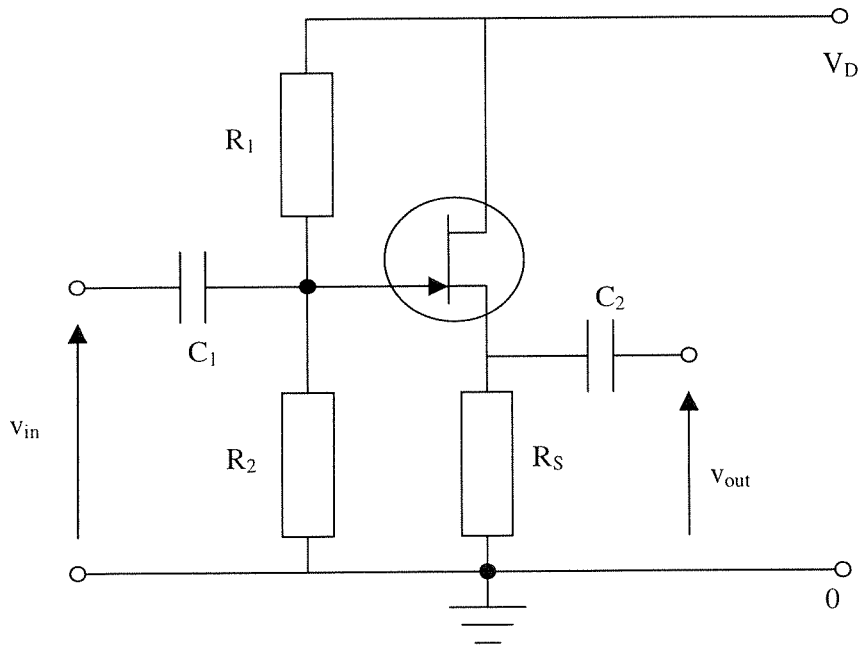

Fig. 2

4 Consider the circuit of Fig. 3, and assume that the operational amplifier is ideal.

(a) State the assumptions made when describing the operational amplifier as ideal. [3]

(b) Sketch a graph of the gain of the circuit against frequency, showing the effect of the inductor on the gain at very low and very high frequencies. [3]

(c) Provide an expression for the gain (v_o / v_i) as a function of R_1, R_2 and L. Determine the values of R_1, R_2 such that at *low frequencies* the magnitude of the gain is 10 and the input impedance is 1 kΩ. [6]

(d) Determine L such that the gain drops to 70% of its low frequency value when the frequency is 10 kHz. [4]

(e) If a signal $v_i = 2 \sin (2\pi\ 10^5\ t)$ is applied to the circuit, the output voltage v_o has the form $v_o = A \sin (2\pi f t + B)$, where t is in seconds. Determine the values of A, f and B. [4]

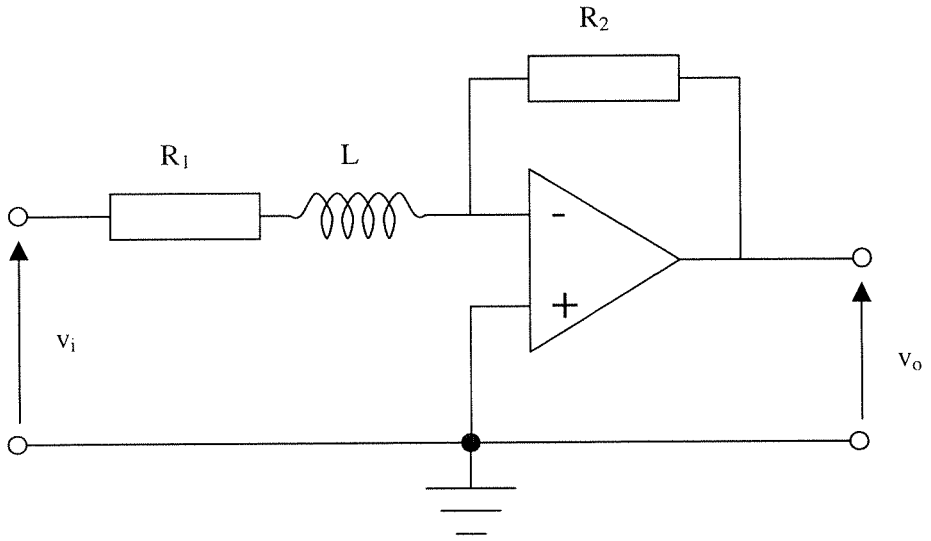

Fig. 3

SECTION B

*Answer not more than **three** questions from this section.*

5 The following program is intended to compute the sum of a set of 2s complement numbers stored in appropriate memory locations.

```
        CLRB
        LDAA $C000
        TSTA
        BLE done
        LDX #$C000
more:   ADDB $01,X
        INX
        DECA
        BNE more
done:   STAB $C000
```

(a) Draw a flow chart to represent the operation of the program. [5]

(b) Describe the operation of the command "ADDB $01,X". What is the addressing mode used? [3]

(c) Write the command "BNE more" in op-code using relative addressing. [3]

(d) The following numbers were stored in the corresponding memory locations at the beginning of the execution of the program.

03	C000
05	C001
0A	C002
1B	C003

(i) How many numbers will the program add? What will be the value stored in memory location $C000 at the end of the execution? [3]

(ii) If the clock frequency of the microprocessor is 2 MHz, how long will the program take to execute? [6]

6 (a) Discuss the differences in function between the following types of memory: RAM, ROM, EPROM, magnetic hard drive. [4]

(b) Determine the binary function implemented by the circuit of Fig. 4. Using Boolean algebra operations simplify the formula and show that the same function can be implemented using a single gate. [4]

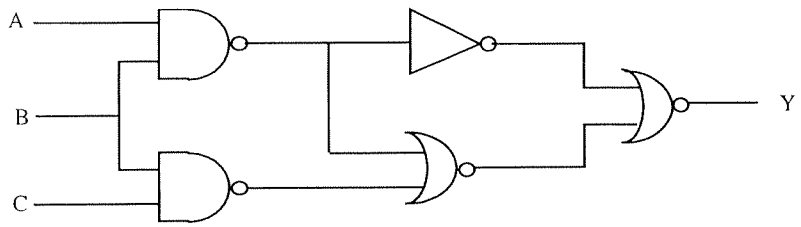

Fig. 4

(c) (i) Give the binary representation of the decimal numbers 0 to 9 as 4 bit binary numbers ABCD. [2]

(ii) On the display of a digital clock, the numbers 0 to 9 are represented by 7 line segments, labelled EFGHIJK as shown in Fig. 5. Letting E = 1 denote "segment on" and E = 0 denote "segment off" leads to a representation of the decimal numbers using 7 bits: number 1 is represented as 0110000, 2 as 1101101, 3 as 1111001, etc. Provide the values of EFGHIJK for the numbers 5 and 7. [2]

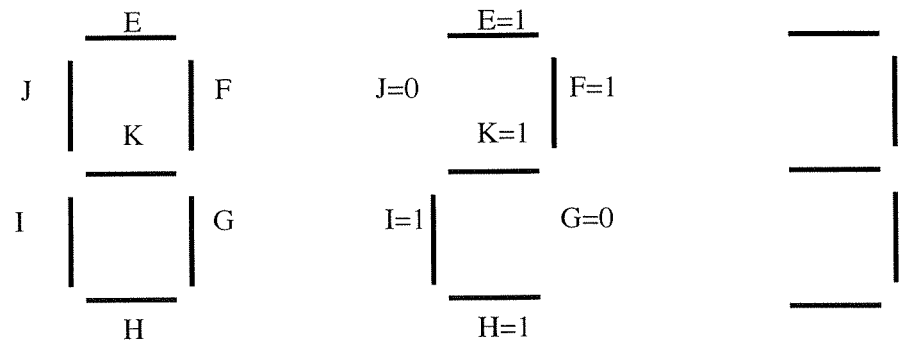

Fig. 5

(iii) Draw two 4 variable Karnaugh maps to relate F and I to ABCD. [4]

(iv) Derive the simplest sum of products formulas for F and I. [4]

7 (a) List the relative merits of NMOS, CMOS, TTL and ECL technologies for the design of digital circuits. [4]

(b) What logic function does the circuit in Fig. 6 perform? Discuss how one can improve the power consumption of the circuit by replacing the resistors by PMOS transistors. Provide the modified circuit diagram. [5]

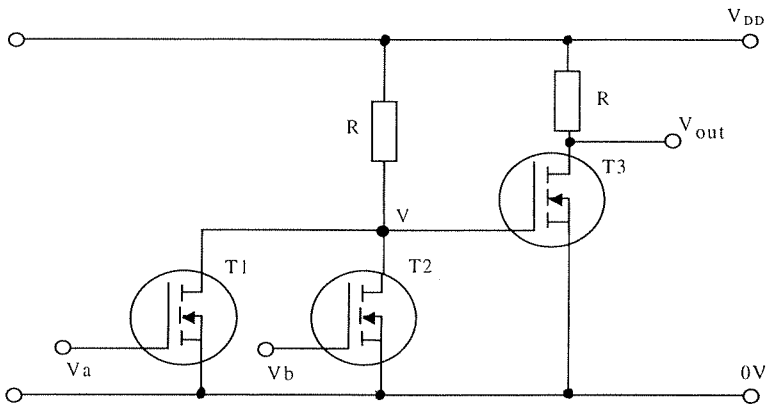

Fig. 6

(c) Explain the function of a one out of 2^n address decoder. Draw a digital circuit that implements a one out of 2^2 decoder using NOT and AND gates. [5]

(d) The digital circuit in Fig. 7 is to be used as a memory element. Briefly explain what the input signals *A*, *L*, *H* and *W* represent, and how the output signal *Y* depends on them. [6]

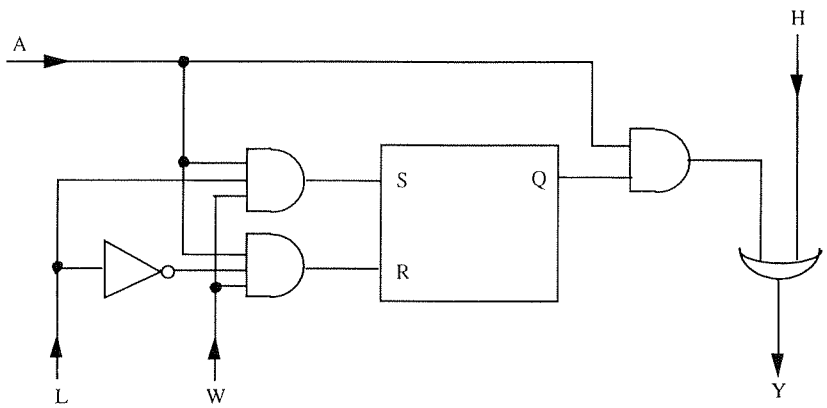

Fig. 7

8 A machine in a manufacturing plant is in one of three states: Idle (denoted by *I*), Working (denoted by *W*) and Down (denoted by *D*). The machine has two binary inputs: "processing" (denoted by *P*) and "malfunction" (denoted by *M*). The state transitions of the machine are summarized in Fig. 8. As usual, *X* stands for "don't care".

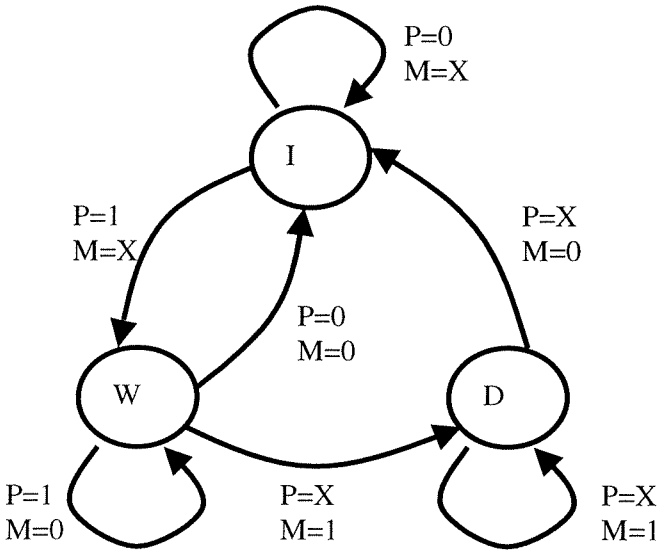

Fig. 8

(a) If we use two bits *AB* to represent the state of the system with $I = 00$, $W = 01$, $D = 10$ how many unused states will there be? Provide the state allocation table. [3]

(b) Assume that all unused states must transition to state *I* at the first clock pulse. Draw a complete state diagram for the process. [4]

(c) A model of the system is to be implemented using two J-K bistables. Determine the logic functions for the inputs J and K of each one. [8]

(d) Draw a complete circuit diagram using AND, OR and NOT gates. [5]

SECTION C

Answer not more than ***two*** *questions from this section.*

9 (a) State Gauss's Law for electrostatics and hence derive an expression for the capacitance of a parallel plate capacitor in which the plates are each of area A and are held apart by a dielectric of relative permittivity ε_r at a distance x. [5]

(b) By considering first the mechanical work done in drawing the plates apart a distance δx when the initial separation is x, and secondly the resultant stored electrostatic energy, derive an expression for the force between the two plates of the capacitor in Fig. 9. [4]

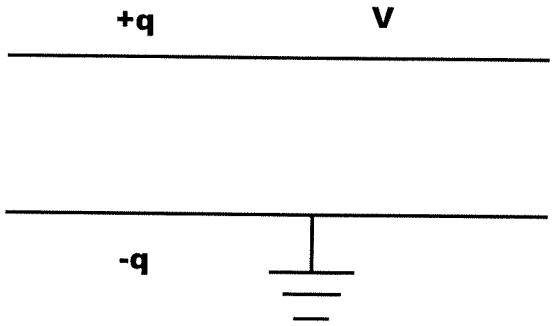

Fig. 9

(c) Calculate the force for the case where $A = 0.1\text{m}^2$, $\varepsilon_r = 5$, $x = 10^{-3}$ m and the potential difference is 10 V. State any assumptions made. [4]

(d) The dielectric material has a Young's modulus E of 100 GPa, an initial thickness of 1 mm, and an ε_r of 1000. Using the expressions derived in parts (a) and (b), or otherwise, calculate the voltage required to produce a strain of 0.5% assuming ε_r is independent of strain. [7]

10 (a) State Ampere's law in integral form and explain its significance. [2]

(b) A magnetic clamp is constructed as shown in Fig. 10. It has a constant cross-sectional area of 100 mm^2 and is constructed from iron with a μ_r of 1000 together with a permanent magnet made from Columax (which is used to hold the clamp shut). The clamp is released by passing current through the coil in order to produce a flux in opposition to that produced by the magnet.

For the case where there is zero current in the coil find the magnetic flux density $\boldsymbol{B}$ at the interface AA due to the remnant flux in the magnet. [7]

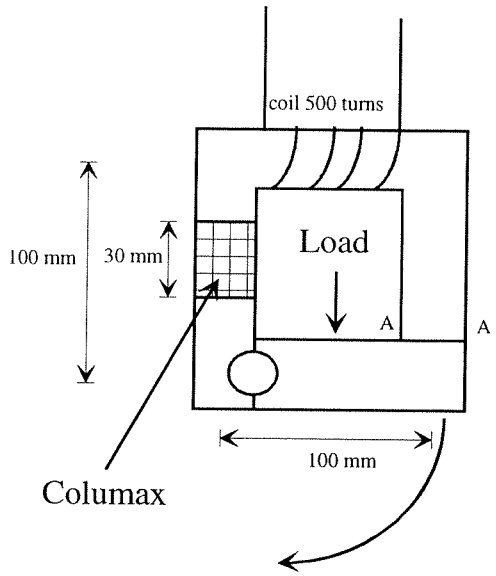

Fig. 10

(c) What current is required in the coil to reduce the flux calculated in (b) to zero. [7]

(d) Assuming that the clamping force due to the magnet acts at the centre of AA and that the load is applied along a line of action which is equidistant from the hinge and the line of action of the clamping force, calculate the maximum load which the clamp will support. [4]

11 (a) What is the Biot-Savart Law ? [3]

(b) Use the Biot-Savart law to show that the magnetic flux density $\boldsymbol{B}$ at a point A at a distance x from the mid point of a short wire, length L, carrying a current I as shown in Fig. 11 is given by

$$\boldsymbol{B} = \frac{\mu_0 LI}{2} \frac{1}{\pi x\left(4x^2 + L^2\right)^{1/2}} \qquad [7]$$

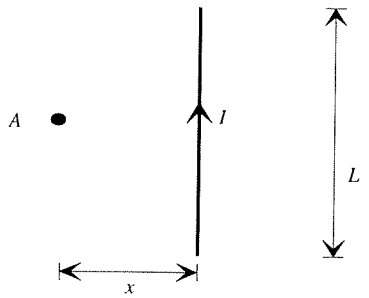

Fig. 11

(c) The magnetic flux density at the centre of a single turn square coil with sides of length L is simply 4 times the answer arrived at in part (b).

Using the above result calculate the magnetic flux density at the centre of the planar square coil with n turns and with inner dimensions a and outer dimensions b shown in Fig. 12. State any assumptions made. [10]

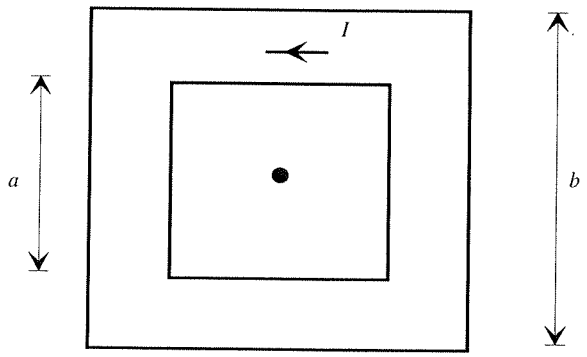

Fig. 12

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