ENGINEERING TRIPOS PART IA

Tuesday 8 June 2004 9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

*Answer not more than **eight** questions, of which not more than **three** may be taken from Section A and not more than **three** from Section B, and not more than **two** from Section C.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

SECTION A

*Answer not more than **three** questions from this section.*

1 (a) Explain what is meant by the term 'ideal op-amp', with particular reference to the gain, input resistance and output resistance. Explain also how the ideal op-amp approximations may be used to simplify the analysis of op-amp circuits. [20%]

(b) In the inverting op-amp circuit shown in Fig. 1, the op-amp may be assumed to be ideal. Derive an expression for the voltage gain in terms of R_1 and R_2. [15%]

(c) If instead the op-amp has finite input resistance, R_i, finite gain A, but is otherwise ideal, show that the voltage gain is given by:

$$\text{Gain} = \frac{-AR_iR_2}{AR_iR_1 + (R_1 + R_2)R_i + R_1R_2}$$

[35%]

(d) With R_i = 10 kΩ , and gain $A = 10^4$, the op-amp circuit of Fig. 1 is to be used to produce a gain of –10. Using the expression for gain obtained in part (c) above, determine the voltage gain for:

(i) $R_1 = 100\ \Omega, R_2 = 1\ \text{k}\Omega$
(ii) $R_1 = 1\ \text{M}\Omega, R_2 = 10\ \text{M}\Omega$ [15%]

(e) Explain why the resistor values of (d) part (i) are appropriate for this application, whereas those of (d) part (ii) are not. [15%]

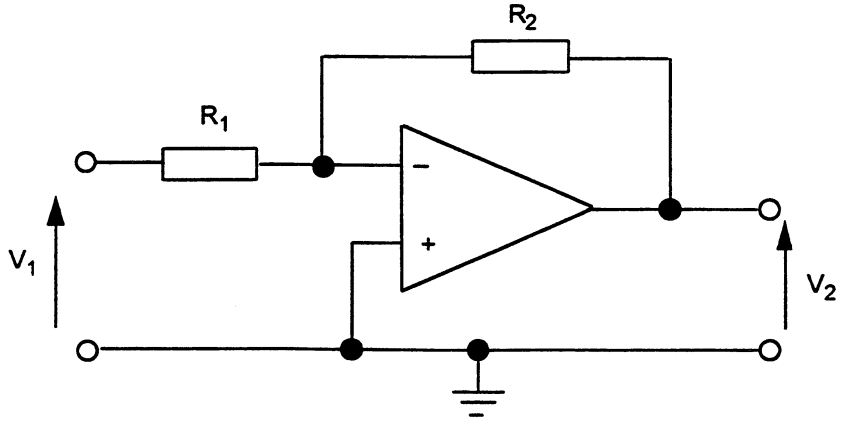

Fig. 1

2 (a) The JFET amplifier shown in Fig. 2 is to be biased so that V_{GS} = –2 V, V_{DS} = 9V, I_D = 4 mA, and it is to have input resistance (to an input small-signal voltage at a mid-band frequency) of 1 MΩ. Determine values for resistors R_1, R_2 and R_3. [25%]

(b) The JFET has small-signal parameters r_d = 10 kΩ and g_m = 5 mS, and the load resistor R_L is 1 kΩ. Draw the small signal circuit for the amplifier valid for mid-band frequencies, and hence determine its mid-band voltage gain. [25%]

(c) Explain why the capacitor C_1 will cause the gain to be attenuated for low frequencies, and find the value of C_1 required if the gain is to fall to 70 % of its mid-band value at a frequency of 10 Hz. You may assume that the reactances of the other capacitors in the circuit are negligible at this frequency. [35%]

(d) If R_L may be set to any value, determine the value required for maximum signal power to be consumed by the load, assuming a 1 kHz input voltage. [15%]

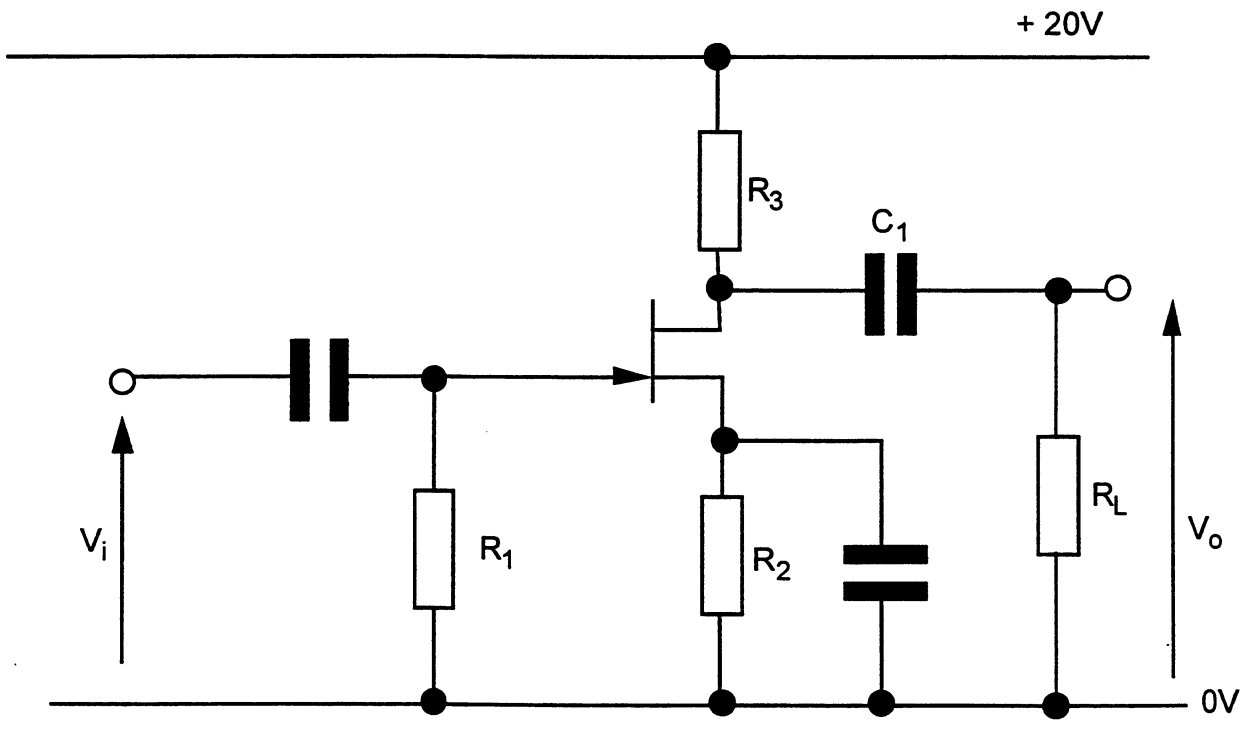

Fig. 2

3 (a) Explain what is meant by the Thevenin equivalent circuit for a linear circuit. Draw the Thevenin equivalent circuit for the circuit shown in Fig. 3a, and derive expressions for the Thevenin voltage and impedance. [25%]

(b) In the circuit of Fig. 3b, R = 100 Ω, L = 31.8 mH, and C = 159 μF. By applying Thevenin's theorem to this circuit, or otherwise, determine the rms magnitude of the current flowing in the capacitor C, its peak value, and also its phase with respect to the 100 V voltage source. [35%]

(c) The capacitor C is now altered to give a resonant frequency for the circuit of 50 Hz. Find the new value of capacitor C, and determine the rms magnitude of the capacitor voltage, and its phase with respect to the 100 V voltage source. [30%]

(d) Explain physically why the magnitude of the capacitor voltage at resonance is much greater than the 100 V supply voltage. [10%]

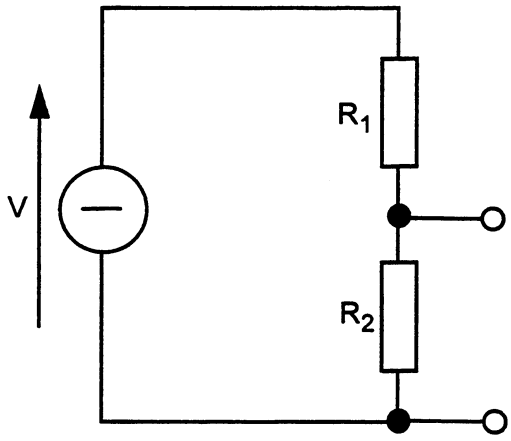

Fig. 3a

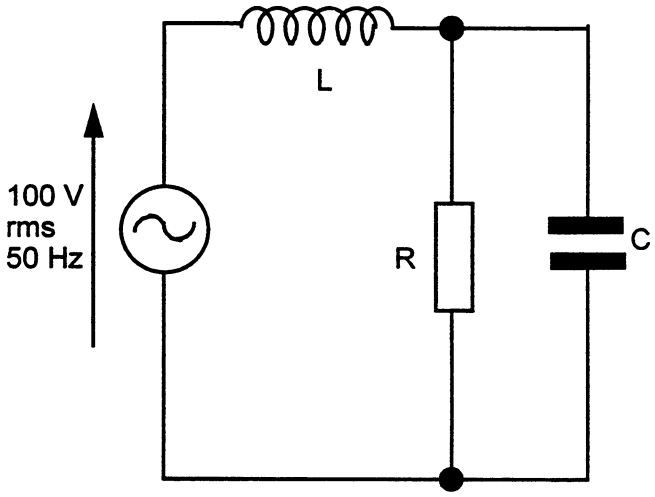

Fig. 3b

4 (a) Explain what is meant by the term 'ideal transformer', and explain the physical significance of the equivalent circuit parameters R_1, R_2, X_1, X_2, R_0 and X_0 in the non-ideal transformer equivalent circuit given in the Electrical and Information Data Book. [25%]

(b) A transformer with equivalent circuit parameters (all referred to the primary) of $R_1 = R_2' = 1\ \Omega$, $X_1 = X_2' = 2\ \Omega$, $X_0 = 50\ \Omega$, $R_0 = 100\ \Omega$, and with turns ratio $N_1:N_2$ of 10:1 has its primary winding connected to a 240 V, 50 Hz ac supply. If the transformer has its secondary winding connected to a load of (0.1+j0.05) Ω, determine:

(i) the load current referred to the primary;
(ii) the load real power and reactive power;
(iii) the input real power and reactive power;
(iv) the transformer input current and input power factor;
(v) the transformer efficiency.

You may use the approximate transformer equivalent circuit shown in the Electrical and Information Data Book, in which R_0 and X_0 are shown connected directly to the primary input voltage supply. [60%]

(c) Determine the value of capacitor which, when connected across the transformer primary winding input terminals, will cause the current drawn from the 240 V supply to be in phase with the 240 V supply voltage. [15%]

SECTION B

*Answer not more than **three** questions from this section.*

5 A combinational logic circuit is required which takes four inputs, A, B, C and D, and gives an output Z of '1' only if two or more inputs is a logic '1', and zero otherwise.

(a) Construct a Karnaugh map which expresses the output in terms of the four inputs. [20%]

(b) Use your Karnaugh map to derive both sum of products, and product of sums expressions for the output in terms of the four inputs. [30%]

(c) Using De Morgan's theorem derive expressions for the output that could be implemented using

(i) NAND gates only, and
(ii) NOR gates only.

Determine the number of logic gates required in both cases. You may assume that gates are available with any number of inputs. Which of the two implementations appears to be the best, assuming that only NAND gates or NOR gates are available? [30%]

(d) More realistically, integrated circuits are available with four 2-input NAND gates per chip, or four 2-input NOR gates per chip. It may be shown that 17 2-input NOR gates are required to implement the solution to (c) part (ii) above. Determine the number of 2-input NAND gates required to implement your solution to (c) part (i). Hence determine the total number of integrated circuits required in each case and comment on your result. [20%]

6 (a) A 3 bit Johnson counter is formed by connecting the input of a 3 bit shift register to the complement of its output, as shown in Fig. 4.

(i) Show that two possible state sequences exist, and list them both.

(ii) If the 3 bit shift register is formed from three J-K flip-flops, explain how the $\overline{CLR}$ inputs to the flip-flops may be used to ensure that, when power is initially applied to the circuit, the output is initialised to 000. [30%]

(b) Instead it is desired for the three flip-flops to be used to perform a count of 8, in which the state sequence increases monotonically from 000 to 111, and then returns to 000.

(i) Construct a table in which each row shows the present state, the next state, and the J-K inputs required for each bistable.

(ii) Using Karnaugh maps, or otherwise, determine simplified expressions for the J-K inputs for all the bistables.

(iii) Hence draw a circuit for the counter. [70%]

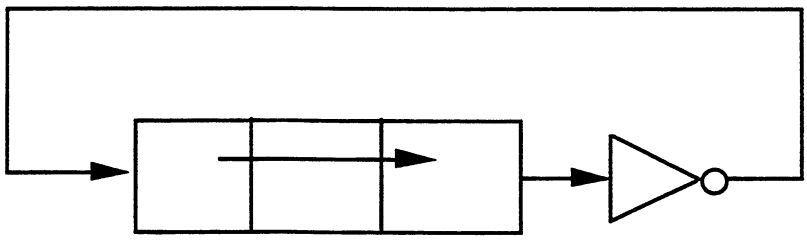

Fig. 4

7 (a) The Motorola 6800 microprocessor has an 8 bit data bus, and a 16 bit address bus.

(i) Explain the terms 'data bus' and 'address bus'. [10%]

(ii) Random access memory uses bistable circuits to store a single bit of data. Calculate the number of such bistables required for an integrated memory circuit which has an 8 bit data bus and a 13 bit address bus, and also express the capacity of this memory device in kbytes. [15%]

(iii) Determine the number of such memory circuits which may be connected to the 6800 microprocessor, and show how you would connect the $\overline{CS}$ signal for the memory device in the address range A000 to BFFF to the address bus of the 6800. [25%]

(b) (i) Explain how the most significant bit of an 8 bit number is used to denote negative numbers in 2's complement notation, and convert the following hexadecimal numbers to decimal, assuming 2's complement notation:

FF, 8C, 3B

Also write down the hexadecimal, binary, and decimal values for the most positive and most negative 2's complement numbers. [25%]

(ii) Convert the decimal numbers –53 and –115 to 2's complement binary form, and using binary addition, add them together, bit by bit, noting carefully the occurrence of any carries. If the 6800 microprocessor was used to perform the addition using the ABA instruction (assuming that the two numbers were initially stored in accumulators A and B) derive the status of the V flag in the condition code register. Explain your result. [25%]

8 The program below is designed to take a list of numbers stored in memory locations $1000 to $100F, and store only the even numbers in an area of memory extending from $1010 to $101F. As well as the program, a partially completed set of hexadecimal op-codes, the number of program bytes and clock cycles required for them, and the address in memory where these op-codes are stored is also given.

	Mnemonic	Op-code	Bytes (#)	Clock cycles (~)	Address
	LDX #$1000	CE 10 00	3	3	0000
next	LDAA 0,X	B6 00	2	5	0003
	LDAB 0,X	E6 00	2	5	0005
	RORB	56	1	2	0007
	BCS label				
	STAA 10,X				
label	INX				
	CPX #$1010				
	BEQ end				
	JMP next				
end	....				

(a) Explain how the RORB instruction combined with the BCS instruction is used to distinguish between odd and even numbers, and hence explain the overall operation of the program. [30%]

(b) Complete the list of op-codes, program bytes, clock cycles and addresses given above for the whole program, paying careful attention to the addressing modes used, and to the calculation of the branch offsets used with the BCS and BEQ instructions, as well as the address used with the JMP instruction. [50%]

(c) If there is an equal number of odd and even numbers in the memory locations between $1000 and $100F, calculate the time taken to execute the program assuming an 8 MHz clock. [20%]

SECTION C

*Answer not more than **two** questions from this section.*

9 (a) A capacitor comprising a horizontal pair of closely spaced parallel metallic plates is filled with oil of relative permittivity 2.2 . The capacitor is charged to 50 volts, then electrically isolated, then the oil is replaced by air. What is the potential difference between the plates of the capacitor? [30%]

(b) Oil is now allowed between the plates so that one plate is covered with a layer of oil whose thickness equals half the spacing between the plates. Determine the ratio of the capacitance of this configuration to the capacitance of the same plates when filled with air. [35%]

(c) The capacitor is now filled entirely with oil, charged to 50 volts and electrically isolated, but a small hole is found in the lower plate of the capacitor. What will be the thickness of the oil layer when it stops leaking? The density of the oil is 1500 kg m^{-3} and the distance between the two plates of the capacitor is 1 mm. [35%]

Hint: The oil stops leaking when the total stored energy in the system (electrostatic energy, and gravitational potential energy of the oil) is a minimum.

10 (a) Derive an expression for the capacitance between two parallel metal plates of area A separated by a distance d. [20%]

(b) Derive an expression for the capacitance of an isolated metal sphere of radius r_0. [40%]

(c) Derive an expression for the capacitance per unit length between an infinitely long metal cylinder of radius a, and an infinite flat metal plate parallel to the axis of the cylinder at a distance s where $s >> a$. [40%]

11 (a) A soft iron bar is placed touching the ends of a C-shaped soft iron bar as shown in Fig. 5, in which all dimensions are in mm. The relative permeability of both bars is fixed at 1000. What is the magnetic flux density at the centre of the straight bar if a current of 5A is passed through the coil? [30%]

(b) The straight and curved bar are now separated so that there is a gap of 1mm between the two. What now is the magnetic flux density at the centre of the straight bar? [35%]

(c) If the weights of the straight bar and coils are negligible, what weight can be suspended from the straight bar (assuming that it is in contact with the curved bar) without it being pulled from the curved bar? [35%]

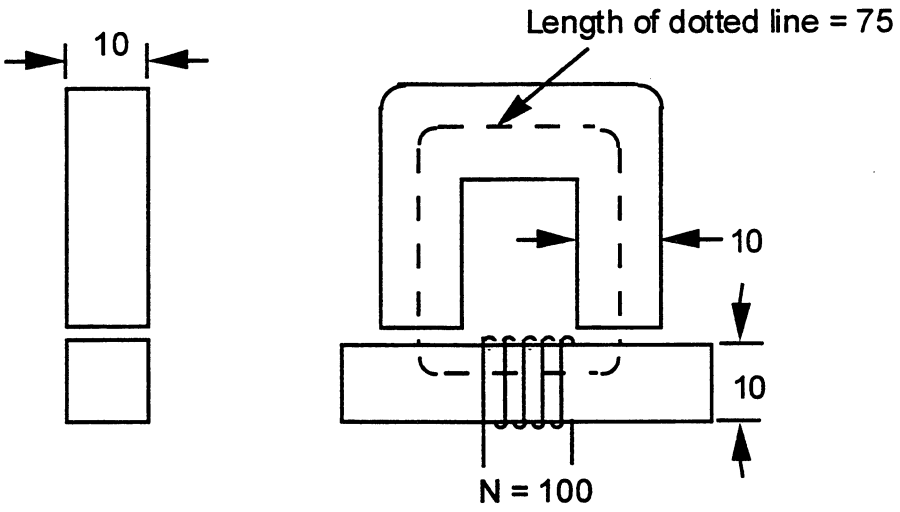

Fig. 5

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