2005 Part IA Engineering, Paper 3 (Electrical and Information Engineering)

Section A (Linear Circuits) **Dr T J Flack**

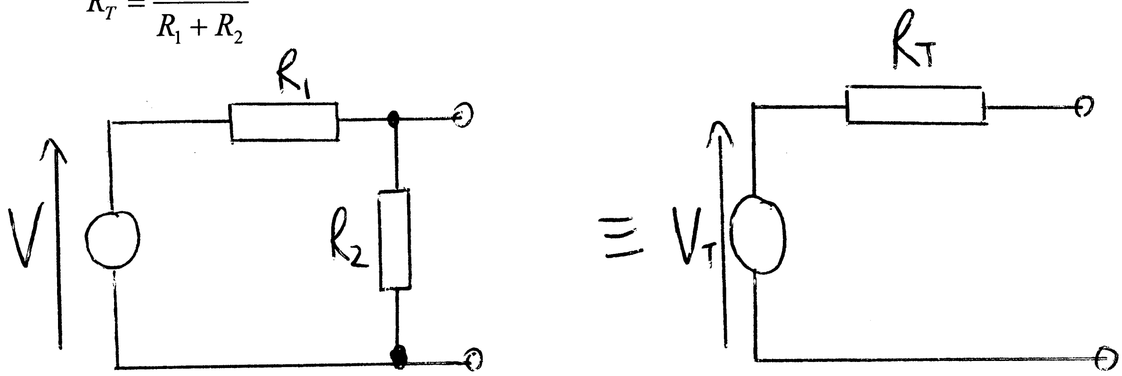
Paper 3 Section A Crib

1. The Thevenin equivalent circuit of a potential divider is shown below, in which V_T is the open circuit voltage of the potential divider

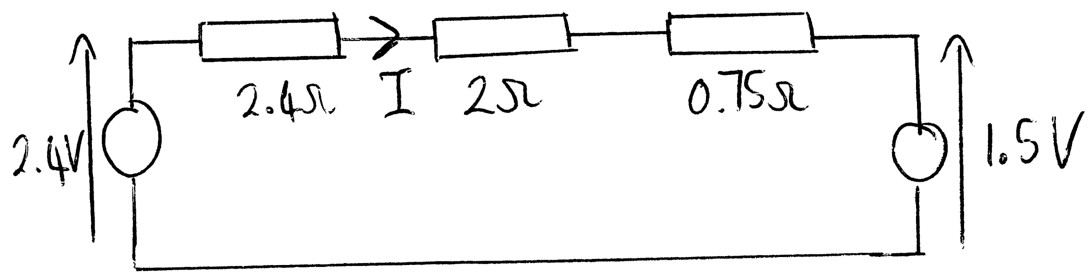
$$V_T = \frac{R_2}{R_1 + R_2} V$$

and R_T is the resistance between the output terminals with all sources of excitation set to zero. In this case, R_1 and R_2 would be in parallel across the output terminals, so

$$R_T = \frac{R_1 R_2}{R_1 + R_2}$$



Applying these ideas to the original circuit, the potential dividers at the left and right hand sides of the circuit may be redrawn so that as far as the 2 Ohm resistor is concerned the circuit becomes

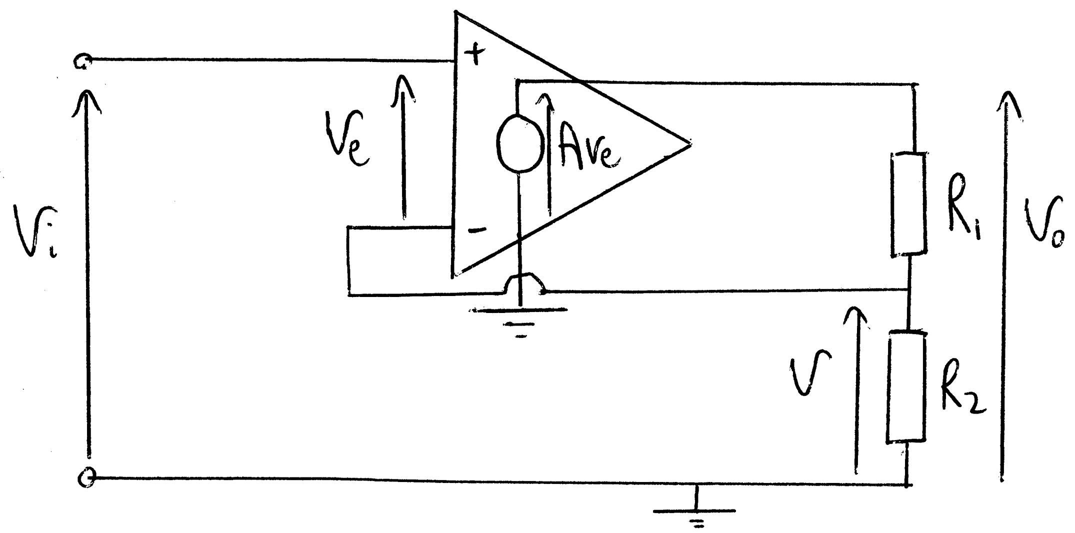


The required current is then the loop current of this circuit:

$$I = \frac{2.4\text{-}1.5}{2.4 + 2 + 0.75} = \frac{0.9}{5.15} = 0.175 \text{ A}$$

2. Op-amp is ideal except for the finite gain, A. Therefore there is a potential between the non-inverting and inverting inputs of v_e, such that:

$$v_0 = Av_e \qquad (1)$$



Since no current flows into the inverting input, resistors R_1 and R_2 act as a potential divider across the output voltage, so that:

$$v = \frac{R_2}{R_1 + R_2} v_0$$

and

$$v_e = v_i - v = v_i - \frac{R_2}{R_1 + R_2} v_0 \qquad (2)$$

Combining (1) and (2):

$$\frac{v_0}{A} = v_i - \frac{R_2}{R_1 + R_2} v_0$$

Rearranging

$$\frac{v_o}{v_i} = \frac{A(R_1 + R_2)}{R_1 + R_2 + AR_2}$$

As A tends to infinity (ideal op-amp case) the denominator tends to AR_2, and so the expression tends to:

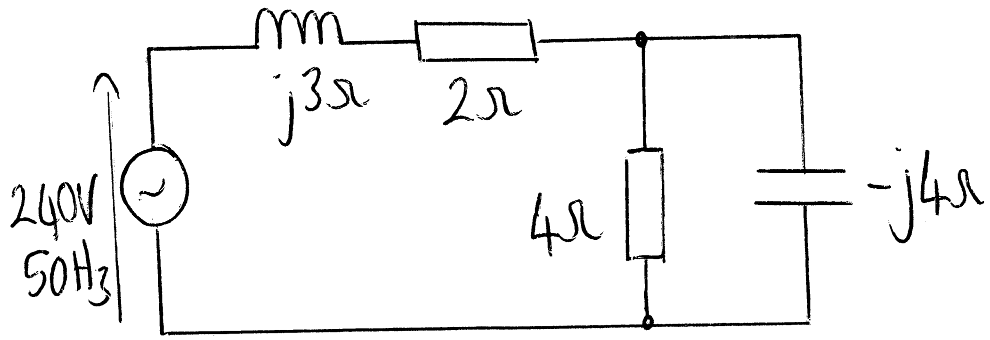
$$\frac{v_o}{v_i} = \frac{R_1 + R_2}{R_2} = 1 + \frac{R_1}{R_2}$$ as required.

3. Impedance of the inductor is

$$\overline{Z}_L = j\omega L = j2\pi fL = j2\times\pi\times 50\times 9.55\times 10^{-3} = j3\,\Omega$$

Impedance of the capacitor is

$$\overline{Z}_C = \frac{1}{j\omega C} = \frac{-j}{2\pi fC} = \frac{-j}{2\times\pi\times 50\times 796\times 10^{-6}} = -j4\,\Omega$$



Combining the 4 Ω resistor in parallel with the capacitor gives

$$\overline{Z} = \frac{-j4\times 4}{4-j4} = \frac{-j4}{1-j} = \frac{-j4(1+j)}{(1-j)(1+j)} = -j2(1+j) = 2-j2\,\Omega$$

Therefore total impedance is

$$\overline{Z}_T = 2+j3+2-j2 = (4+j1)\,\Omega = \sqrt{4^2+1^2}\angle\tan^{-1}(1/4) = 4.12\angle 14^0\,\Omega$$

Current is the found from Ohm's Law

$$\overline{I} = \frac{\overline{V}}{\overline{Z}_T} = \frac{240}{4.12\angle 14^0} = 58.2\angle -14^0\ \text{A}$$

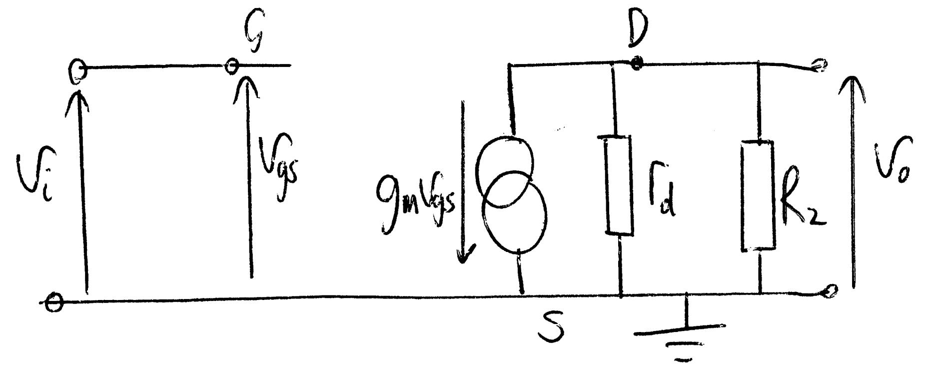
4. a) The capacitor C1 is an open-circuit to dc, and there is no gate current into the FET. Therefore, there is no current flowing through the 1 MΩ resistor, so no voltage across it, so the gate is tied to 0 V dc. The source resistor R_1 has a voltage $R_1 I_D$ across it, and so $V_{GS} = - R_1 I_D$ which biases the FET into its linear region providing suitable choices are made for R_1 and I_D.

b) $R_1 I_D = 4 \Rightarrow R_1 = \frac{4}{I_D} = \frac{4}{4\times10^{-3}} = 1\,k\Omega$

Voltage at the drain is 4 + V_{DS} = 4 + 8 = 12 V, and so the voltage across R_2 is 8 V.

Therefore, $R_2 I_D = 8 \Rightarrow R_2 = \frac{8}{I_D} = \frac{4}{4\times10^{-3}} = 2\,k\Omega$

c) For the small-signal equivalent circuit, all capacitors are treated as short circuits, and all points at a fixed potential are short-circuited to ground:



The small-signal equivalent circuit shows that

$v_{gs} = v_i$ and $v_0 = -g_m v_{gs} \frac{r_d R_2}{r_d + R_2}$

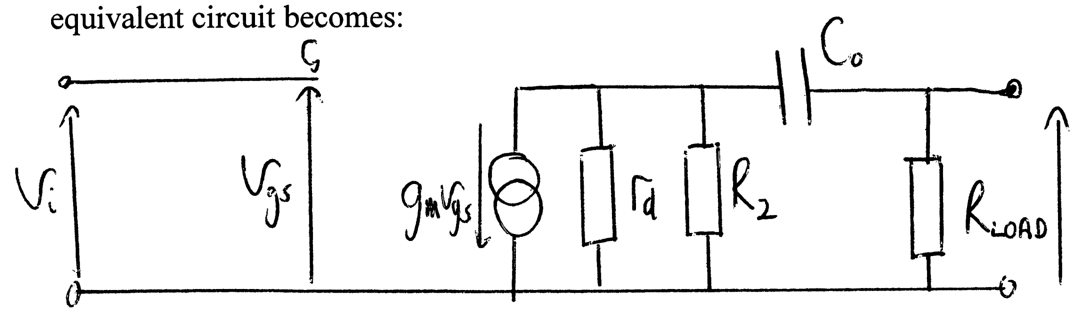
Therefore, Gain = $\frac{v_0}{v_i} = -g_m \frac{r_d R_2}{r_d + R_2} = -5\times10^{-3} \times \frac{10\times10^3 \times 2\times10^3}{10\times10^3 + 2\times10^3} = -8.33$

Output resistance is found by setting input voltage to zero, and calculating the current which would flow into the output of the circuit when a voltage is applied across the output:

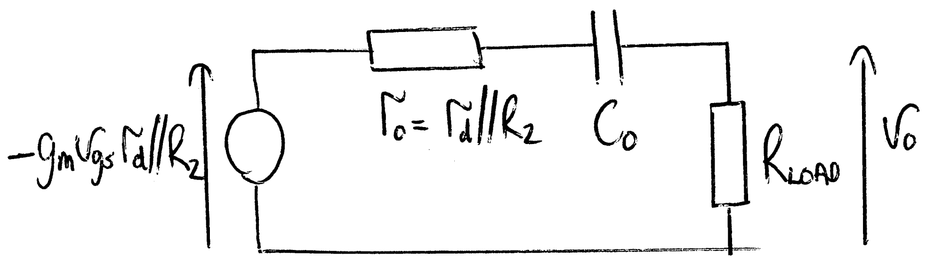
$$R_{out} = \frac{v_o}{i_o}\bigg|_{v_i=0}$$

With $v_i = 0$, $i_o = \frac{v_o}{r_d} + \frac{v_o}{R_2}$ so $\frac{v_0}{i_o} = \frac{r_d R_2}{r_d + R_2} = 1.67\,k\Omega$ ie the output resistance is the parallel combination of r_d and R_2.

d) With the capacitor C_0 and load resistor of 5 kΩ connected, the small-signal equivalent circuit becomes:



Converting the Norton circuit consisting of the current source $g_m v_{gs}$ in parallel with r_d and R_2 to its Thevenin equivalent gives:



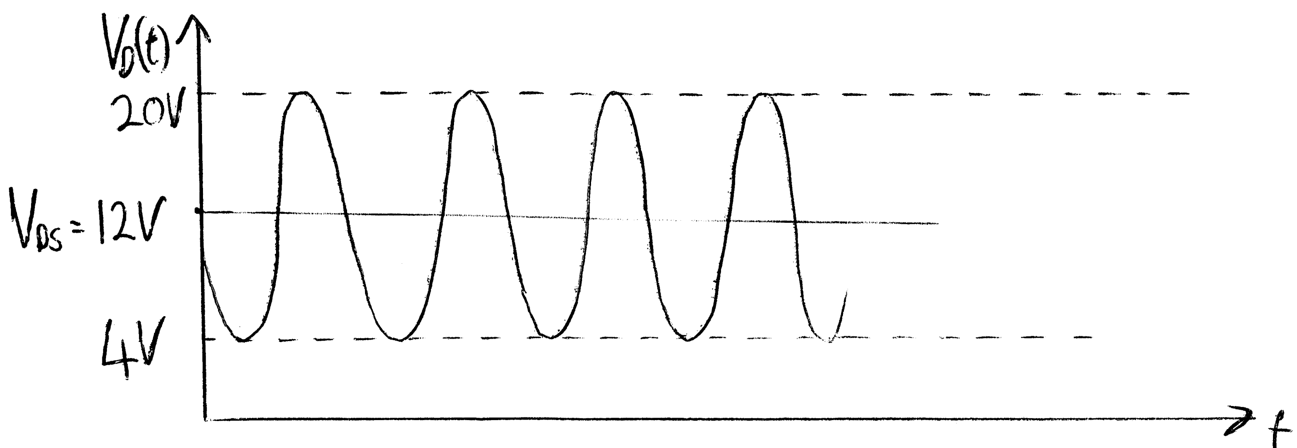
The output voltage is then obtained by the potential divider action of the load resistor with the output resistance of the amplifier and the capacitor impedance:

$$v_0 = \frac{R_{LOAD}}{r_o + \dfrac{1}{j\omega C_0} + R_{LOAD}} g_m v_i r_o \quad \text{and so Gain} = \frac{R_{LOAD}}{r_o + \dfrac{1}{j\omega C_0} + R_{LOAD}} g_m r_d$$

To find the 3 dB point, equate magnitudes of the real and imaginary parts of the denominator

$$(1.67+5)\times 10^3 = \frac{1}{2\times\pi\times 10\times C_0} \Rightarrow C_0 = 2.39\mu\, F$$

e) For maximum voltage swings across the load, the voltage at the drain of the FET must be set midway between the maximum and minimum voltages that point can attain. The maximum voltage at the drain is 20V (when $I_D = 0$) and the minimum is 4 V (when the FET is fully on, so that $V_{DS} = 0$, the voltage at the drain will be the same as the source voltage which is 4V). Therefore, having a drain voltage of 12 V meets this requirement, allowing 8 V swings in both directions, and a V_{DS} of 8 V achieves this.



5. Factory consumes 100 kW at a lagging power factor of 0.85

$P = VI\cos\varphi \quad \Rightarrow \quad 100\times10^3 = 1000\times I\times 0.85$ giving I = 117.6 A

Feeder power loss is

$P_f = I^2 R_f = 117.6^2 \times 0.5 = 6.91\,\text{kW}$

Feeder reactive power is

$Q_f = I^2 X_f = 117.6^2 \times 1.5 = 20.7\,\text{kVAr}$

Load reactive power is found using the power triangle as

$Q_L = P_L \tan\varphi = 100\times10^3 \tan\cos^{-1} 0.85 = 62.0\,\text{kVAr}$

Applying conservation of real and reactive power, the total real power and total reactive power supplied by the voltage source at the sending end is

$P_T = P_L + P_f = 100 + 6.91 = 106.91\,\text{kW}$

$Q_T = Q_L + Q_f = 62.0 + 20.7 = 82.7\,\text{kVAr}$

Total apparent power from the sending end is found using the power triangle

$S_T = \sqrt{P_T^2 + Q_T^2} = \sqrt{106.91^2 + 82.7^2} = 135.2\,\text{kVA} = V_{SEND} I = V_{SEND} \times 117.6$

giving V_{SEND} = 1.149 kV

ii) The capacitor must generate an amount of reactive power equal to that consumed by the load, which is 62.0 kVAr. Therefore:

$$\frac{V_L^2}{X_C} = 62000 \quad \Rightarrow \quad \omega C V_L^2 = 62000 \quad \Rightarrow \quad C = \frac{62000}{2\pi\times 50\times 1000^2} = 197\,\mu\text{F}$$

New feeder current is given by $V_L I = 100\times10^3 \quad \Rightarrow \quad I = \dfrac{100\times10^3}{1000} = 100\text{ A}$

New feeder loss is $P_f = I^2 R_f = 100^2 \times 0.5 = 5\,\text{kW}$

iii) Correcting the load power factor to unity means that the load takes less current. This means that:

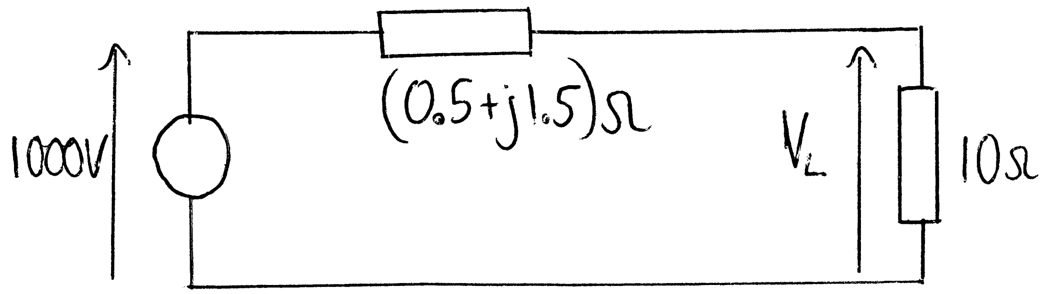
a) The power lost in transmitting the power is reduced.

b) The voltage required to transmit the power is also reduced, so the ratings of the generators, transformers etc in the power supply network can be reduced, and will cost less.

iv) With the power factor correction capacitor still connected, the combined impedance of the load in parallel with the capacitor must be purely resistive, since no reactive power is consumed or generated by this combination. Since it is known that the load consumed 100 kW of real power with a voltage across it of 1 kV, the load may be thought of as being a resistor given by:

$$\frac{V_L^2}{R_L} = 100\times10^3 \text{ so that } R_L = \frac{1000^2}{100\times10^3} = 10\,\Omega$$

connected in parallel with an inductor. However, the value of the inductor doesn't matter, since it is known that the capacitor value has been chosen so that the load, including the parallel capacitor, is purely resistive. Therefore, the system may be drawn as:



The factory voltage may now be found by the potential divider action of the factory equivalent impedance and the feeder impedance:

$$V_L = \frac{R_L}{|R_L + R_f + jX_f|}V_{SEND} = \frac{10}{|10+0.5+j1.5|}\times1000 = 943\text{ V}$$

6.

LDAA #3	Load ACC A with 3 (immediate addressing)
ADDA #6	add 6 to contents of ACCA (ie now has contents 9) - immediate
LDAB #8	load ACCB with 8 (immediate)
STAA $30	store contents of acc A in $0030 (direct)
INCB	increment (ie add 1) to contents of ACCB - now contains 9 (implied)
CMPB $30	compares contents of ACCB with contents of loc^n $0030 -> contents of ACCB unaffected (direct)

Contents of	ACCA	9
" "	ACCB	9

7. ~~2~~ from data book 20 ≡ BRA (branch always)

Addressing is relative for BRA

$0004 ←
$0005
$0006
$0007
$0008
$0009
$000A
⋮ × 15 locations
$001A 20
$001B

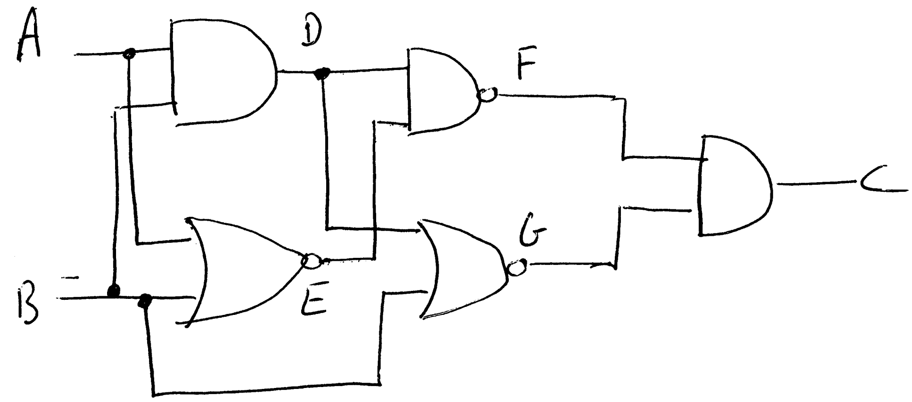
back 23 locations so want −23 as contents of $001B

~~$0~~ 23 is ~~0~~ $17 in HEX or ~~00001100~~ 00010111

negative in 2-s complement is complement + 1

or 11101000 or **$E8**

8.

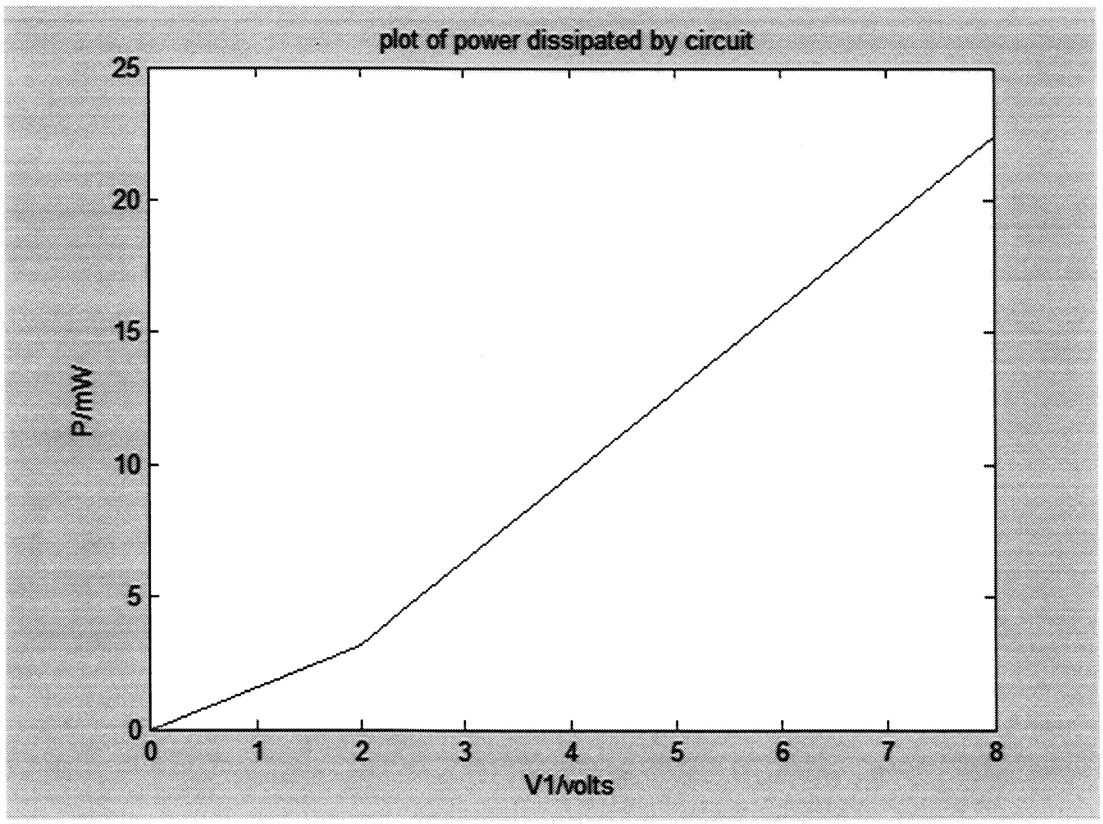


Inputs		Intermediate Values				Output
A	B	$D = A \cdot B$	$E = \overline{A+B}$	$F = \overline{D \cdot E}$	$G = \overline{B+D}$	$C = F \cdot G$
0	0	0	1	1	1	1
0	1	0	0	1	0	0
1	0	0	0	1	1	1
1	1	1	0	1	0	0

9 (a) $V_2 = \frac{8 - I_{DS}}{2500}$ so at $V_2 = V_{DS} = 0$, $I_{DS} = 0.32$mA, at $V_{DS} = 8$, $I_{DS} = 0$. Plot a line between these two points on Fig. 7(b) and read off the value of V_{DS} when $V_1 = V_{GS} = 2$V to get $V_2 = 7.1$ volts.

(b) The power dissipated by the circuit equals the voltage across the circuit times the current through it, so $P = 8I_{DS}$. From the plot on Fig. 7(b), read off values of I_{DS} versus V_{GS} and hence plot P versus V_1.

V_1	I_{DS}/mA	P/mW
2	0.4	3.2
4	1.2	9.6
6	2	16
8	2.8	22.4



(c) The drain/source voltages across the two transistors must sum to 8 volts while the drain currents must be equal though opposite. A simple way to depict this graphically is to plot PMOS and NMOS characteristics on a single pair of axes by

- negating V_{DS} for the PMOS plot
- shifting the origin of the PMOS characteristics to 8 volts beyond that for the NMOS plot.

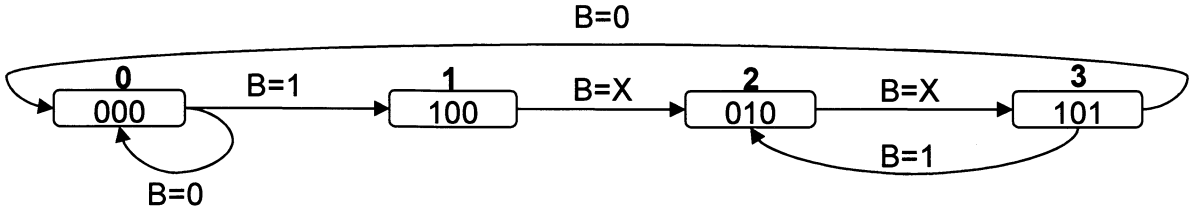
The gates of the two transistors are joined such that if V_{GS} for the NMOS transistor is 2,4, 6 or 8, then V_{GS} for the PMOS transistor must be -6,-4, -2 or 0 respectively. Plot the points where these characteristics for each transistor coincide, and one has the operating profile of the circuit. An actual plot of V_2 (= V_{DS}) versus V_1 = (V_{GS}) should be drawn on separate axes.

(d) Little current flows when V_1 is at either extreme so if used as a logic gate, the new circuit will dissipate less power than before, mostly when switching between logic states.

Examiner's comments: Question was attempted by 230 (78%) of candidates and average mark was 18/30. Section (a) was answered well, less so sections (b) and (c). A minority of candidates realized that the power dissipation in section (b) is simply the product of supply voltage and drain current, and many found it by the correct but more complicated route of summing dissipation in resistor and transistor.

10.

(a)



(b) The number of states equals 2n where n equals the number of bistables. There are only 4 possible states, so n=2.

(c)

State	a	B	H	S	F
0	0	0	0	0	0
1	0	1	1	0	0
2	1	0	0	1	0
3	1	1	1	0	1

By inspection, H=a, $S = a.\overline{b}$, F=a.b

B	Previous state		Next state		J_a	K_a	J_b	K_b
	a	b	a	b				
0	0	0	0	0	0	X	0	X
1	0	0	0	1	0	X	1	X
0	0	1	1	0	1	X	X	1
1	0	1	1	0	1	X	X	1
0	1	0	1	1	X	0	1	X
1	1	0	1	1	X	0	1	X
0	1	1	0	0	X	1	X	1
1	1	1	1	0	X	0	X	1

$J_a = Q_b$

$B \backslash Q_aQ_b$	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$K_a = \overline{B}.Q_b$

$B \backslash Q_aQ_b$	00	01	11	10
0	X	X	1	0
1	X	X	0	0

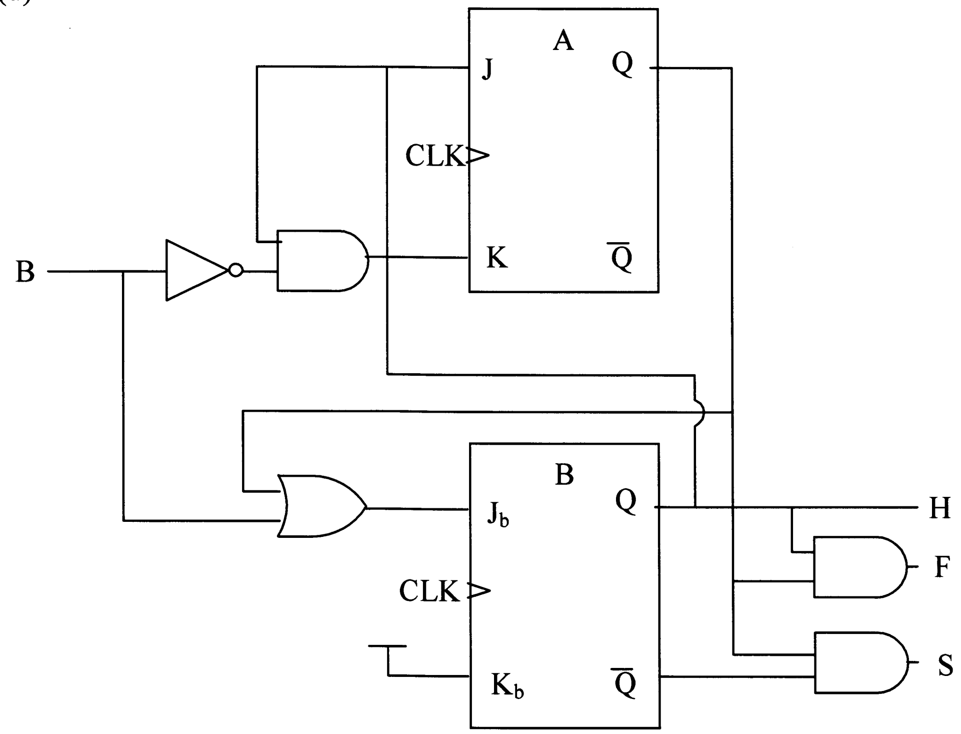
$J_a = Q_a + B$

B\Q$_a$Q$_b$	00	01	11	10
0	0	X	X	1
1	1	X	X	1

$K_b = 1$

B\Q$_a$Q$_b$	00	01	11	10
0	X	1	1	X
1	X	1	1	X

(d)



Examiner's comments: Question was attempted by 271 (92%) candidates and average mark was 21. About a third of candidates correctly noted that 2 bistables are sufficient, but a surprising fraction went on to design a system with 3 bistables. Otherwise the question was answered correctly.

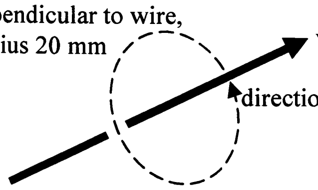
11.

The electromagnetic equations tell us that $\mathbf{B} = \mu\mathbf{H}$ and that $\oint_c \mathbf{H.dl} = \int_s (\mathbf{J} + \dot{\mathbf{D}})\mathbf{dS}$. By symmetry, the direction and strength of magnetic field (**H**) is constant along a circle drawn round the wire. Through this circle there is no rate of change of electric flux (**D**) and the surface integral of current flux (**J**) equals the wire's current (call it I). so:

$$H.2\pi r = I$$

$$B = \frac{\mu I}{2\pi r} = \frac{4\pi \times 10^{-7}}{2\pi \times 0.02} = 10\mu T$$

The direction of B flux is parellel to the fingertips of a right hand whose thumb points in the direction of current:



The question was attempted by 285 (96%) of candidates and the average mark was 7.9/10. Most candidates answered with little difficulty.

12.

The spring will eventually contract because the currents through the coils are parallel and parallel steady-state currents attract. This can be shown by finding the direction of the B flux as in question 11, then using the equation that $\mathbf{F} = -e\mathbf{v} \times \mathbf{B}$ (or else the motor rule).

[Some candidates noticed that the spring will initially extend because all systems adjust to exclude changing flux. This can be shown by noting that the magnetic field through the centre of the spring is inversely proportional to length ($B = \mu NI/L$) and that $\oint_c \mathbf{E.dl} = -\int_s \dot{\mathbf{B}}.\mathbf{dS}$. In the brief moment after switch on, the changing magnetic field causes a large electric field whose energy is minimized if the spring extends.]

The question was attempted by 279 (94%) of candidates and the average mark was 6.6/10. This was not an ideal short question because there is the potential to answer in more depth than required. A good fraction of candidates noted that it is equivalent to analyzing the current through parallel wires and deduced the correct answer.

13.

(a) The electromagnetic equations tell us that **D** = εE, and **E** = ∇V. We are told here that **D** = x**i**, so:

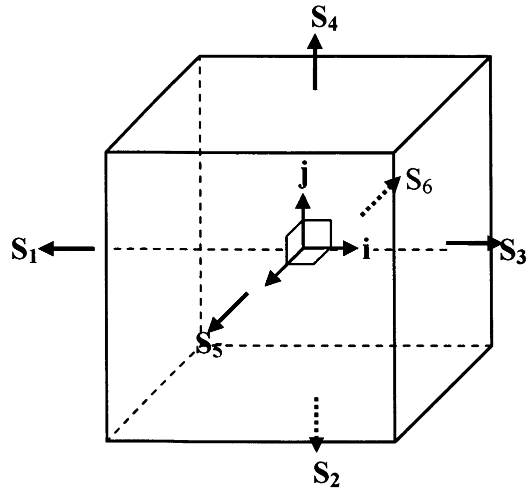
$$\nabla V = \begin{pmatrix} \partial V/\partial x \\ \partial V/\partial y \\ \partial V/\partial z \end{pmatrix} = \frac{1}{\varepsilon}\begin{pmatrix} x \\ 0 \\ 0 \end{pmatrix}$$

so $$\partial V/\partial x = x/\varepsilon$$

It follows that the voltage between the points (-½, 0, 0) and (½, 0, 0) is given by:

$$\begin{aligned} V &= \int_{x=-1/2}^{x=1/2} \frac{x}{\varepsilon} dx \\ &= \left[\frac{x^2}{2\varepsilon}\right]_{x=-1/2}^{x=1/2} \\ &= 0 \end{aligned}$$

(b) The electromagnetic equations tell us that the charge enclosed by a surface, S, is given by $Q = \int_S \mathbf{D.dA}$. In this case, the surface of integration is comprised of the six faces of a unit cube and the vector areas $\mathbf{S_1}$, $\mathbf{S_2}$, $\mathbf{S_3}$, $\mathbf{S_4}$, $\mathbf{S_5}$ and $\mathbf{S_6}$ of the faces have in each case a magnitude of 1^2 and are perpendicular to the face pointing outwards.



Now $\mathbf{D.S_4} = \mathbf{D.S_2} = \mathbf{D.S_5} = \mathbf{D.S_6} = 0$, so:

$$\int_S \mathbf{D.dA} = (\mathbf{D} \text{ at } x=-½).\mathbf{S_1} + (\mathbf{D} \text{ at } x=½).\mathbf{S_3}$$

$$= \begin{pmatrix} -\frac{1}{2} \\ 0 \\ 0 \end{pmatrix} \cdot \begin{pmatrix} -1 \\ 0 \\ 0 \end{pmatrix} + \begin{pmatrix} \frac{1}{2} \\ 0 \\ 0 \end{pmatrix} \cdot \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix}$$

$$= 1 \text{ Coulomb}$$

(c) The electromagnetic equations tell us that the energy per unit volume stored in a uniform electric field equals ½E^2. In this case the electric field varies with x, so we must integrate it:

$$\text{Energy stored in cube} = \iiint_V \frac{1}{2\varepsilon} E^2 dV$$

$$= \frac{1}{2\varepsilon} \int_{z=-\frac{1}{2}}^{z=\frac{1}{2}} \int_{y=-\frac{1}{2}}^{y=\frac{1}{2}} \int_{x=-\frac{1}{2}}^{x=\frac{1}{2}} x^2 dx dy dz$$

$$= \frac{1}{2\varepsilon} \int_{x=-\frac{1}{2}}^{x=\frac{1}{2}} x^2 dx$$

$$= \frac{1}{6\varepsilon} \left[x^3 \right]_{x=-\frac{1}{2}}^{x=\frac{1}{2}}$$

$$= \frac{1}{24\varepsilon} \text{ Joules}$$

Examiner's comments: Question was attempted by 102 (34%) of candidates and average mark was 14.4/30. It was unpopular perhaps because the question is not amenable to the laws taught in A level physics but solution using the electromagnetic equations is fairly straightforward. Section (a) was answered well but sections (b) and (c) gave more trouble, particularly the concepts of summing the dot products of D with vector area, and of integrating energy per unit volume throughout the cube.