

2009 PART 1A P3
Electrical and Information Engineering

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1 (short)

(a) What are the parameters that describe an ideal operational amplifier, and under what circumstances may real amplifiers be regarded as ideal

Output Resistance R_o

Input Resistance R_{in}

Gain A

In the ideal case: $R_o=0$; $R_{in}=\infty$; $A=\infty$

(b) The operational amplifier in Fig. 1 is ideal, except that it has a gain $A=100$. Calculate the input impedance and the gain of the circuit, V_o/V_i

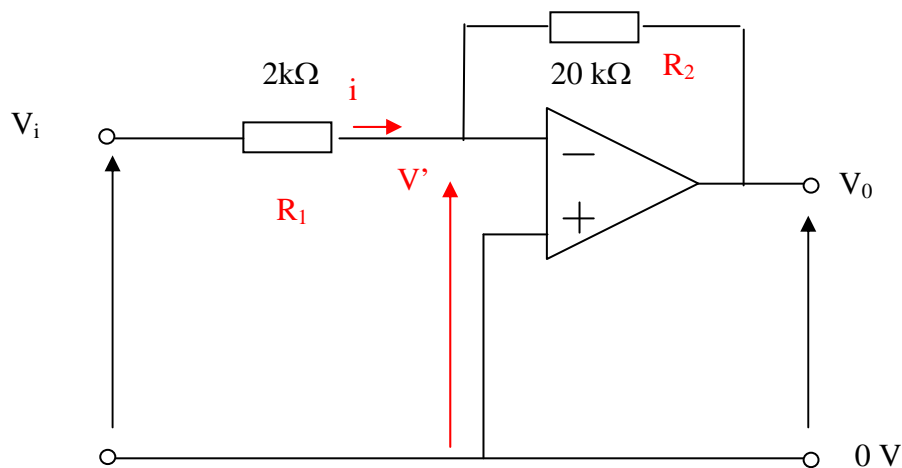


Fig. 1

Calling $R_1=2k\Omega$ and $R_2=20k\Omega$, we have

$$i = \frac{V' - V_0}{R_2} = \frac{V'(1+A)}{R_2}$$

$$V' = \frac{iR_2}{1+A}$$

But

$$V_i = R_{in}i = R_1i + V'$$

Thus

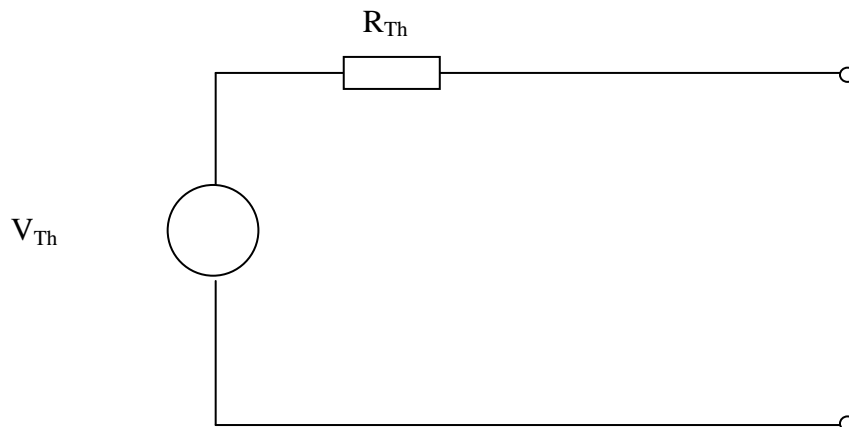
$$R_{in} = R_1 + \frac{R_2}{1+A} = 2198\Omega$$

$$V_0 = -AV' = -\frac{iAR_2}{1+A}$$

$$G = \frac{V_0}{V_i} = -\frac{AR_2}{R_1(1+A) + R_2} = -9.01$$

2 (short) (a) State Thevenin's and Norton's Theorems

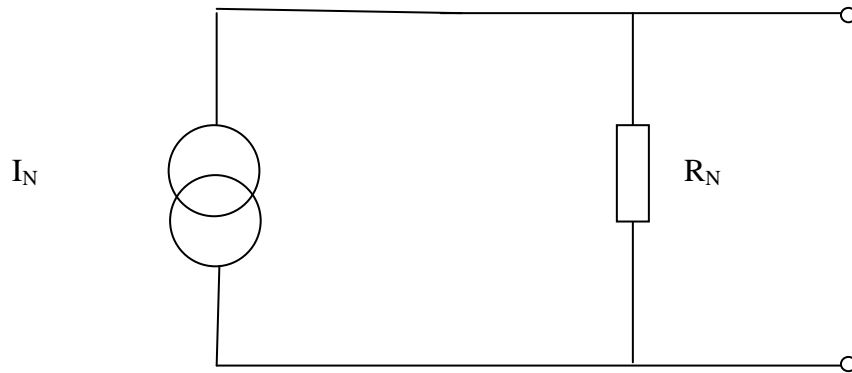
Thevenin: Any linear circuit may be represented as:



$$V_{Th} = V_{\text{Open Circuit}}$$

$$R_{Th} = V_{\text{Open Circuit}} / I_{\text{Short Circuit}}$$

Norton: Any linear circuit may be represented as:



$$I_N = I_{\text{Short Circuit}}$$
$$R_N = V_{\text{Open Circuit}} / I_{\text{Short Circuit}}$$

(b) Calculate the Thevenin and Norton equivalents of the circuit in Fig. 2

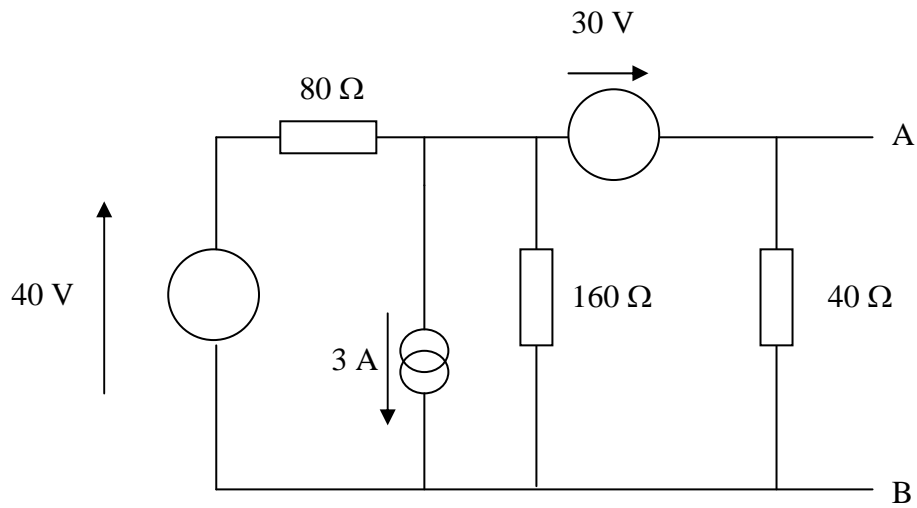
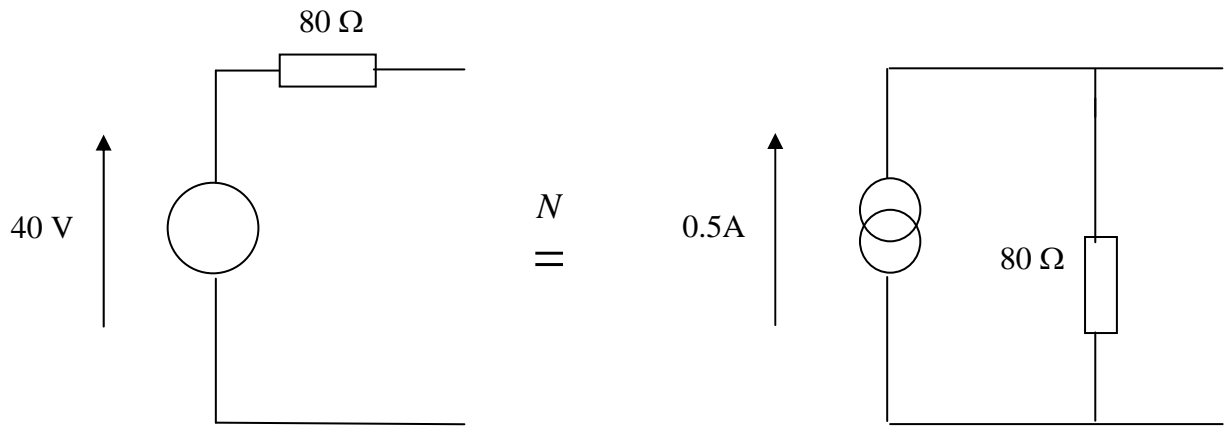
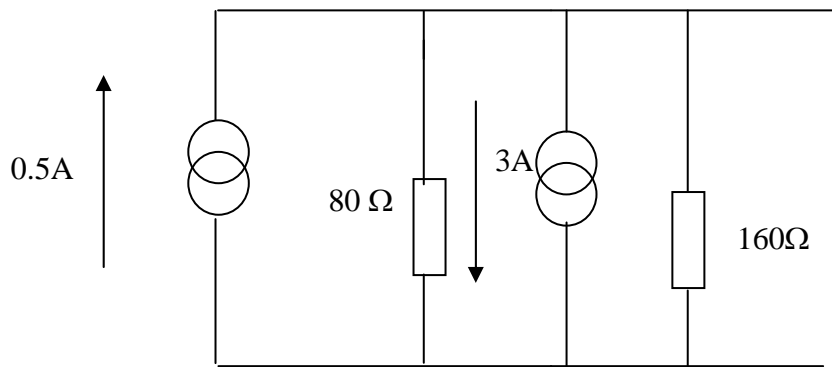


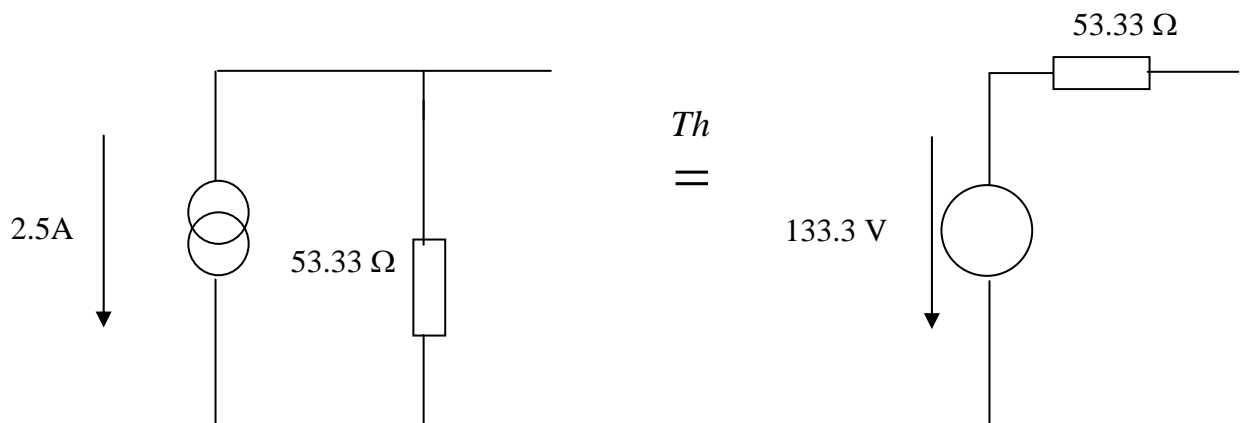
Fig.2



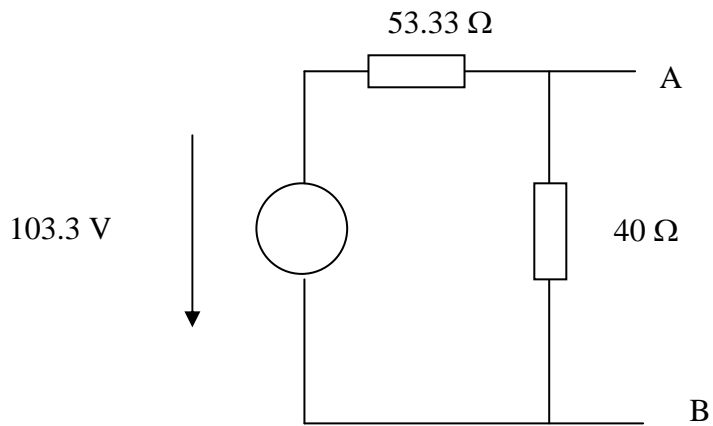
This gives



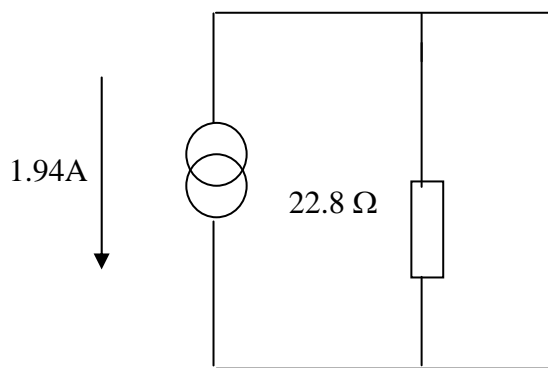
Which is equivalent to:



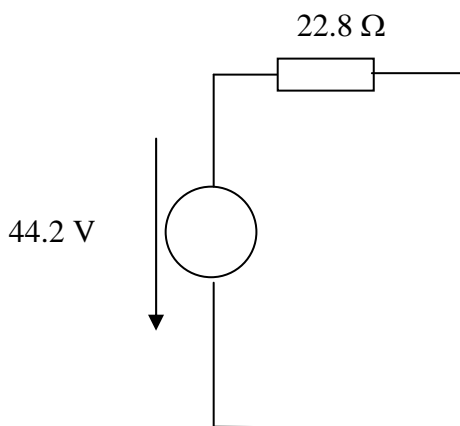
The circuit then becomes



Its Norton equivalent is then:



Its Thevenin equivalent is:



3 (**short**) The ac circuit shown in Fig. 3 is connected to a 240V, 50 Hz power supply. Determine the total complex impedance of the circuit and hence find the magnitude and phase with respect to the voltage source of the input current.

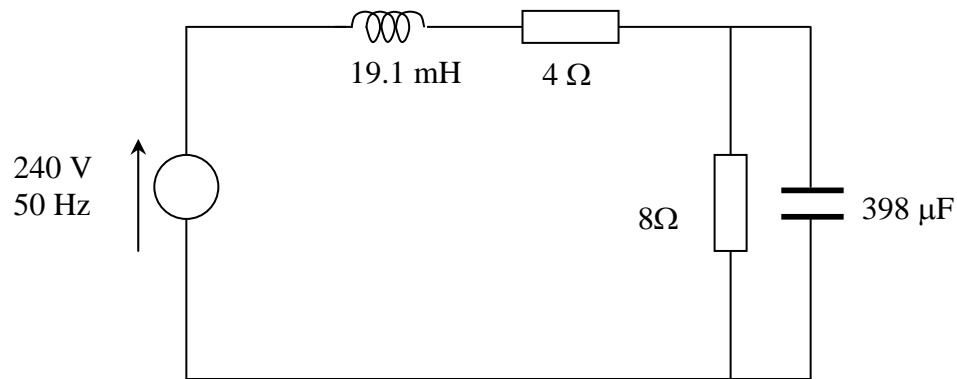


Fig. 3

The impedance of the inductor is

$$\overline{Z}_L = j\omega L = j2\pi fL = j6\Omega$$

The impedance of the capacitor is

$$\overline{Z}_C = \frac{1}{j\omega C} = -j8\Omega$$

Combining the 8Ω resistor in parallel with the capacitor gives

$$\overline{Z} = (4 - j4)\Omega$$

Therefore the total impedance is

$$\overline{Z}_T = j6\Omega + 4\Omega + 4\Omega - j4\Omega = (8 + j2)\Omega$$

From Ohm's Law we have

$$\bar{I} = \frac{\bar{V}}{Z_T} = 29.1 \angle -14^\circ \text{ A}$$

4 (long) The circuit of an ac amplifier is shown in Fig. 4

(a) Calculate the values of R_1 and R_2 required to set the transistor operating point, where $V_{DS}=13 \text{ V}$, $I_D=0.3 \text{ mA}$, and $V_{GS}=-3 \text{ V}$. You may assume that the transistor is ideal and that no current flows.

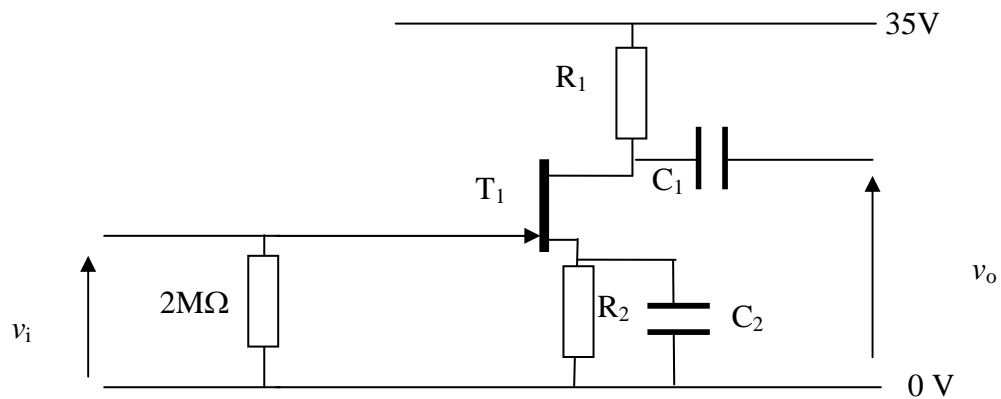
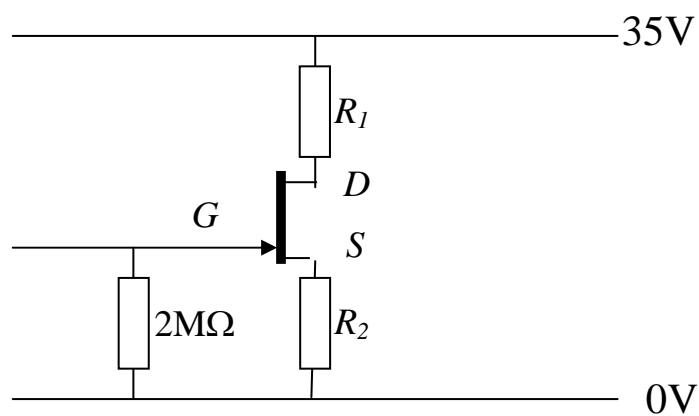


Fig. 4

The DC equivalent circuit is:



$$V_G=0 \Rightarrow V_S=3V$$

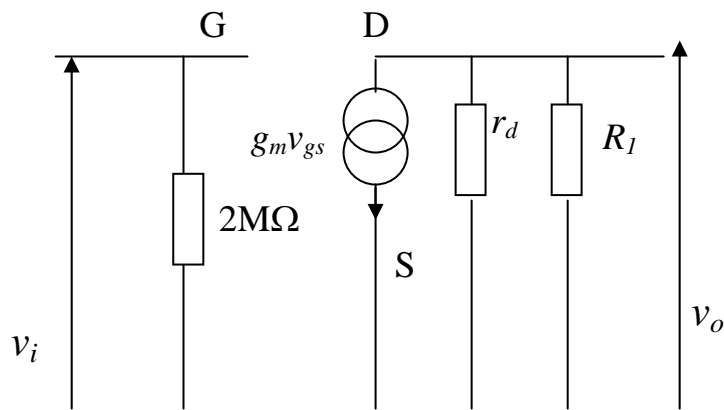
$$R_2 = \frac{V_S}{I_D} = 10k\Omega$$

Voltage across R_1 is $35V-13V-3V=19V$

Since $I_D=0.3mA$

$$R_1 = \frac{19V}{0.3mA} = 63.3k\Omega$$

(b) Draw the small signal model for the circuit, assuming that the impedances of the capacitors are negligible at small signal frequencies.



(c) Derive approximate expressions for the small signal gain, v_o/v_i , and the output impedances for the circuit, assuming that the output circuit draws no current. Hence evaluate these expressions with the values of the resistors calculated in (a). For the FET small signal parameters take $g_m=1mS$ and $r_d= 200k\Omega$

$$V_i = V_{gs}$$

Sum of current at drain node:

$$g_m v_{gs} + \frac{v_o}{\frac{R_1 r_d}{R_1 + r_d}} + i_o = 0$$

Then:

$$v_o = (-g_m v_{gs} - i_o) \frac{R_1 r_d}{R_1 + r_d}$$

But

$$v_o = \text{Gain} \times v_{gs} - R_{out} \times i_o$$

Thus

$$\text{Gain} = \frac{-g_m R_1 r_d}{R_1 + r_d} = 48.1$$

$$R_{out} = \frac{R_1 r_d}{R_1 + r_d} = 41.8k\Omega$$

(d) What value of C_1 is required if the circuit is to have a -3dB ($1/\sqrt{2}$) low frequency cut-off of 15Hz , with a $10k\Omega$ load connected to the output, and assuming the source to be grounded (i.e. assuming the impedance of C_2 to be negligible) ?

$$v_0 = \text{Gain} \times v_i \frac{R_{Load}}{R_{Load} + R_{out} + \frac{1}{j\omega C_1}}$$

This drops to -3dB, or $1/\sqrt{2}$ of mid-band value when the real and imaginary part of the denominator are equal

$$R_{Load} + R_{out} = \frac{1}{\omega C_1}$$

Then

$$C_1 = 182.6 \text{ nF}$$

5 (**long**) An extraction fan driven by an ac motor is powered from the mains via a long length of cable. The motor, cable and mains supply are represented by the equivalent circuit shown in Fig. 5

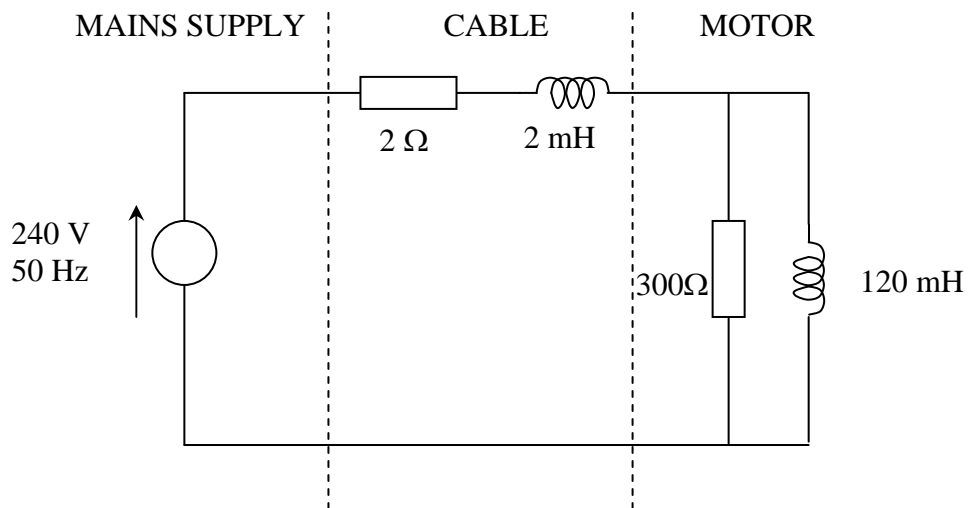


Fig. 5

(a) Explain the significance of Watts and VARs

Watts= $VI\cos\Phi$ produce useful work, heat, light, etc.

VARs= $VI\sin\Phi$ represent energy stored and released in capacitors and inductors during the ac cycle and produce no useful work

(b) Calculate the current drawn from the supply and the power factor

In the Cable

$$j\omega L_C = j0.002 \times 100\pi = j0.628\Omega$$

Thus

$$\overline{Z}_C = (2 + j0.628)\Omega = R_C + X_C$$

In the Motor

$$j\omega L_m = j0.12 \times 100\pi = j37.7\Omega$$

$$\overline{Z}_m = \frac{300 \times j37.7}{300 + j37.7} \Omega = (4.66 + 37.1j)\Omega = R_m + X_m$$

Then

$$\overline{I} = \frac{\overline{V}}{\overline{Z}_m + \overline{Z}_C} = \frac{240}{2 + 4.66 + j(37.1 + 0.628)} A = 6.26 \angle -80^\circ$$

Power factor

$$\cos\Phi = 0.178 \text{ lag}$$

(c) How many Watts and VARs are drawn by the motor and what is the power loss in the cable

$$\text{Motor Power} = I^2 R_m = 182.6 \text{ W}$$

$$\text{Motor VARs} = I^2 X_m = 1454 \text{ VARs}$$

$$\text{Cable power loss} = I^2 R_C = 78.4 \text{ W}$$

(d) A capacitor is connected across the motor to correct its power factor to unity. Calculate the required value of this capacitance

To correct the power factor to unity we need to shunt the motor with a capacitor producing equal but opposite VARs to the motor inductance

Calling V_m the voltage across the motor

$$\text{Motor VARs} = 1454 = \frac{V_m^2}{37.7}$$

$$\text{Capacitor VARs} = -\frac{V_m^2}{\frac{1}{\omega C}} = -\omega C V_m^2$$

Thus

$$C = \frac{1}{100\pi 37.7} \text{ F} = 84.4 \mu\text{F}$$

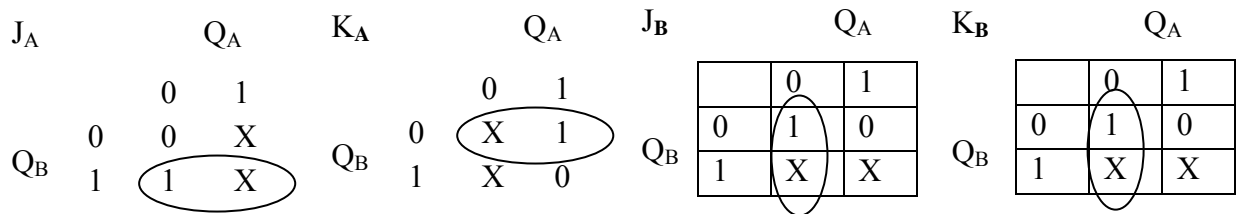
SECTION B

6 (a) 4 states so $2^m = 4$ where m is the number of bistables so $m = 2$.

(b)

Present state		Next state					
Q_A	Q_B	Q_A	Q_B	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	1	1	X	X	0
1	1	1	0	X	0	X	1
1	0	0	0	X	1	0	X

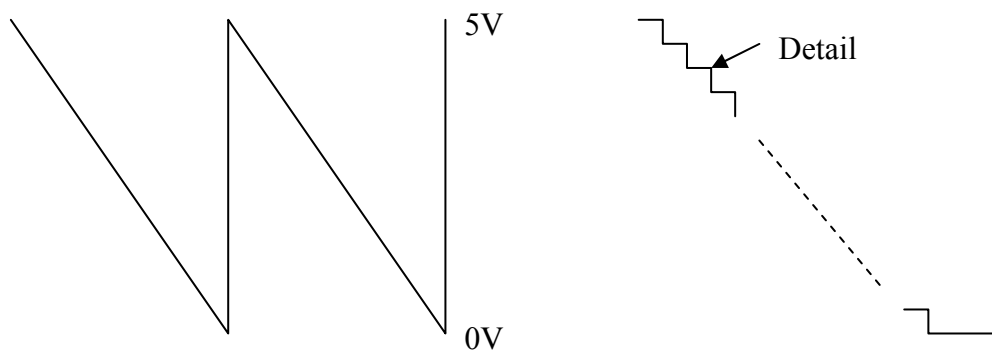
(c)



From Karnaugh maps $J_A = Q_B$ $K_A = \overline{Q_B}$ $J_B = \overline{Q_A}$ $K_B = Q_A$

7 (a) Memory-mapped I/O refers to the designation of an I/O port by a memory address. Reading/writing to this memory address results in data being read from/written to the corresponding I/O port.

(b) The code loads accumulator A with \$FFH and then enters a loop in which the contents of A is sent to the DAC, A is decremented and the process repeated until A becomes \$00H. At this point A is reinitialized to \$FFH. Thus, the output of the DAC ramps down from 5V to 0V in 255 steps, and then jumps back up to 5V. This results in the sawtooth waveform sketched below.



The first and last instructions of the code are executed once per cycle of the output waveform, the intervening three instructions are executed 255 times. Assigning clock cycles as shown below results in a total number of clock cycles per period of $N = 1 \times (2+4) + 255 \times (11) = 2811$.

With a clock frequency of 8 MHz this gives a period of $2811/8 \mu\text{s} = 351.4 \mu\text{s}$.

		Clock cycles
start:	LDAA #\$81	2
loop:	DECA	2
	STAA \$E000	5
	BNE loop	4
	JMP start	4

It is assumed that the JMP instruction uses the extended mode of addressing.

8 (a) Current flowing in left-most $2R$ resistor is $V_{ref}/2R$, and this is the current flowing towards switch S_7 . Resistance 'seen' to the right is also $2R$, so current flowing in left-most R resistor is also $V_{ref}/2R$. Current in this resistor splits equally at the next node because the resistance is $2R$ either way. So current flowing towards switch S_6 is $V_{ref}/4R$. Similarly, current flowing towards switch S_5 is $V_{ref}/8R$, S_4 is $V_{ref}/16R$ etc. These currents are therefore weighted according to the weights of the columns in the binary number system. If a switch is in position '1' then the current contributes towards the total current flowing towards the inverting input of the op-amp, I_T . If a switch is in position '0' then the corresponding current does not contribute. Therefore I_T is proportional to the binary number represented by switches $S_7 \dots S_0$. Since the output voltage $V_0 = -I_T R'$ assuming ideal op-amp characteristics then V_0 is also proportional to the to the binary number represented by switches $S_7 \dots S_0$.

$$(b) \quad I = \frac{V_{ref}}{8R} + \frac{V_{ref}}{32R} + \frac{V_{ref}}{64R} + \frac{V_{ref}}{256R} = \frac{V_{ref}}{R} \left[\frac{1}{8} + \frac{1}{32} + \frac{1}{64} + \frac{1}{256} \right] = \frac{0.1758V_{ref}}{R}$$

$$V_0 = -IR' = -(-5) \times \frac{5000}{5000} \times 0.1758 = 0.8789 V$$

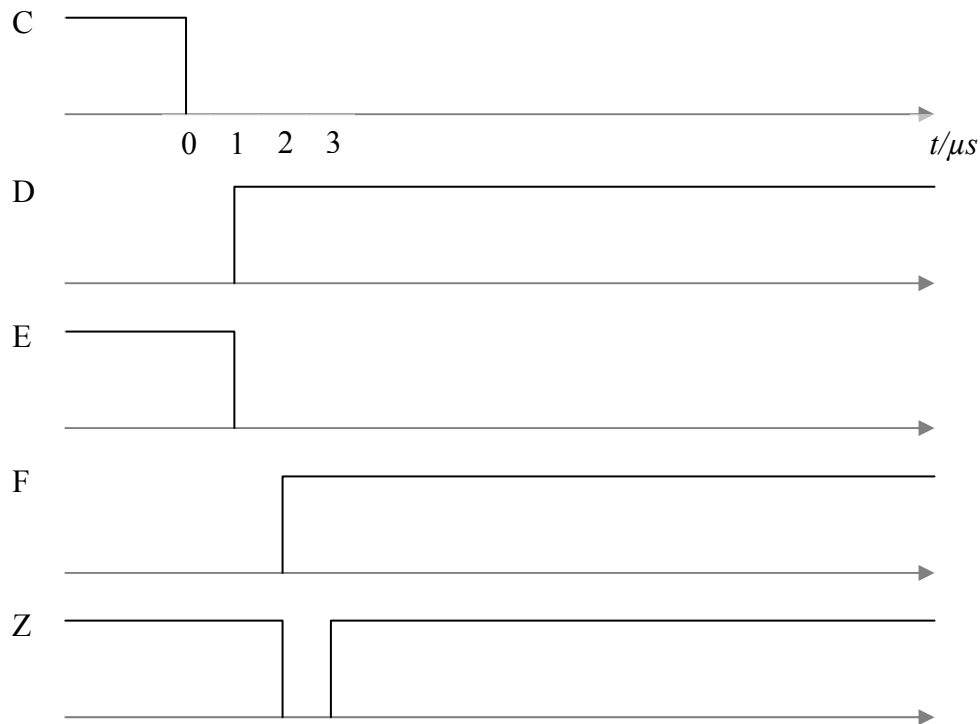
(c) Either do a similar calculation to that of part (b) or use scaling. Here we use scaling. In (b) binary number is 90_{10} , FF is 255_{10} and so output will be:

$$V_0 = \frac{255}{90} \times 0.8789 = 2.49 V$$

9 (a) (i) By inspection of the circuit $Z = A.C + B.C$

(ii) Substituting in $A = B = 1$ into above expression gives $Z = 1.C + 1.\bar{C} = C + \bar{C} = 1$. Thus $Z = 1$ independent of C .

(iii)



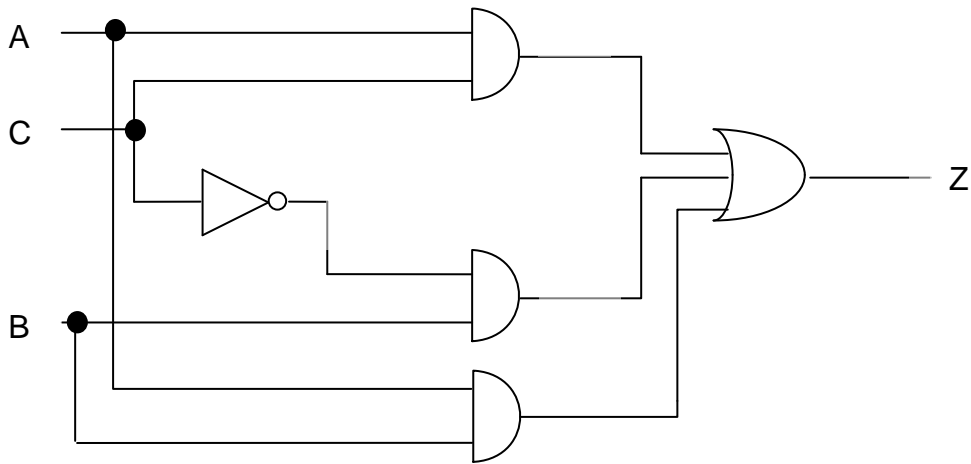
The timing diagrams show that Z goes to zero between $t = 2\mu s$ and $3 \mu s$ whereas it should always be 1. There is therefore a static 1 hazard.

(iv) To remove static hazard an additional term is needed to 'cover' the adjacent but non-overlapping groups, shown dotted in the Karnaugh map below. The new group is $A.B$.

	AB			
C	00	01	11	10
0	0	1	1	0
1	0	0	1	1

The Karnaugh map shows two groups of 1s circled with solid lines: a horizontal group covering cells (0,01) and (0,11), and a vertical group covering cells (0,11) and (1,11). A third group, consisting of the two cells (1,01) and (1,11), is circled with a dashed line.

$$Z = A.C + B.\bar{C} + A.B$$



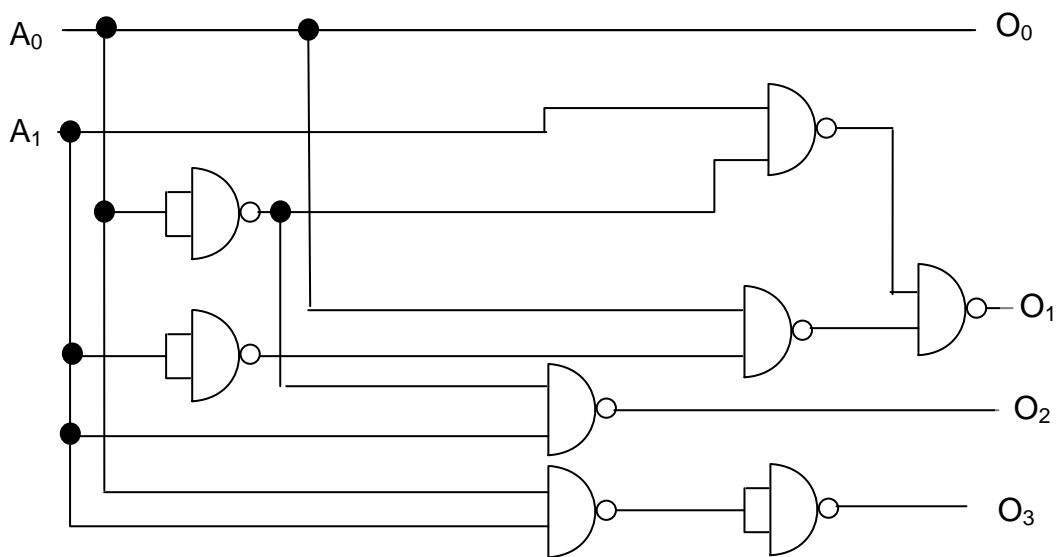
(b) The table below shows the relationship between the 4 outputs and the 2 inputs.

A_1	A_0	O_3	O_2	O_1	O_0
0	0	0	0	0	0
0	1	0	0	1	1
1	0	0	1	1	0
1	1	1	0	0	1

By inspection $O_0 = A_0$, $O_1 = A_1 \oplus A_0$, $O_2 = A_1 \cdot \overline{A_0}$, $O_3 = A_1 \cdot A_0$

$O_3 = \overline{\overline{A_1 \cdot A_0}}$ $O_2 = \overline{A_1 \cdot \overline{A_0}}$ $O_1 = A_1 \cdot \overline{A_0} + \overline{A_1} \cdot A_0$ Applying De Morgan's theorem: $\overline{O_1} = \overline{A_1 \cdot \overline{A_0} + \overline{A_1} \cdot A_0}$ and so $O_1 = \overline{A_1 \cdot \overline{A_0} \cdot \overline{A_1} \cdot A_0}$

The resulting circuit is shown below.



SECTION C

10 (a) Gauss' Law: $\oiint_S \mathbf{D} \cdot d\mathbf{S} = Q$

(b) Charges are confined to surface of both conductors, thus $D = E = 0$ for $r < 1$ mm and $r > 3$ mm.

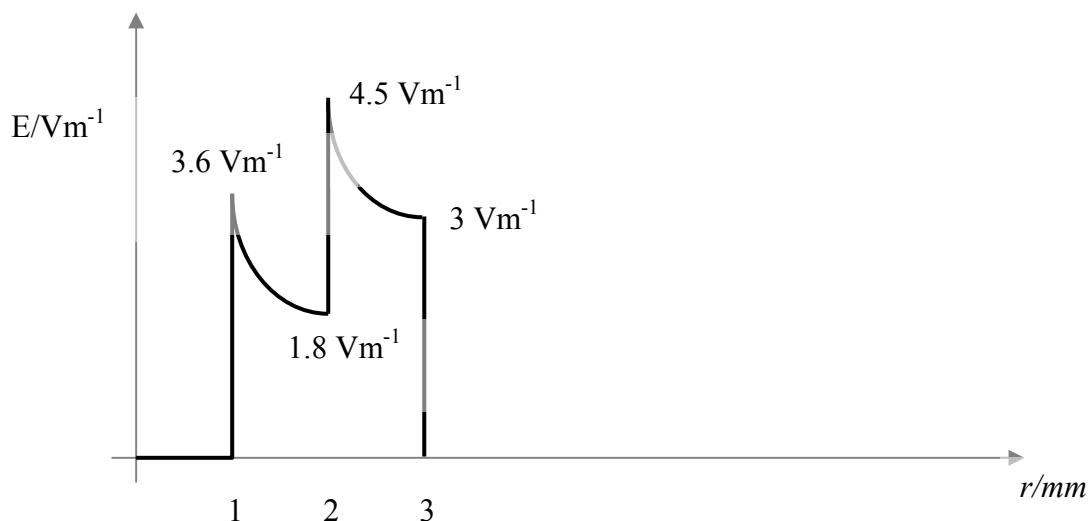
$D \times 2\pi r = \rho$ so $D = \rho/2\pi r$ and using $D = \epsilon_0 \epsilon_r E$ gives $E = \rho/2\pi \epsilon_0 \epsilon_r r$

Substituting in the numbers gives, in the material of relative permittivity 5:

$E(1 \text{ mm}) = 3.6 \text{ Vm}^{-1}$ $E(2 \text{ mm}) = 1.8 \text{ Vm}^{-1}$

In the material of relative permittivity 2:

$E(2 \text{ mm}) = 4.5 \text{ Vm}^{-1}$ $E(3 \text{ mm}) = 3 \text{ Vm}^{-1}$

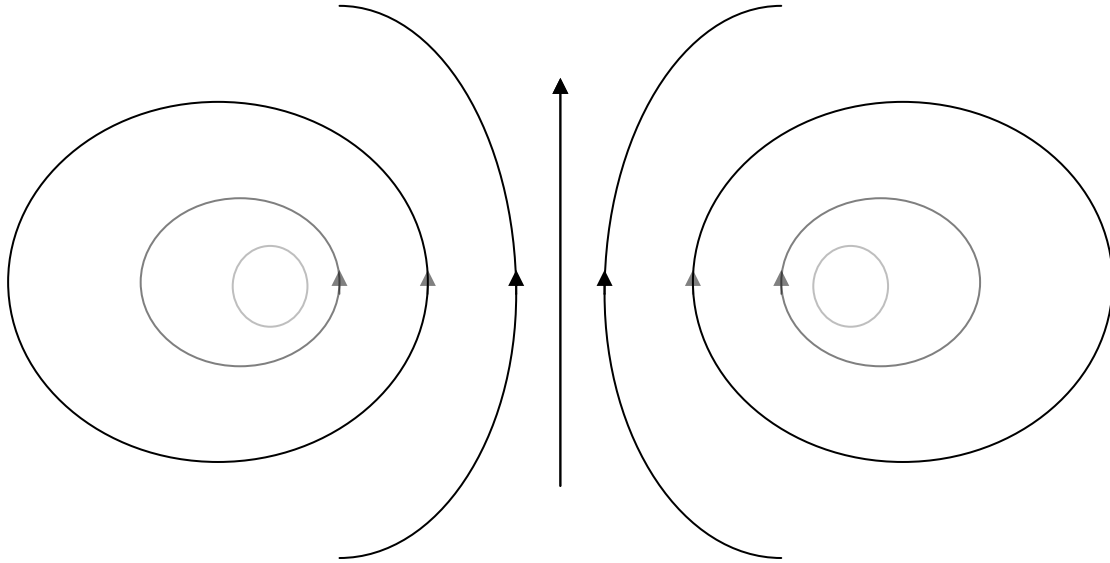


(c) Find the voltage between inner and outer conductors by integrating the electric field from $r = 1$ mm to $r = 3$ mm, noting that the integration has to be broken down into two intervals:

$$V = \int_{1\text{mm}}^{2\text{mm}} \frac{\rho}{2\pi\epsilon_0\epsilon_{r1}r} dr + \int_{2\text{mm}}^{3\text{mm}} \frac{\rho}{2\pi\epsilon_0\epsilon_{r2}r} dr = \frac{\rho}{2\pi\epsilon_0} \left[\frac{1}{\epsilon_{r1}} \ln 2 + \frac{1}{\epsilon_{r2}} \ln 1.5 \right] = 6.15 \text{ mV}$$

$$C_l = \frac{\rho}{V} = \frac{10^{-12}}{0.00615} = 0.163 \text{ nFm}^{-1}$$

11 (a) Ampere's Law: $\oint_C \mathbf{H} \cdot d\mathbf{l} = I$



(b) $H \times 2\pi r = I$ so $H = I/2\pi r$ and $B = \mu_0 H = \mu_0 I/2\pi r$

in which r is the distance from the centre of the conductor. Using superposition and expressing r in terms of x gives

$$B = \frac{\mu_0 I}{2\pi} \left[\frac{1}{a-x} + \frac{1}{a+x} \right]$$

$$(c) \varphi = \varphi' = 2 \int_0^{a-b} B dx = \frac{\mu_0 I}{\pi} \int_0^{a-b} \left[\frac{1}{a-x} + \frac{1}{a+x} \right] dx = \left[\frac{\mu_0 I}{\pi} \ln \left(\frac{a+x}{a-x} \right) \right]_0^{a-b} = \frac{\mu_0 I}{\pi} \ln \frac{2a-b}{b}$$

$$L = \frac{\varphi'}{I} = \frac{\mu_0}{\pi} \ln \frac{2a-b}{b} \approx \frac{\mu_0}{\pi} \ln \frac{2a}{b}$$

assuming that $a \gg b$. This ignores partial flux linkages ie flux lines which cut the conductors themselves and therefore only link part of the current.

12 (a) Consider a length l of conductor of fixed cross section A and resistivity ρ . Then

$$V = El, \quad J = I/A \text{ and } E = \rho J = \rho I/A. \text{ Combining: } V = \rho l I/A \text{ and so } V/I = R = \rho l/A$$

Every turn is $4 \times 35 = 140$ mm long and there are 200 turns so $l = 28$ m.

$A = \pi r^2$ with $r = 0.25$ mm giving $A = 1.96 \times 10^{-7}$ m². Resistivity $\rho = 1.72 \times 10^{-8}$ Ω m. Putting in the numbers gives $R = 2.45$ Ω .

(b) Amperes law: $H \times l = NI = 200I$ so $H = 200I/0.56$ and $B = \mu_0 \mu_r H$

$$\text{so } B = 4\pi \times 10^{-7} \times 1000 \times 200I/0.56 = 0.449I.$$

$$\phi' = N \phi = 200 \times 0.449I \times A \text{ where } A \text{ is the core cross-sectional area} = 0.035^2 = 1.225 \times 10^{-3}$$

$$\text{giving } \phi' = 1.1I \text{ and so } L = \phi'/I = 0.11 \text{ H}$$

$$(c) \text{ Impedance} = R + j\omega L = 2.45 + j2\pi \times 50 \times 0.11 = (2.45 + j34.6)\Omega$$

$$I = V/Z = 100/34.6 = 2.89 \text{ A rms.}$$

(d) Peak flux density is 1.8 T, at this value using B-H curve from data book $H = 500$ Am⁻¹.

At half of this value ie 0.9 T $H = 25$ Am⁻¹. Applying Amperes Law gives $Hl = NI$ and so $I = Hl/N$.

When $B = 1.8$ T this gives $I = 1.4$ A.

When $B = 0.9$ T this gives $I = 0.07$ A.

These answers show that the inductor is highly non-linear when driven to a peak flux density of 1.8 T. In theory, doubling the flux density should double the current, but here it is seen that the current increases by a factor of 20. This would lead to a very 'peaky' input current which is much larger than the predicted input current owing to the iron core being driven into saturation.