ENGINEERING TRIPOS PART IA

Monday 8 June 2009 9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

*Answer **all** questions.*

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

Answers to questions in each section should be tied together and handed in separately.

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

SECTION A

1 **(short)**

(a) What are the parameters that describe an ideal operational amplifier, and under what circumstances may real amplifiers be regarded as ideal? [3]

(b) The operational amplifier shown in Fig. 1 is ideal, except that it has a gain A = 100. Calculate the input impedance and the gain of the circuit, V_o/V_i. [7]

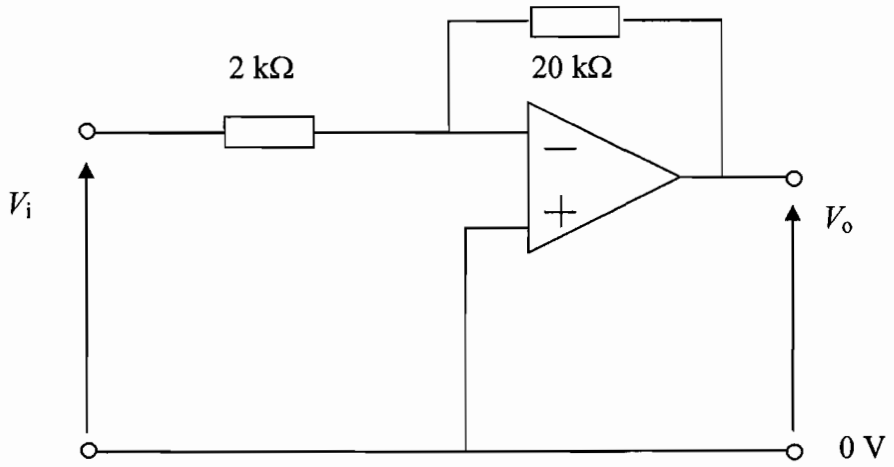


Fig. 1

2 **(short)**

(a) State Thevenin's and Norton's theorems. [3]

(b) Calculate the Thevenin and Norton equivalents of the circuit in Fig. 2. [7]

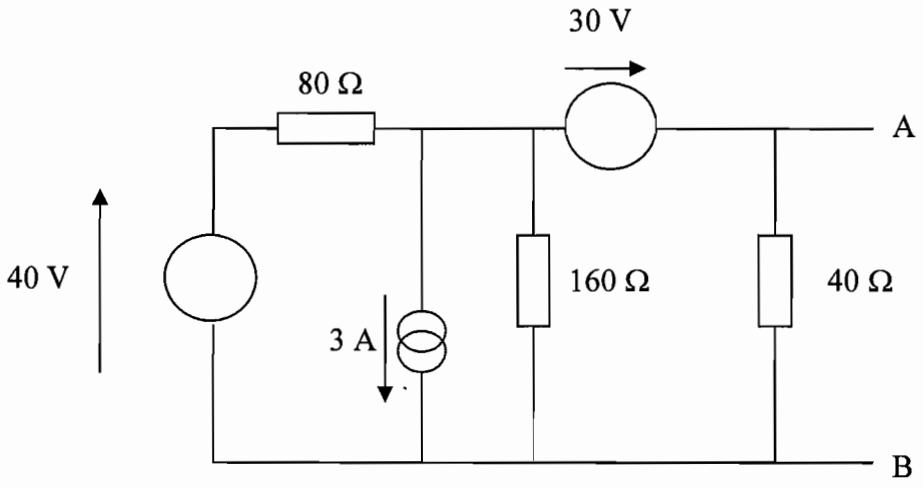


Fig. 2

3 **(short)** The ac circuit shown in Fig. 3 is connected to a 240 V, 50 Hz power supply. Determine the total complex impedance of the circuit and hence find the magnitude and phase with respect to the voltage source of the input current. [10]

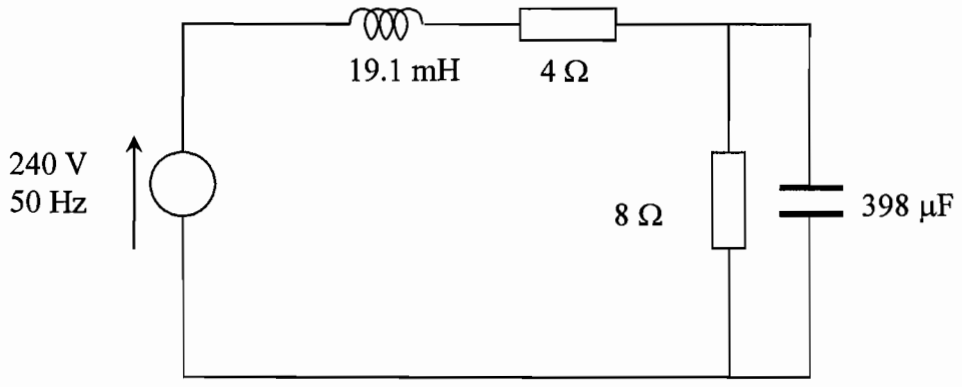


Fig. 3

4 **(long)** The circuit of an ac amplifier is shown in Fig. 4.

(a) Calculate the values of R_1 and R_2 required to set the transistor operating point, where $V_{DS} = 13$ V, $I_D = 0.3$ mA, and $V_{GS} = -3$V. You may assume that the transistor is ideal and that no gate current flows. [10]

(b) Draw the small-signal model for the circuit, assuming that the impedances of the capacitors are negligible at small-signal frequencies. [5]

(c) Derive approximate expressions for the small-signal gain, v_o/v_i, and the output impedance for the circuit, assuming that the output circuit draws no current. Hence evaluate these expressions with the values of the resistors calculated in (a). For the FET small-signal parameters take $g_m = 1$ mS and $r_d = 200$ kΩ. [10]

(d) What value of C_1 is required if the circuit is to have a –3dB ($1/\sqrt{2}$) low frequency cut-off of 15Hz, with a 10 kΩ load connected to the output, and assuming the source to be grounded (i.e. assuming the impedance of C_2 to be negligible)? [5]

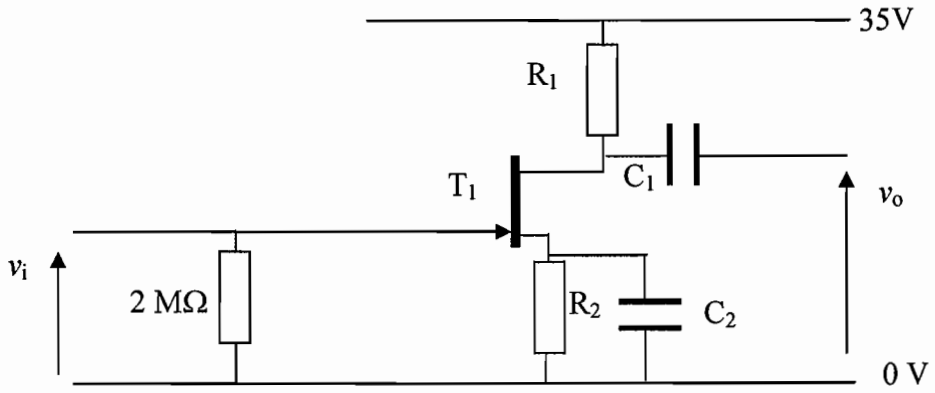


Fig. 4

5 **(long)** An extraction fan driven by an ac motor is powered from the mains via a long length of cable. The motor, cable and mains supply are represented by the equivalent circuit shown in Fig. 5.

(a) Explain the significance of Watts and VARs. [5]

(b) Calculate the current drawn from the supply and the power factor. [10]

(c) How many Watts and VARs are drawn by the motor and what is the power loss in the cable? [5]

(d) A capacitor is connected across the motor to correct its power factor to unity. Calculate the required value of this capacitance. [10]

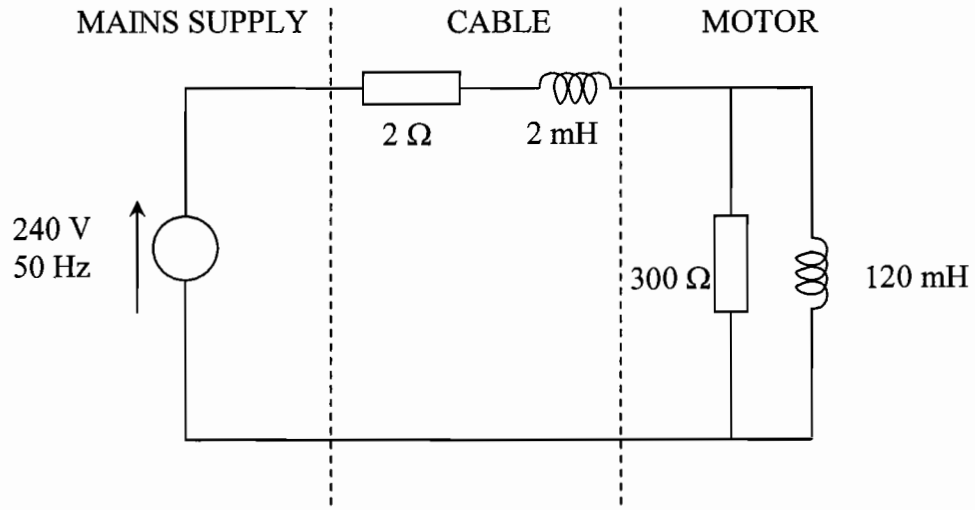


Fig. 5

SECTION B

6 **(short)** A 2-bit gray-code counter is to be designed using J-K bistables. The counter is to follow the sequence 00 - 01 - 11 - 10 indefinitely.

(a) How many bistables are required? [1]

(b) Write out the state transition table for the counter. [4]

(c) Using Karnaugh maps, or otherwise, find expressions for the J-K inputs of the bistables in terms of their outputs. [5]

7 **(short)** For the 6800 microprocessor:

(a) Explain what is meant by memory-mapped I/O. [2]

(b) Memory location $E000 corresponds to an output port to which a digital to analogue converter (DAC) is connected. When the input to the DAC is $00H its output is 0 V, when the input to the DAC is $FFH its output is 5 V. Sketch the waveform at the output of the DAC when the code below is executed, and calculate the period of the waveform assuming that the 6800 has an 8 MHz clock. State any assumptions made. [8]

```
start: LDAA #$FF
loop: STAA $E000
      DECA
      BNE loop
      JMP start
```

8 **(short)** The circuit shown in Fig. 6 is an 8-bit R-2R digital to analogue converter (DAC). The reference voltage V_{ref} is –5 V, and resistors R and R' are both 5 kΩ.

(a) Explain how the circuit operates to produce an analogue voltage at its output which is proportional to the binary number set by the switches S_0 .. S_7. [4]

(b) With switches S_6, S_4, S_3 and S_1 set to '1' and the other switches set to '0' determine the output voltage of the circuit, V_0. [4]

(c) Write down the output voltage of the circuit when all switches are set to '1'. [2]

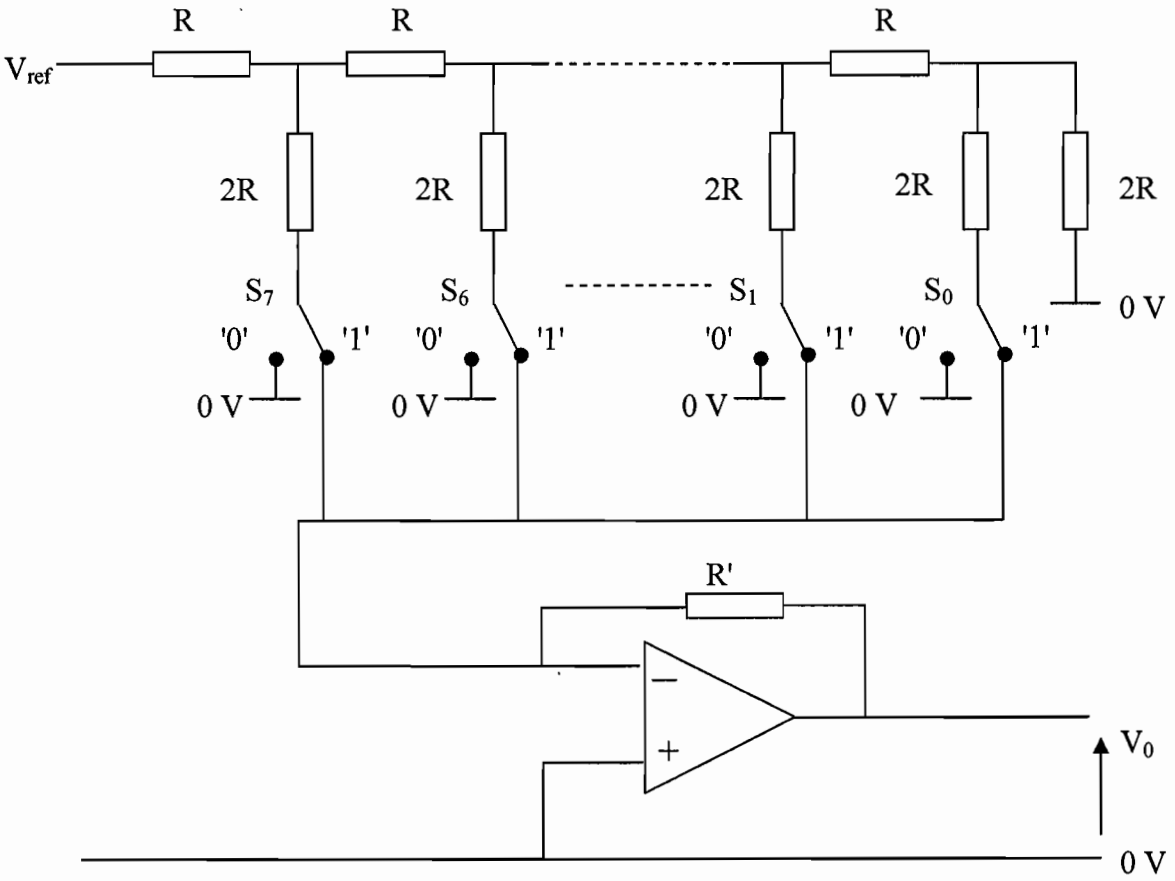


Fig. 6

9 **(long)**

(a) For the combinational logic circuit shown in Fig. 7:

(i) Write down a Boolean expression for the output Z in terms of the inputs A, B and C. [3]

(ii) In the case that inputs A and B are always set to '1' show that the output Z is independent of input C. [2]

(ii) At time t = 0 input C changes from '1' to '0'. Inputs A and B remain at '1'. All logic gates in the circuit have a propagation delay of 1μs. By drawing a set of timing diagrams showing the state of input C and the points D, E, F and Z shown in Fig. 7, show that a static hazard exists. [7]

(iv) Show how the circuit can be altered to avoid this static hazard. [3]

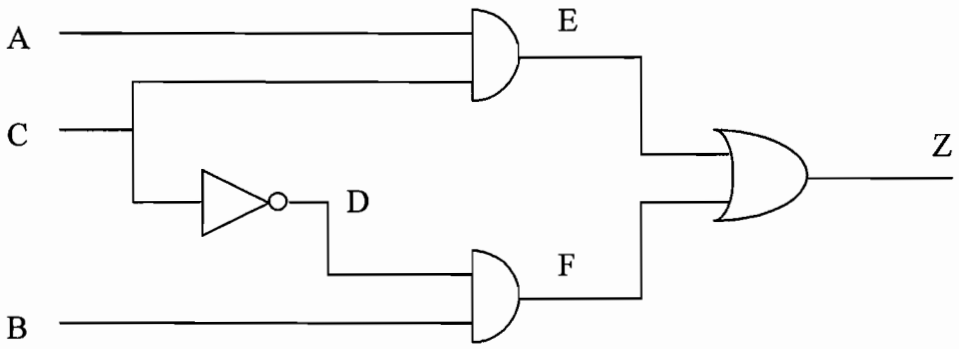


Fig. 7

(b) A combinational logic circuit is to be designed which takes a 2-bit number A_1A_0 as its input, and its output $O_3O_2O_1O_0$ is to be the 4-bit number given by multiplying the input by 3.

(i) By using Karnaugh maps, or otherwise, find Boolean expressions for each of O_3, O_2, O_1 and O_0 in terms of A_1 and A_0. [6]

(ii) Draw a circuit to implement the design which uses only 2-input NAND gates. [9]

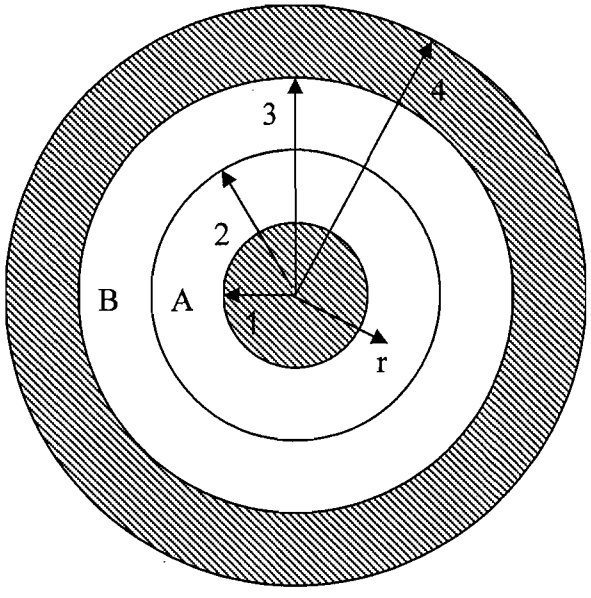
SECTION C

10 **(short)** The coaxial cable shown in Fig. 8 consists of an inner conductor of circular cross-section, radius 1 mm and an outer conductor which is an annulus concentric with the inner conductor of inner radius 3 mm, outer radius 4 mm. The gap between the inner and outer conductors is filled with two dielectric materials: annulus A has inner radius 1 mm, outer radius 2 mm and a relative permittivity of 5; annulus B has inner radius 2 mm, outer radius 3 mm and a relative permittivity of 2. The cable may be assumed to be very long, and has a charge per unit length on the inner and outer conductors of +1 pC/m and –1 pC/m respectively.

(a) State Gauss' Law. [2]

(b) Sketch a graph of the magnitude of the electric field strength vs radius r, taking $r = 0$ as the centre of the inner conductor, from $0 < r < 5$ mm. Annotate your sketch with the values of the electric field strength at $r = 1$ mm, 2 mm and 3 mm. [5]

(c) Determine the capacitance per unit length of the cable. [3]



All dimensions are in mm

Fig. 8

11 **(short)** A pair of identical very long wires of circular cross-section of radius b carry equal but opposite currents I, as shown in Fig. 9. The cables have their centres separated by the distance $2a$.

(a) State Ampere's Law and sketch the magnetic field lines. [3]

(b) Show that the magnetic flux density along the line AA' shown in Fig. 9 varies as

$$B = \frac{\mu_0 I}{2\pi}\left[\frac{1}{a-x} + \frac{1}{a+x}\right].$$ [3]

(c) Hence find the inductance per unit length of the wires, stating any assumptions made. [4]

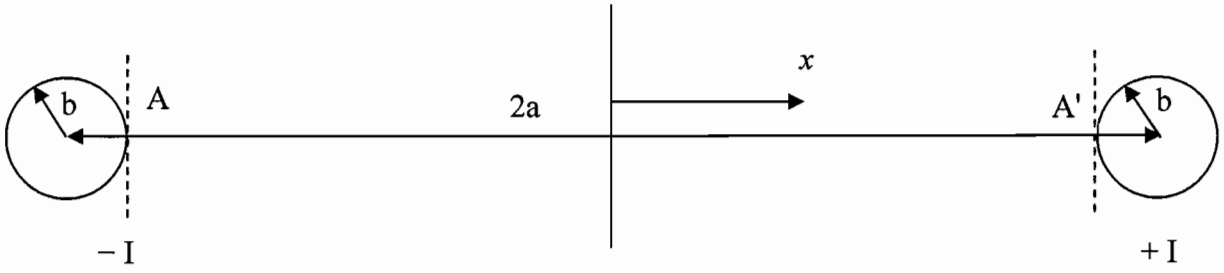


Fig. 9

12 **(long)** An inductor is formed by winding copper wire of circular cross-section around an iron core. The wire has diameter 0.5 mm and a thin layer of insulation, the thickness of which may be neglected. The coil has 200 turns and all turns are in direct contact with the iron core. The iron core has a square cross-section with side length 35 mm, and the mean path length around the iron core is 560 mm. The iron may be assumed to be lossless.

(a) Show from first principles that the resistance of the coil is given by $R = \rho l/A$ and explain what all the terms in the expression mean. Hence find the resistance of the coil, taking the resistivity of the copper to be 1.72×10^{-8} Ωm. [8]

(b) Assuming that the iron core has a fixed relative permeability of 1000, find the self-inductance of the coil. [8]

(c) Using parts (a) and (b) write down the impedance of the coil at 50 Hz. Hence find the rms coil current if the coil is supplied by a 100 V rms, 50 Hz ac voltage. [5]

(d) For part (c), the peak flux density in the core turns out to be 1.8 T. Assuming now that the iron core is made from grain orientated silicon-iron (see Engineering Data Book) determine the coil input current when the core flux density is at its peak value and at half of its peak value. Comment on your answers. [9]

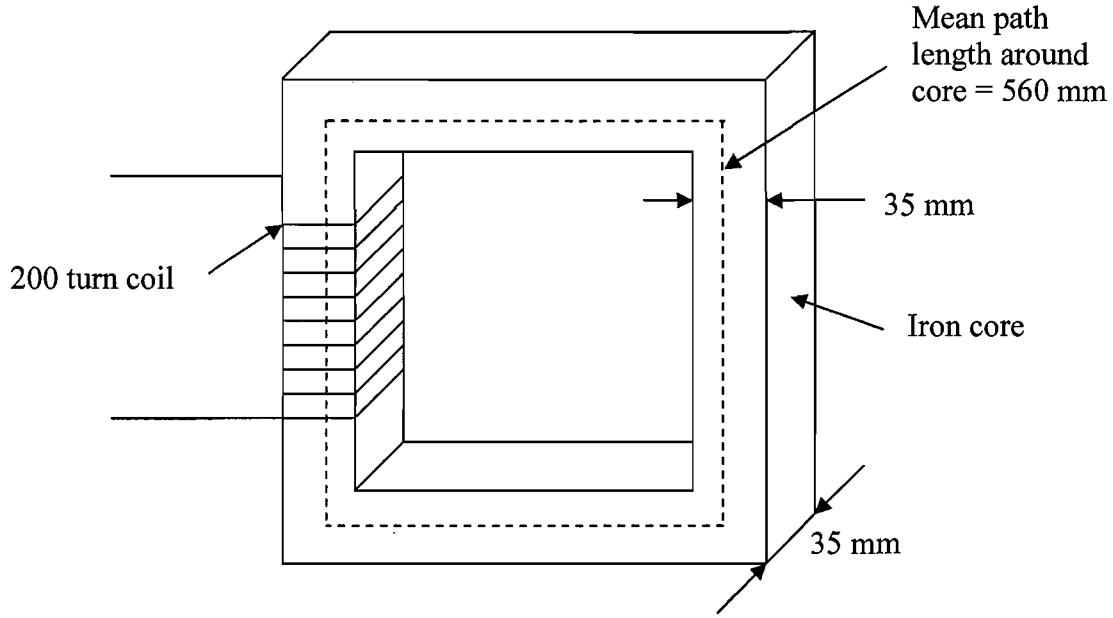


Fig. 10

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