ENGINEERING TRIPOS  PART IA

Monday 7 June 2010     9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

*Answer **all** questions.*

*The **approximate** number of marks allocated to each part of a question is indicated in the right margin.*

*Answers to questions in each section should be tied together and handed in separately.*

*There is one attachment.*

**You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator**

SECTION A

1 **(short)**

(a)    In the inverting op-amp circuit in Fig. 1, the op-amp may be assumed to be ideal. Derive an expression for the voltage gain in terms of $R_1$ and $R_2$.    [5]

(b)    If instead the op-amp has finite input resistance, $R_i$ , and finite gain $A$, but is otherwise ideal, derive an expression for the voltage gain in terms of $A$ , $R_i$, $R_1$ , $R_2$.    [3]

(c)    With  $R_i = 10$ k$\Omega$, $A = 10^3$, the op-amp of Fig. 1 is to be used to produce a voltage gain of $-20$. Using the expression for gain obtained in part (b) above, calculate $R_2$ , if $R_1 = 100$ $\Omega$.    [2]
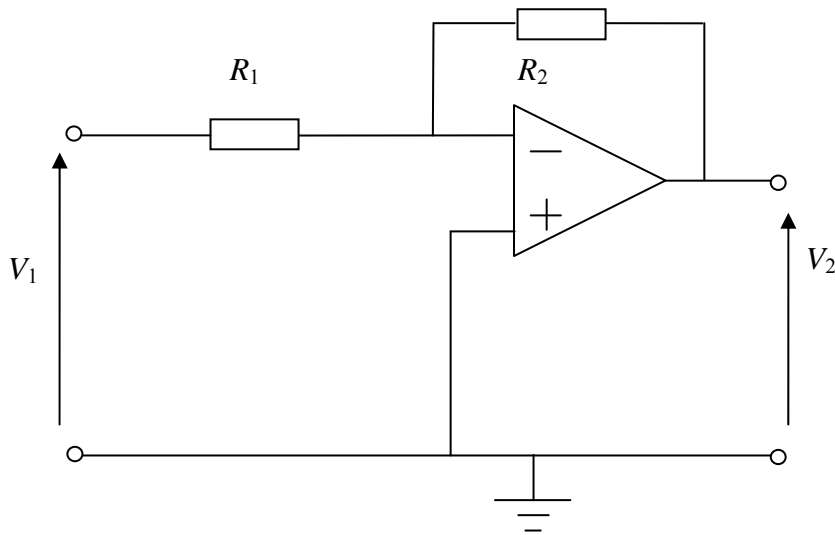


Fig. 1

2 **(short)**

(a)    In the circuit of Fig. 2, $R = 200\ \Omega$, $L = 70$ mH and $C = 159\ \mu$F. By applying Thevenin's theorem to this circuit, or otherwise, determine the rms magnitude of the current flowing in the capacitor $C$, its peak value and also its phase with respect to the 100 V voltage source.                                                [7]

(b)    The capacitor is now altered to give a resonant frequency of the circuit of 50 Hz. Find the new value of capacitor $C$ and determine the rms magnitude of the capacitor voltage, and its phase, with respect to the 100 V voltage source.           [3]
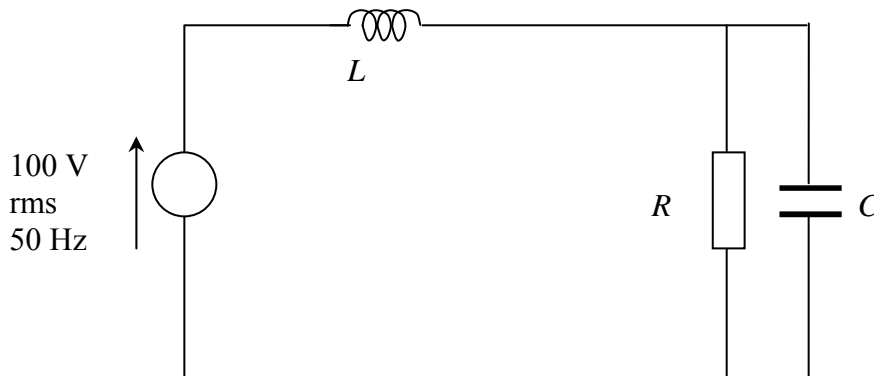


Fig. 2

3 **(short)**

(a)    A 240 V, 50 Hz mains transformer is used to drive a load of $(20+10j)\ \Omega$ with 40 V rms. Assuming the transformer to be ideal, calculate the turns ratio of the windings and the impedance of the load when referred across to the high voltage (primary) side.                                                [4]

(b)    Draw the equivalent circuit of a non-ideal power transformer and briefly explain the physical significance of each of the circuit elements.           [6]

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4 **(long)**    Figure 3(a) shows the circuit diagram of a test probe, its cable and the input section of an oscilloscope. The oscilloscope input impedance is equivalent to a 2 MΩ resistor in parallel with a 30 pF capacitor. The cable is represented by a 40 pF capacitance to the ground.

(a)    The probe may be set to either × 1 or × 10 attenuation by the operation of the switch shown. At low frequencies the effects of capacitance may be ignored. Hence calculate the value of $R$ required to achieve the × 10 attenuation at low frequencies.    [5]

(b)    For the × 1 switch position, and now also considering the capacitors, derive an expression for the complex input impedance, seen at the input to the probe, as a function of frequency.    [10]

(c)    An engineer wishes to measure the voltage at a test point within a television which monitors the line frequency at 20 kHz. An equivalent circuit for the test point is given in Fig. 3(b). Determine the voltage measured with the probe set to × 1 attenuation.    [15]
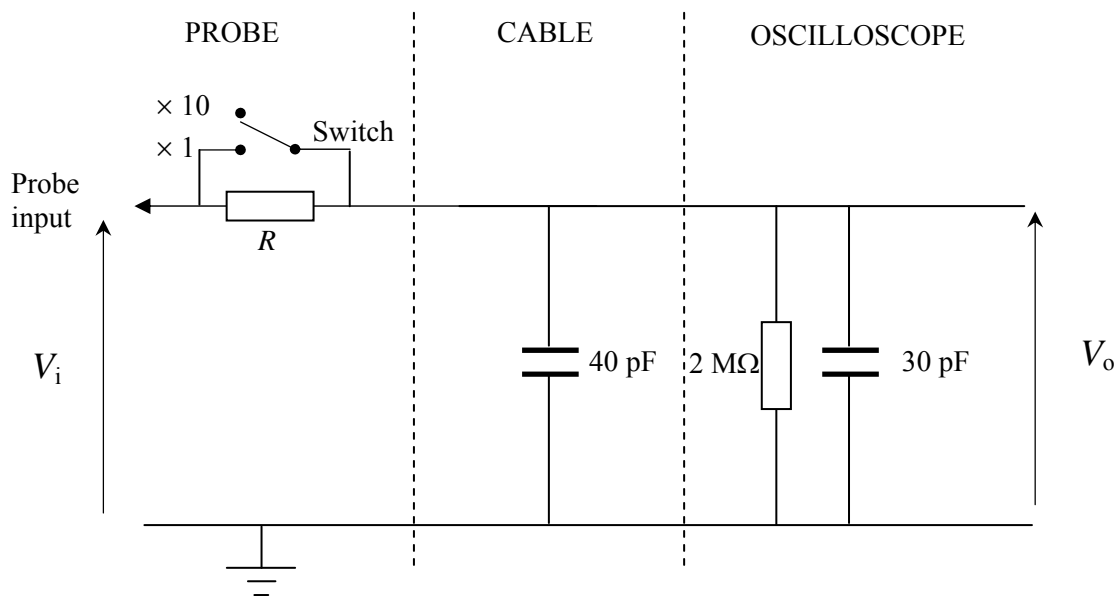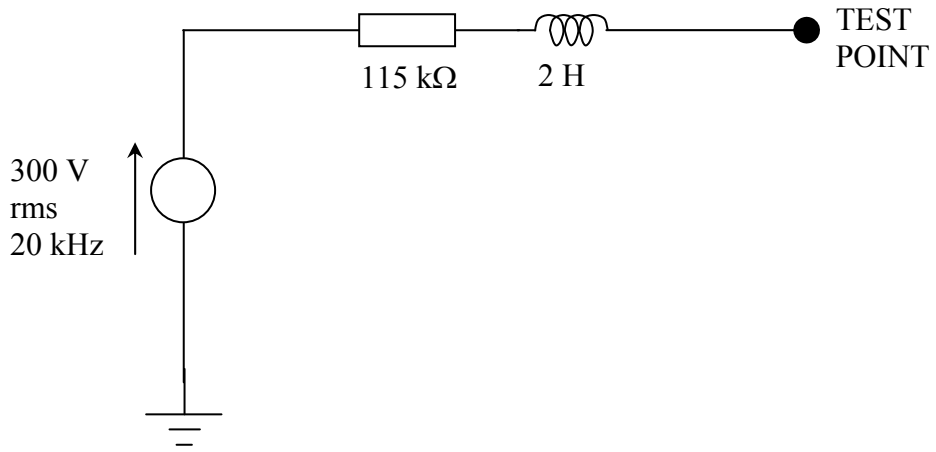


Fig. 3(a)

Fig. 3(b)

**5 (long)**

(a)    Briefly describe the electrical characteristics of an enhanced-mode field effect transistor. [5]

(b)    Draw the small signal model for the source-follower circuit shown in Fig. 4 and derive expressions for the:

(i)    input impedance;
(ii)   gain when no load is connected;
(iii)  output impedance.

Evaluate these parameters with $g_m = 3$ mS and $r_d = 15$ kΩ for the transistor, and with $R_1 = 20$ MΩ and $R_2 = 5$ kΩ. [15]

(c)    If the circuit is used to drive an inductive load of 50 mH, calculate the frequency at which the current through the inductive load drops to 70% of its mid-band value. [10]



Fig. 4

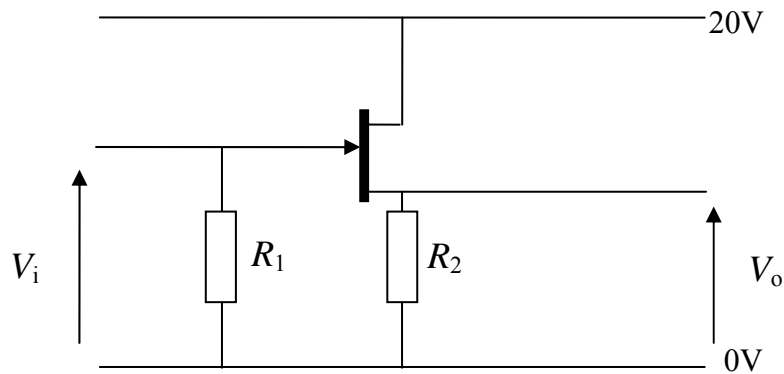SECTION B

6 **(short)**  A four variable function is given by $F = A.\bar{B}.C + B.C.D + A.\bar{C}.D$ , where $\bar{A}.\bar{B}.C.D,$   $A.\bar{B}.C.D$ and $A.B.\bar{C}.\bar{D}$ are don't care states.  Using a Karnaugh map, or otherwise:

(a)  Find the simplest sum of products expression for *F*.  [3]

(b)  Design a circuit to implement *F* using NAND gates only.  [3]

(c)  Design a circuit to implement *F* using NOR gates only.  [4]

7 **(short)**  A serial line carries digital data to a system with input X.  The system is required to detect a sequence 101 and give an output Y at the end of the sequence.  Only non-overlapping sequences should be detected (i.e. the output Y should only be high for the "1" underlined in the input sequence 0101010).  J-K bistables are to be used in the design of the system.

(a)   Draw the state diagram and state how many bistables are required.  [4]

(b)  Write down the state transition table for the system.  [6]

8 **(short)**  A memory chip has 16 data lines and 14 address lines.  The chip is selected when a "0" is input to its chip select pin.  The memory chip is used in a microprocessor system which has a 16 bit wide address bus, where A15 is the most significant bit and A0 is the least significant bit.

(a)  Determine the capacity of the memory chip in kbytes.  [3]

(b)   The memory map of a microprocessor places the memory chip between addresses $8000 and $BFFF.  Write down a Boolean expression for the address decoding logic.  [7]

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9 **(long)**     Figure 5(a) shows a PMOS logic circuit incorporating a FET, whose characteristics are shown in Fig. 5(b), and a resistor which has a value of 1100 Ω.

(a)     Sketch, incorporating appropriate values, the transfer characteristic of the circuit and hence identify its function.     [6]

(b)     Give suitable voltage ranges for HIGH and LOW signals for this circuit.     [4]

(c)     Complete a table of power consumption against input voltage for input voltage values of 0, 2, 4, 6, 8 and 10 V.  Sketch on a graph the power dissipation of the circuit as a function of the input voltage.     [6]

(d)     The resistor is replaced by an NMOS FET as shown in Fig. 5(c).  The properties of the NMOS transistor are shown in Fig. 5(d).  Sketch the transfer characteristic of the new circuit.  Comment on how the power dissipation differs from the first circuit.     [10]

(e)     Identify the logic functions of the circuits in Fig. 5 (e) and (f).     [4]

NOTE:  The graphs in Fig. 5 (b) and (d), are reproduced at the end of this paper.  You may use these to help you complete this question. If you do, you should attach them to your answer.
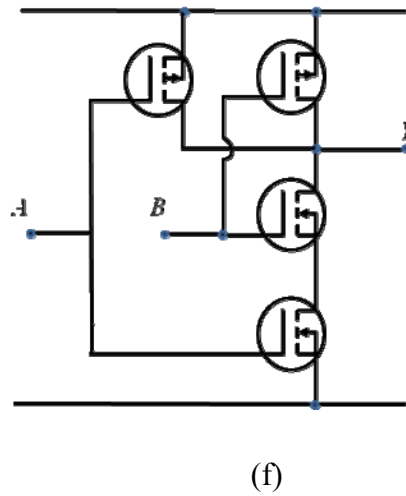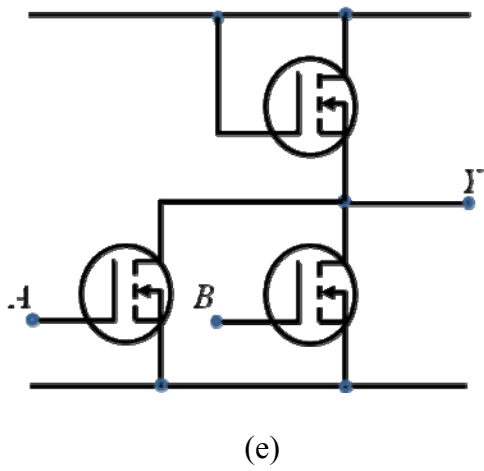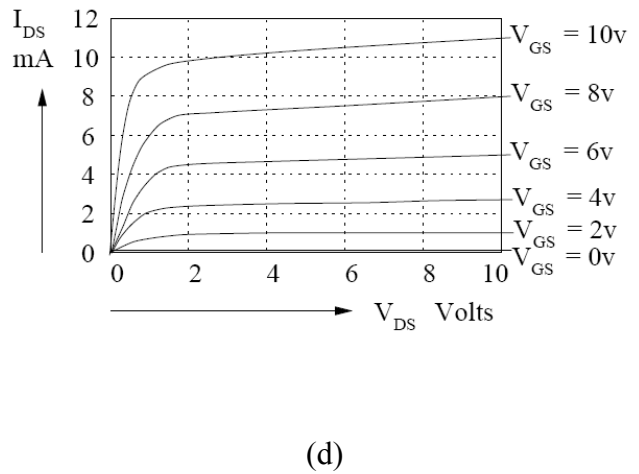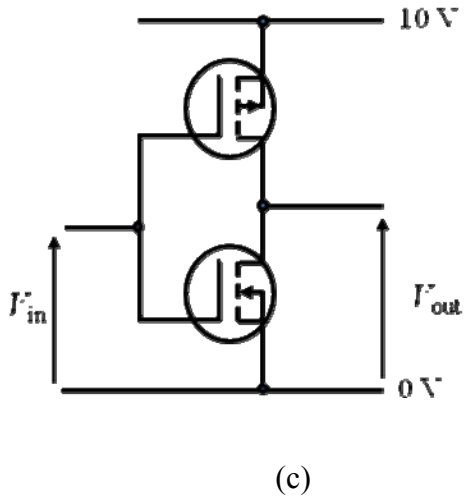
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(a)



(b)



(c)



(d)



(e)



(f)
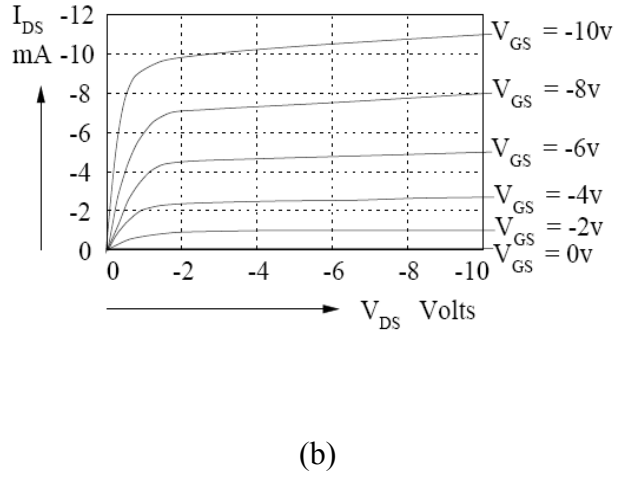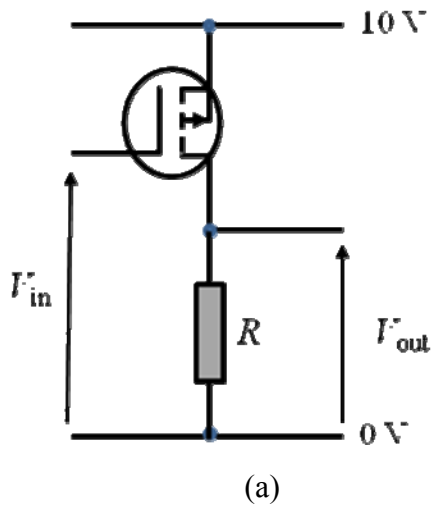
Fig. 5

SECTION C

10 **(short)**

    (a)    Using Gauss's law, derive an expression for a parallel plate, air filled capacitor with plate separation $d$. State any assumptions made.     [5]

    (b)    Show that the electrostatic force on a capacitor plate is $F = 0.5\,QE$, where $Q$ is the total charge and $E$ is the electric field.     [5]

11 **(short)**

    (a)    A straight wire carries a current of 2 A. Find the direction and strength of the magnetic flux density $B$ at a distance of 30 mm perpendicular to the wire, showing your answer on a diagram.     [3]

    (b)    A second wire is placed 80 mm away from and parallel to the first one and contains a current of 4 A in the opposite direction to the first wire. Calculate $B$ at the mid-point between the two wires.     [7]

12 **(long)** Figure 6 shows a semi-circular permanent magnet of radius $R$, thickness $\delta R$ (small) and depth $d$, which is constructed of COLUMAX. The magnet has a soft iron keeper, which is of very high permeability ($\mu_r \sim 10^4$), but which is prevented from touching the pole pieces by a plastic sheet ($\mu_r = 1$) of thickness $t$. The weight of the plastic and the keeper may be ignored.

(a)    If $I = 0$ A, $R = 200$ mm, $\delta R = 10$ mm, $d = 20$ mm, and $t = 0.1$ mm, what is the flux density, $B_c$ , in the magnet?  (Use Fig. 2b, page 7, Electrical and Information Data Book)    [10]

(b)    What force is necessary to pull the keeper from the magnet, with $I = 0$ A?    [10]

(c)    If $N = 10^5$ turns, what current $I$ is necessary for the force between magnet and keeper to be zero?    [5]

(d)    Does the direction of the current matter? What happens if $I$ is increased beyond the value calculated in part (c)?    [5]
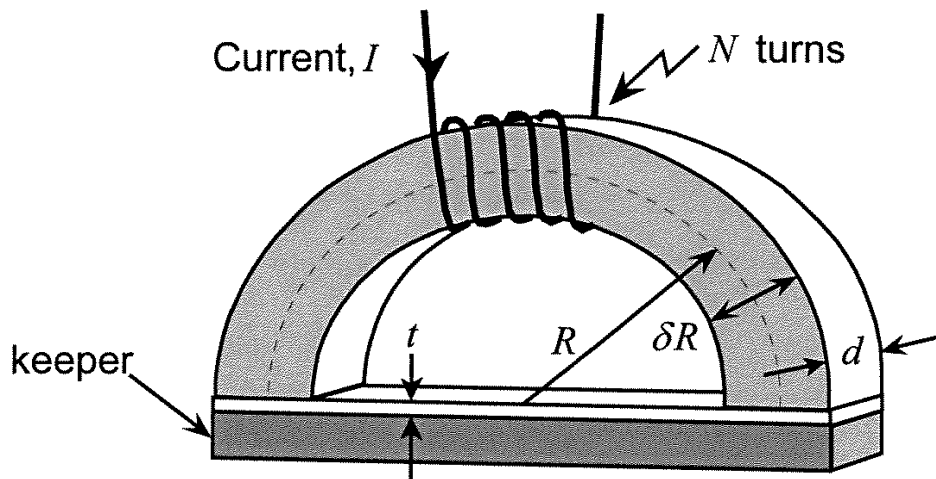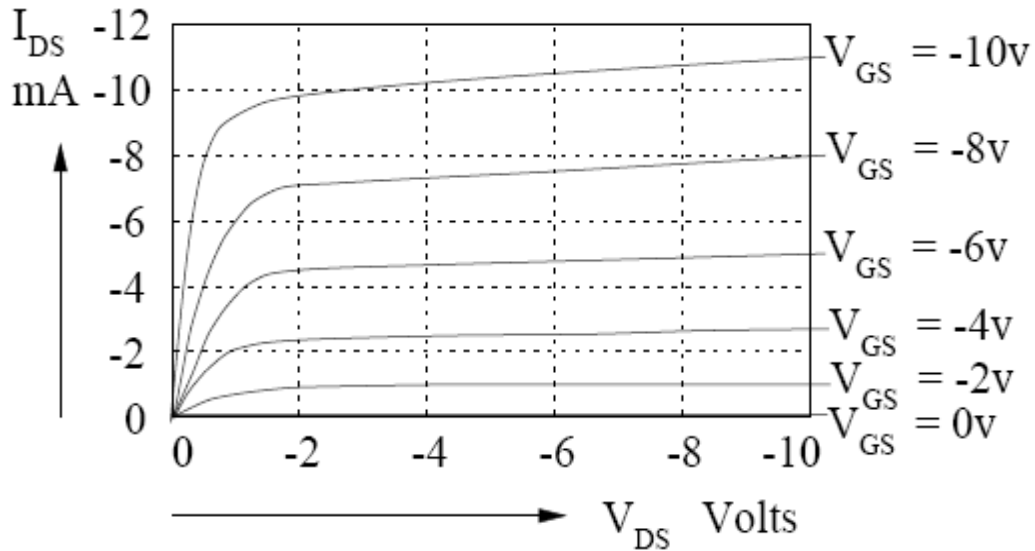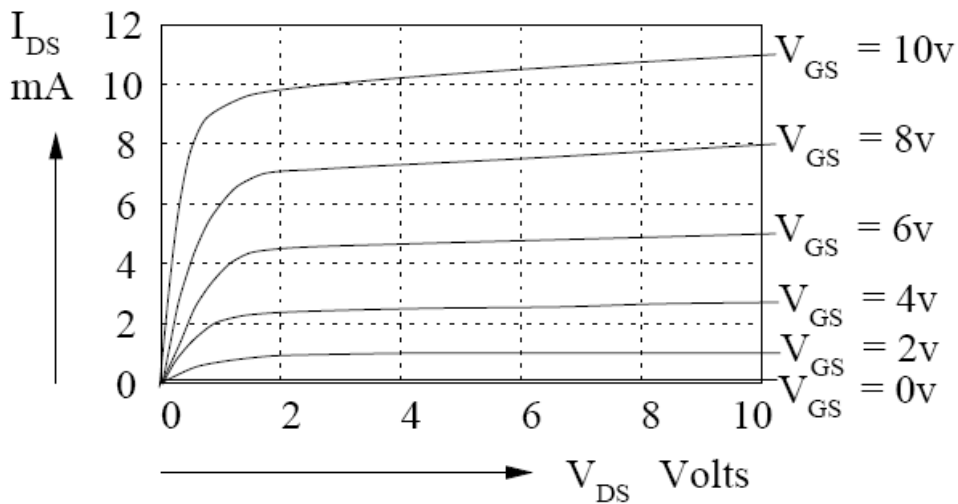


Fig. 6

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PART IA Paper 3 Q9                    Candidate Number _____



PMOS
Fig. 5(b)



NMOS
Fig. 5(d)

NOTE: The graphs in Fig. 5 (b) and (d), for Q 9 are reproduced here. You may use these to help you complete this question. If you do, you should attach them to your answer.

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