

ENGINEERING TRIPOS PART IA

Monday 10 June 2013

9 to 12

Paper 3

ELECTRICAL AND INFORMATION ENGINEERING

Answer *all* questions.

The *approximate* number of marks allocated to each part of a question is indicated in the right margin.

Answers to questions in each section should be tied together and handed in separately.

Attachments: Copy of Fig. 2 for question 1.

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS

Engineering Data Book

CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

SECTION A

1 (long)

(a) A small camera which is used for monitoring traffic flow at the side of a road takes a constant d.c. current of 50 mA when operational. It is connected to a 0.9 V battery and circuit as shown in Fig. 1(a). Calculate the potential difference across the camera, V_c , and the current from the battery, I_b . [10]

(b) Fig. 1(b) shows the equivalent circuit of a solar cell which is being illuminated by sunlight. It consists of a 100 mA ideal current source in parallel with a diode and a $6\ \Omega$ parasitic shunt resistance. If the characteristics of the diode are as shown in Fig. 2, calculate the output voltage, V_o , between the cell's terminals (marked A and B). A copy of Fig. 2 is reproduced at the end of this paper for you to detach and hand in with your answer. [10]

(c) The solar cell is connected to the camera circuit by connecting terminal A to terminal A' and terminal B to terminal B' in Fig. 1. Calculate the new output voltage from the solar cell, V_o , and the current I_b that is now taken from the battery. [10]

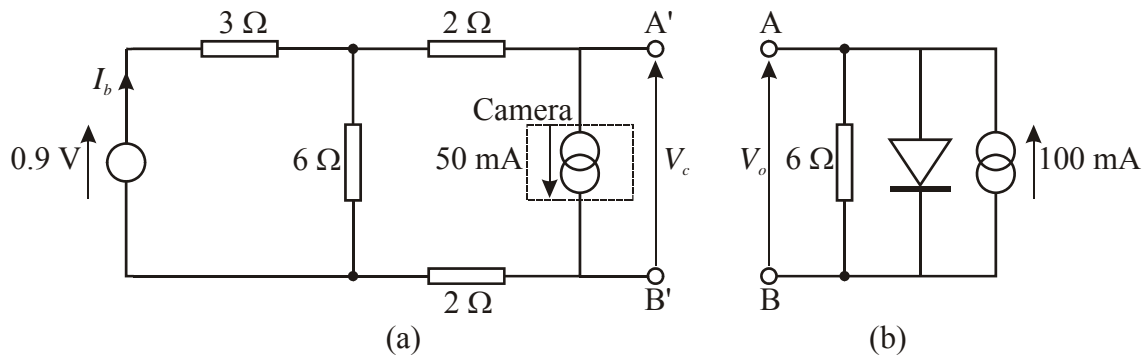


Fig. 1

(cont.)

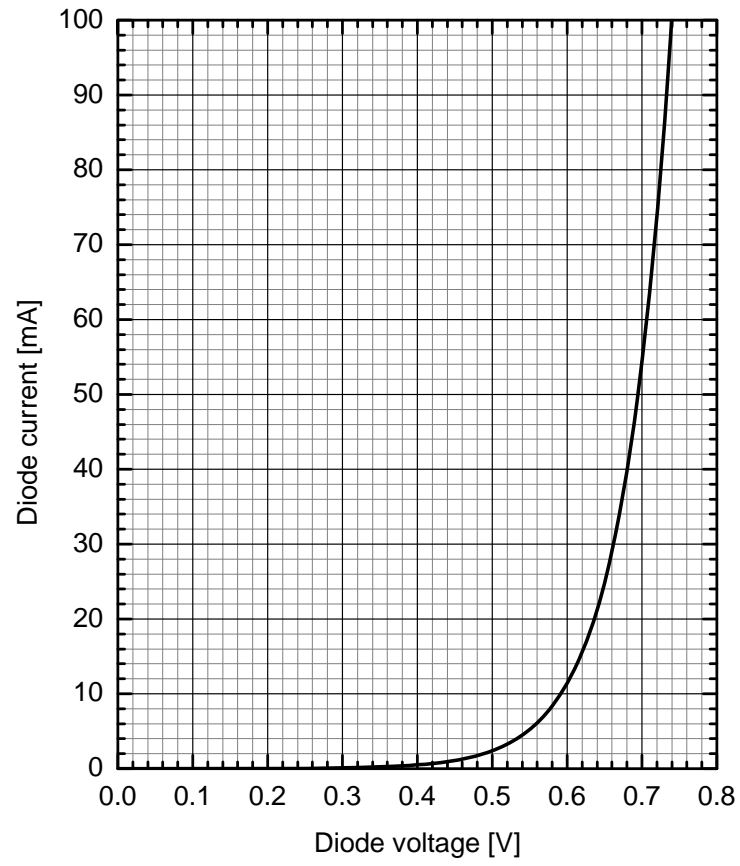


Fig. 2

(TURN OVER

2 (**long**) A factory manufacturing windows uses 30 kW of power to heat the glass to form it into sheets. As shown in Fig. 3, it is connected to a power station via a transmission line of impedance $(100 + 100j) \Omega$ through a 10 kV r.m.s. to 240 V r.m.s. step-down transformer. The transformer may be considered as being ideal. The r.m.s. voltage and current on the secondary side of the transformer are 240 V and 147 A respectively, and the phase of the current lags the voltage. The other end of the transmission line is connected to a power station generating at a frequency of 50 Hz.

- (a) Calculate the power factor of the factory. [3]
- (b) Determine the real power dissipated in the transmission line. [4]
- (c) Calculate the r.m.s. voltage, V_p , at the power station end of the transmission line. [7]
- (d) The power factor of the factory is to be corrected to 1 by connecting a capacitor across the secondary side of the transformer (in parallel with the factory).
- (i) Calculate the capacitance required to achieve this. [4]
- (ii) If the r.m.s. voltage on the secondary side of the transformer is still 240 V, calculate the real power that is now dissipated in the transmission line. [4]
- (iii) Determine the total impedance of the transmission line and factory as seen by the power station. [8]

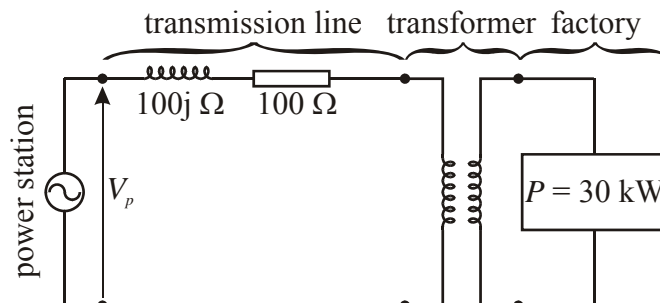


Fig. 3

3 (short) Figure 4 shows the circuit diagram of a single-stage field effect transistor (FET) amplifier circuit that is being used to amplify the signal from a microphone.

(a) Explain the purpose of the capacitors C_1 , C_2 and C_3 in the circuit. [4]

(b) Draw the small-signal equivalent circuit of the amplifier circuit operating at mid-band frequencies. [6]

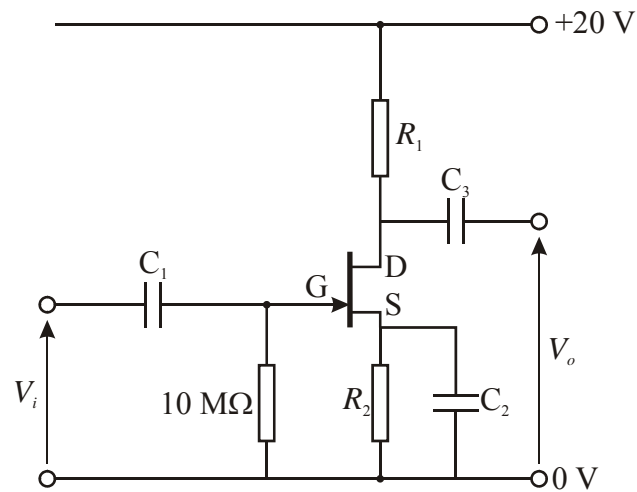


Fig. 4

(TURN OVER

4 (**short**) Using an ideal operational amplifier, design a circuit that will amplify signals with a midband gain of -15 . The circuit should have an input resistance of $1\text{ k}\Omega$ and well-defined lower and upper -3 dB frequencies of 20 Hz and 20 kHz respectively. [10]

5 (short) Fig. 5 shows a series resonant circuit that is connected to a radio antenna. The antenna produces an r.m.s. voltage of $500\ \mu\text{V}$ and has an internal resistance of $100\ \Omega$. The $10\ \text{mH}$ inductor and variable capacitor may be considered to be ideal. The circuit has been tuned to BBC Radio Cambridgeshire at a frequency of $1.026\ \text{MHz}$.

(a) Why will the circuit resonate at a particular frequency? What is oscillating? [4]

(b) What resistance, R , is required if the half-power bandwidth of the circuit is required to be $5\ \text{kHz}$? [6]

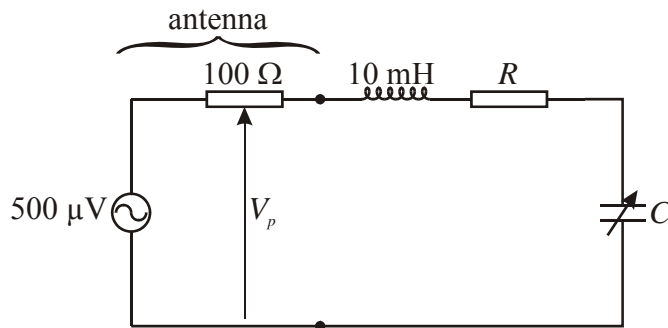


Fig. 5

(TURN OVER

SECTION B

6 (**long**) A microprocessor has an 8 bit data bus, a 16 bit address bus and an active low chip-select \overline{CS} port. Several integrated memory circuits made of individual memory elements which use bistables to store bits of data are to be connected to the microprocessor. Each integrated memory circuit has an 8 bit data bus and a 14 bit address bus and an active high ENABLE port.

- (a) Explain the terms *data bus* and *address bus*. [3]
- (b) Calculate the number of bistables needed for each of the integrated memory circuits. Express the capacity of this memory device in kbytes. [3]
- (c) Figure 6 shows a one-bit memory element which is the building block of the integrated memory circuit. The one-bit memory element incorporates an SR bistable and two tri-state buffers, D1 and D2. Describe the operation of the one-bit memory element, including the role of the tri-state buffers, and briefly explain what the signals X, Y and Z/W represent. [12]
- (d) Determine how many integrated memory circuits can be connected to the microprocessor. Draw the address decoding circuit and the main connections from the microprocessor to the integrated memory circuits including the data bus, address bus and \overline{CS} and ENABLE ports. [12]

(cont.

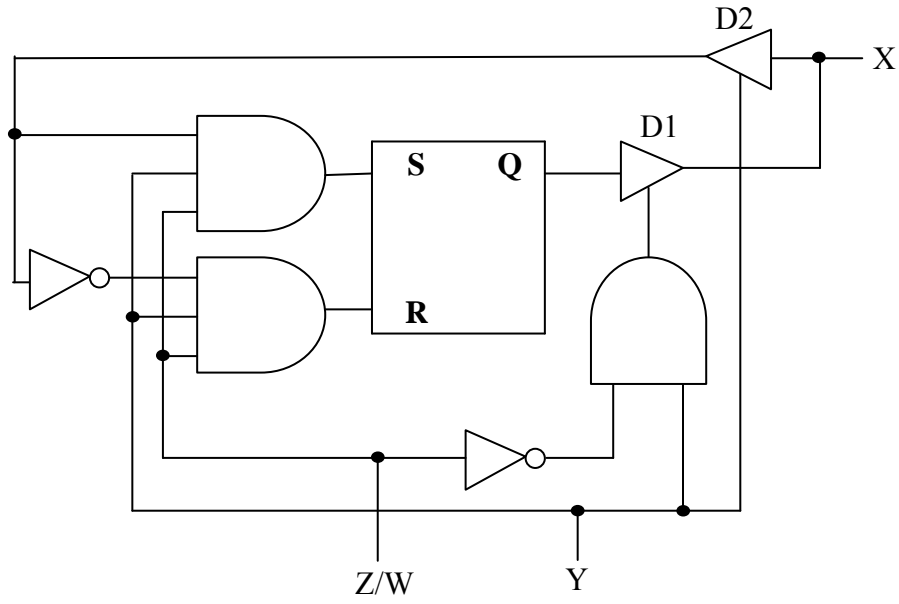


Fig. 6

(TURN OVER

7 (**short**) A half adder adds two single binary digits (A and B) and has two outputs, sum (S) and carry (C_{out}). A full adder circuit adds two binary digits but also accounts for a digit carried in (C_{in}) as well as out (C_{out}).

(a) Derive logical expressions for the outputs of the half adder in terms of its inputs and draw a circuit implementation using one XOR gate and other gates if needed. [4]

(b) Derive logical expressions for the outputs of the full adder in terms of its inputs and draw a circuit implementation using logic gates. [6]

8 (short) A two-bit counter implemented using D-type bistables is shown in Fig. 7.

- (a) Draw the state diagram for the two-bit counter. [5]
- (b) What is the code implemented by this counter and why is this advantageous in certain applications? [2]
- (c) How would you reconfigure the counter to reverse the sequence determined above? Draw the actual circuit implementation. [3]

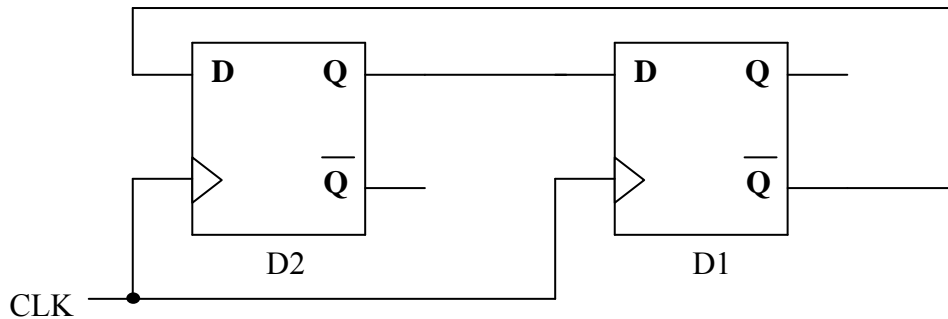


Fig. 7

(TURN OVER

9 (short) The circuit in Fig. 8 shows a simple form of a 4-bit digital-to-analogue converter. Digital '1' is assumed to be 5V and digital '0' is assumed to be 0V.

(a) Briefly explain the principle of operation and the nature of the circuitry that must be connected to the inputs S_0 to S_3 . Which of these inputs represents the least significant bit? [5]

(b) If the value of R is $1\text{k}\Omega$ and the operational amplifier may be assumed to be ideal, determine the input resistance at the terminals S_1 and S_2 . [2]

(c) Determine the output voltage V_o if the digital signal 1011 is present at the inputs. [3]

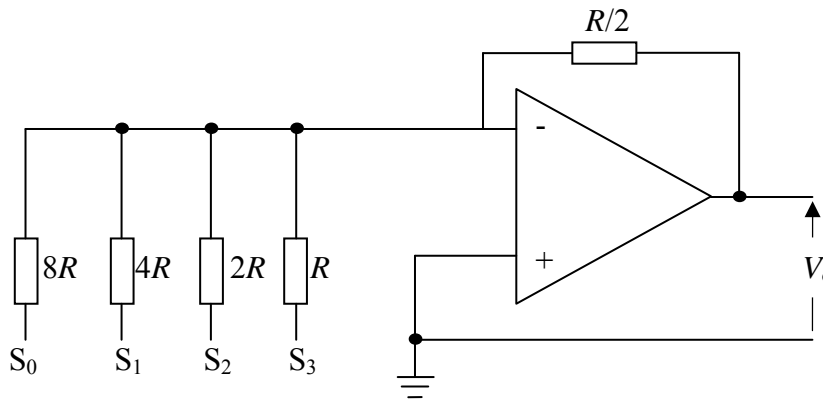


Fig. 8

SECTION C

10 (**short**) A straight, cylindrical solenoid has N turns carrying a current, I . The turns are uniformly wound along the length, l , of the solenoid. The solenoid is air filled and l is long compared to the solenoid radius.

(a) Using Ampere's law, show that the magnetic flux density, B , inside the solenoid can be approximated by

$$B = \frac{\mu_0 NI}{l}$$

where μ_0 is the permeability of free space. [3]

(b) Hence, calculate the self-inductance of the solenoid if $N = 300$, $l = 25$ cm and the cross-sectional area of the solenoid is 4 cm^2 . [5]

(c) Calculate the self-induced voltage in the solenoid if the current through it, I , is decreasing at a rate of 50 A s^{-1} . [2]

(TURN OVER

11 (**short**) An ideal parallel plate capacitor has a plate separation d , plate area A , and a capacitance C_0 when there is only air between the plates.

(a) For each of the following new configurations, determine the ratio of the capacitance of the new configuration to the capacitance C_0 :

(i) a slab of dielectric material of relative permittivity 3 and thickness $d/3$ is inserted midway between the plates; [3]

(ii) an uncharged metal slab of thickness $d/3$ is inserted midway between the plates. [3]

(b) The capacitor is fully filled with a dielectric material of relative permittivity 2. The capacitor is charged to a potential difference between the plates of 50 V and then electrically isolated. Then the dielectric is removed. Calculate the potential difference that now exists between the plates of the capacitor. [4]

12 (**long**) As shown in Fig. 9, a coaxial cable of length L consists of a solid inner cylindrical conductor of radius a , concentrically surrounded by a tubular non-magnetic dielectric with outer radius b and a cylindrical outer conductor with outer radius c .

(a) A potential difference is applied between the ends of the cylindrical outer conductor which produces a current parallel to its axis. Determine the resistance of the outer conductor in terms of L , b , c and the resistivity ρ_C of the material used. [5]

(b) The inner conductor carries a current I with a non-uniform current density, $J = \alpha r$, where α is a constant and r is the radial distance from the centre. The current in the outer conductor is equal and opposite. Assuming that the relative permeability is 1 everywhere, use Ampere's law to determine the magnetic flux density for:

- (i) $r > c$;
 - (ii) $r < a$;
 - (iii) $a < r < b$.
- [15]

(c) The dielectric between the inner and outer conductor has a finite resistivity ρ_D . Hence, for a potential difference applied between the inner and outer conductor, a leakage current flows radially. Determine the resistance of the coaxial dielectric in terms of L , a , b and ρ_D . (Hint: consider the current passing through a sequence of cylindrical shells of radius r and thickness δr , with each shell having a resistance δR .) [10]

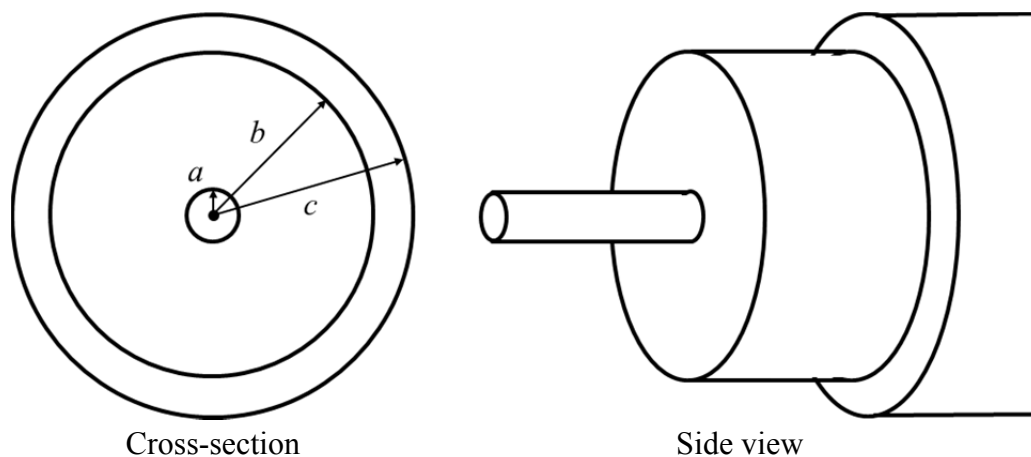


Fig. 9

Answers to questions

1. (a) 0.3 V, 133 mA (b) 0.56 V (c) 0.45 V (d) 116 mA
2. (a) 0.85 (b) 1245 W (c) 10.45 kV
(d) (i) 1.03 mF (ii) 900 W (iii) $(3433+100j) \Omega$
5. (b) 214 Ω
6. (b) 16 kbytes
9. (c) -3.4375 V
10. (b) 181 μH (c) 9.05 mV
11. (a) (i) 9/7 (ii) 3/2 (b) 100 V

A.J. Flewitt, F. Udrea, S. Hofmann