ANSWERS 3B2 2003 F. UDREA

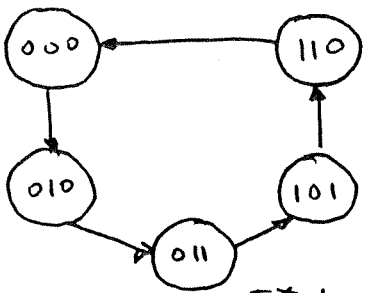
Q1:

a)

1. To systematically examine each term of the logic expression
2. To group terms with the same number of 'High' variables and place them in the same block as part of a list
3. To build a sequence of lists by combining terms from adjacent blocks which satisfy: $P0Q + P1Q = PQ$ where P and Q are groups of variables. This is done repeatedly, the remaining terms which did not combine are 'Prime Implicants'.
4. Using a table, named 'Prime Implicant table', the prime implicants are compared to the original expression.
5. The final solution is based on the minimal and simplest set of terms 'to cover' the original expression.

Don't cares are used in the lists but not in the Prime Implicant tbl

b)

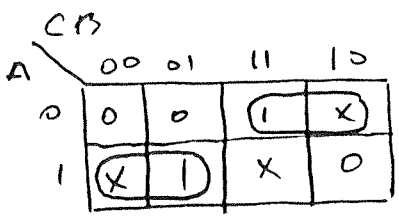


Toggle excitation tbl

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

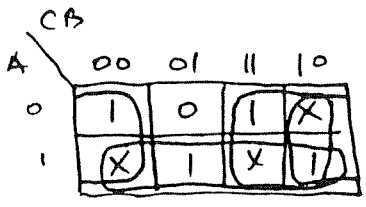
Present state C B A	Next state C^+ B^+ A^+	Toggle inputs TC TB TA
0 0 0	0 1 0	0 1 0
0 0 1	x x x	x x x
0 1 0	0 1 1	0 0 1
0 1 1	1 0 1	1 1 0
1 0 0	x x x	x x x
1 0 1	1 1 0	0 1 1
1 1 0	0 0 0	1 1 0
1 1 1	x x x	x x x

From the state table:



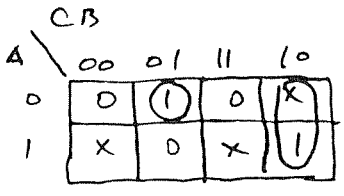
TC

$TC = \bar{A}C + A\bar{C} = A \oplus C$



TB

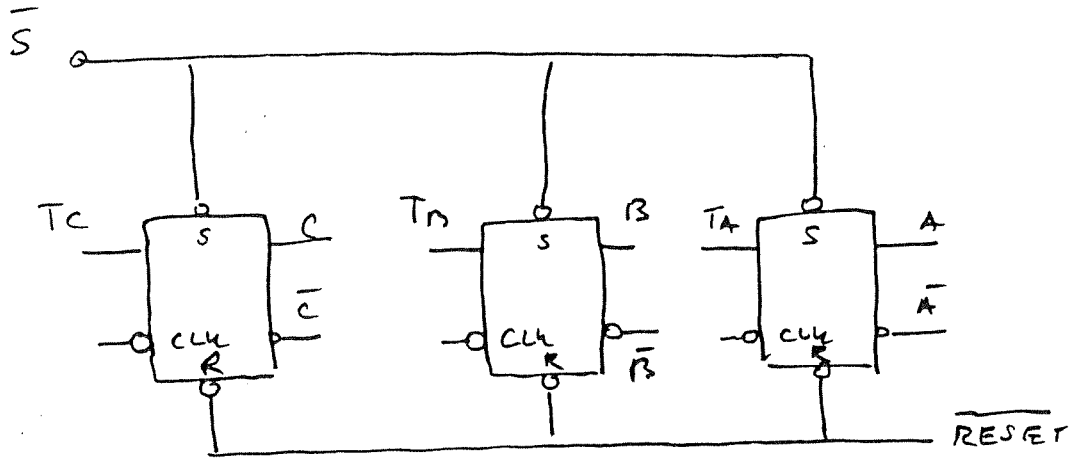
$TB = A + \bar{B} + C$

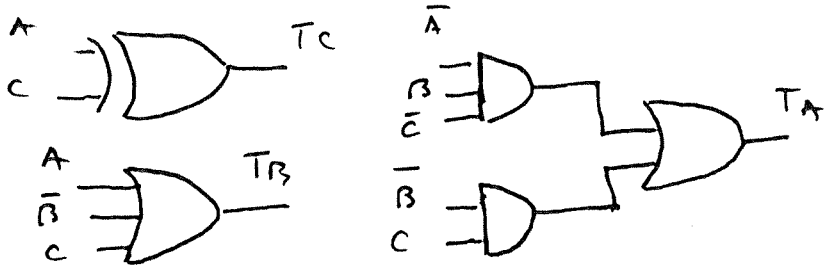


TA

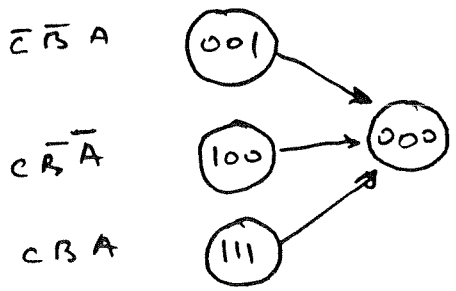
$TA = \bar{A}B\bar{C} + \bar{B}C$

CIRCUIT IMPLEMENTATION

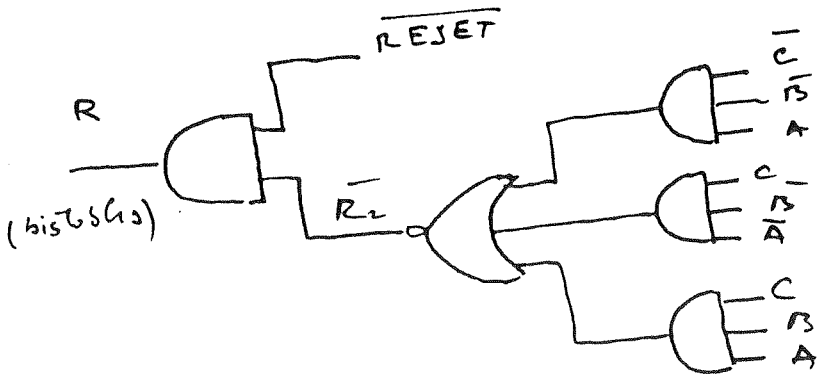




c) The undefined states can be made to advance to 000 by resetting the bistables



$$\overline{R_2} = \overline{\bar{C}\bar{B}A + C\bar{B}\bar{A} + CBA}$$



It is also possible to use a monostable to force the counter in 000

Q2:

a) Definition: A hazard is defined as an actual or potential malfunction of a circuit due to signals encountering delays in the paths of a network. Every active gate has a propagation time (10ns). Every length of wire has a delay associated with it (3ms/m).

The main type of hazards that can occur in a asynchronous circuit are given below:

(1) A static hazard is a momentary change of state not defined by the inputs. There are two types of static hazards:

- static-1 hazard: normal output = 1
- static-0 hazard: normal output = 0

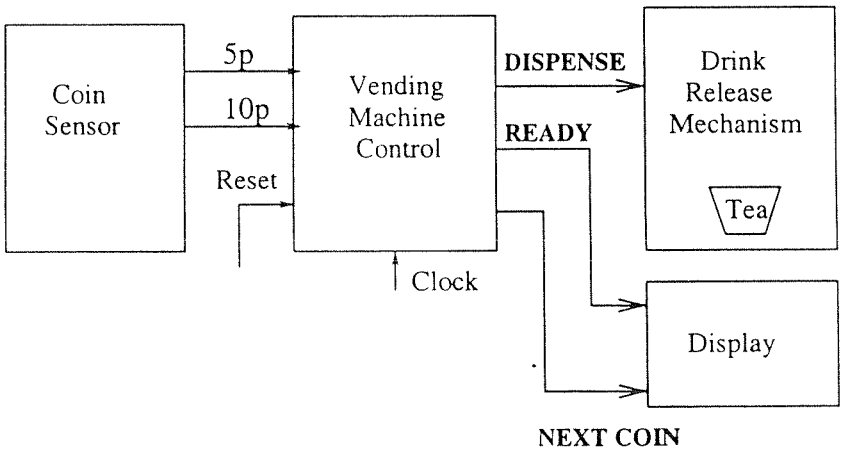
(2) A dynamic hazard: output changes several times before settling down.

(3) A function hazard is shown when more than one input changes at a time -very difficult to analyse.

(4) An essential hazard is caused by a race between an input signal change and an output change.

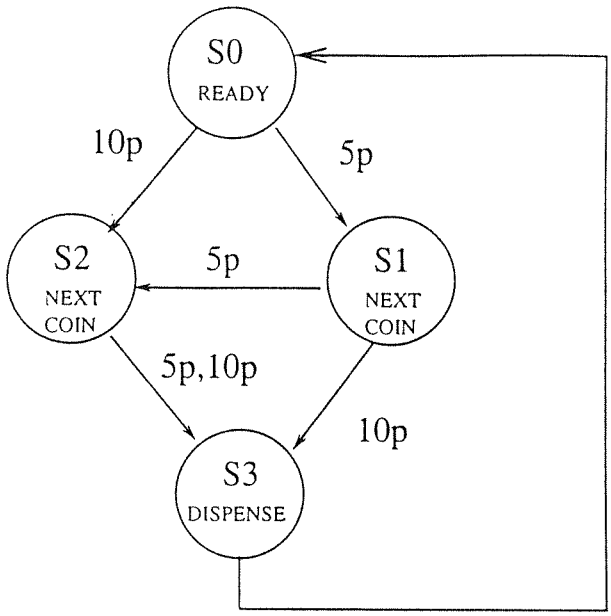
b)

The vending machine diagram is shown below. This helps us to understand the problem. There are two inputs, 5p and 10p and three outputs: DISPENSE, READY and NEXT COIN.



A good way to begin the design is to enumerate all the possible unique sequences of inputs which lead to releasing the drink and the output .

- Three 5p coins in sequence
- Two 5p coins followed by a 10p coin in sequence (note that here the customer looses 5p)
- One 5p coin followed by a 10p coin in sequence
- One 10p coin followed by 5p coin in sequence



- Two 10p coins in sequence

  The state diagram can then be obtained as shown below:

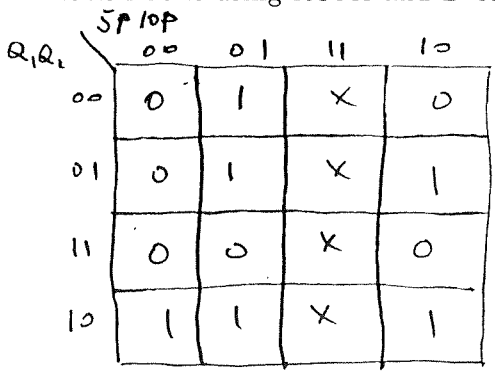
  There are 4 states, S0,S1,S2.S3. Since the output is only dependent on the state, this is a Moore circuit. If no coins are received the machine remains in the same state. Also note that two coins cannot be received at the same time.

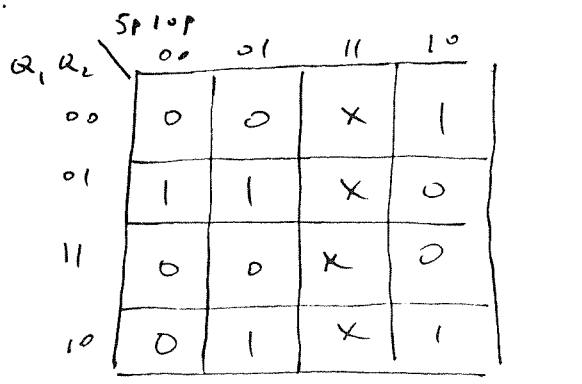
  The state table which includes the allocation of states is given below:

Present State		Next state for 5p 10p = 00	01	11	10	DISPENSE	READY	NEXT COIN
S0	00	00	10	–	01	0	1	0
S1	01	01	11	–	10	0	0	1
S3	11	00	00	–	00	1	0	0
S2	10	10	11	–	11	0	0	1

  The table translates in the k-maps below:

  The implementation can be done in several ways. The figure below shows the implementation done using ROMs and D bistables.





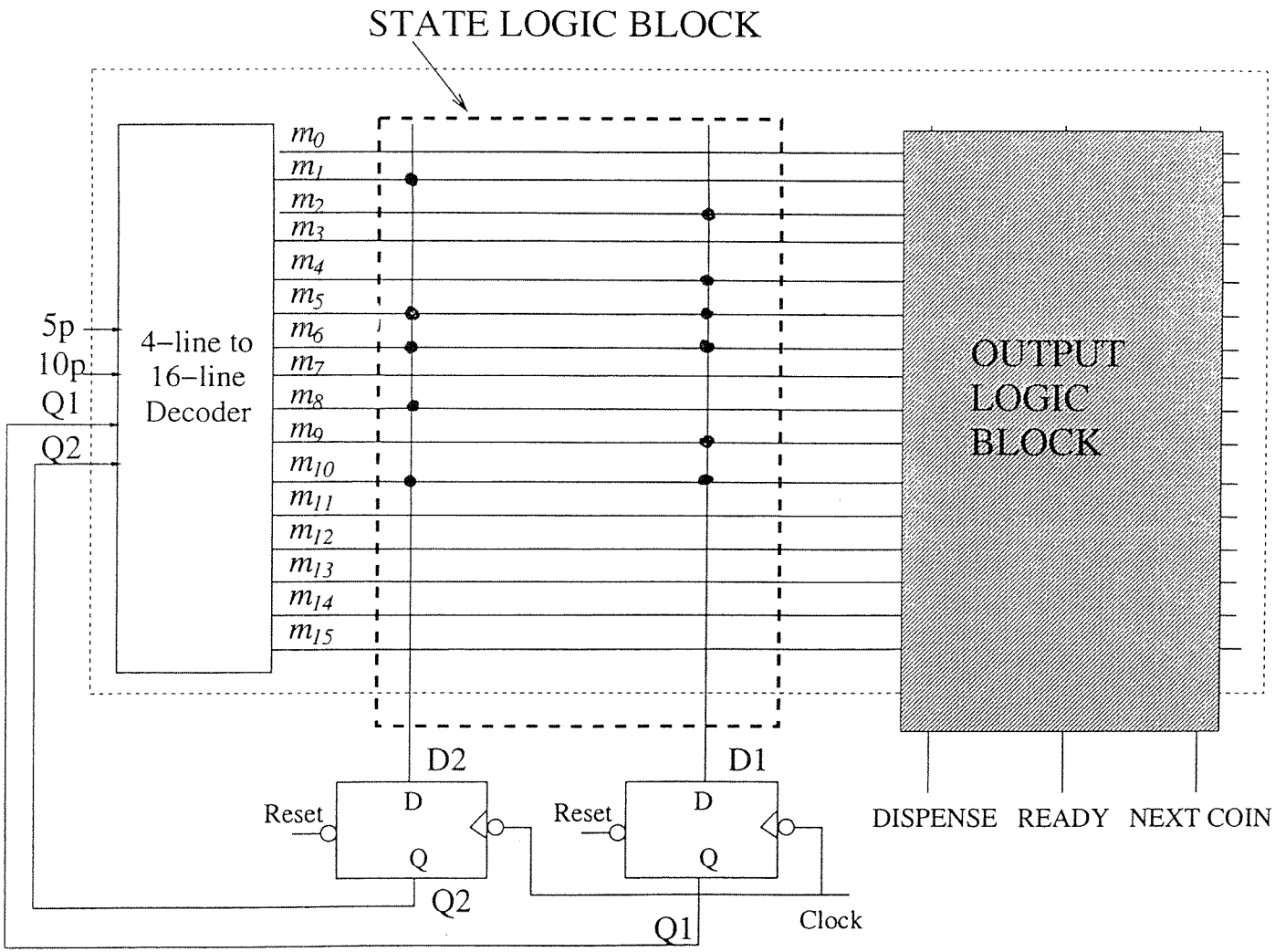


Figure 1

3.

(a)(i) For inverter A, when $V_{IN} = 0$ V_O becomes V_{OH}

M1 does not conduct since no channel formed ($V_{GS} < V_T$) however in order that M2 may conduct its source can rise no higher than $V_{DD} - V_{Tn} = 4V$ $\therefore V_{OH} = 4V$

For inverter B, when $V_{IN} = 0$ V_O becomes V_{OH}
M1 does not conduct. M3 is fully conductive
Hence $V_{OH} = V_{DD} = 5V$

(ii) For inverter A, when $V_{IN} = V_{DD}$ V_O becomes V_{OL}
First assume $V_{DS} = V_{OL}$ is of order 1V or less so that M1 is in non-saturated mode, $V_{DS} < V_{GS} - V_T$
We will later confirm this assumption,
For M2, since $V_{GS} \equiv V_{DS}$, the device is always in saturation
Drain currents in M1 and M2 are equal (assuming no current drawn from output.

$$K_1 = 2 \times 10 \times 10^{-6} \qquad K_2 = 0.2 \times 10 \times 10^{-6}$$

$$\frac{K_1}{2}\left[2(V_{DD} - V_{T1})V_{OL} - V_{OL}^2\right] = \frac{k_2}{2}\left[V_{DD} - V_{OL} - V_{T2}\right]^2$$

$$10^{-5}\left[2.4.V_{OL} - V_{OL}^2\right] = 10^{-6}\left[4 - V_{OL}\right]^2$$

$$80\,V_{OL} - 10\,V_{OL}^2 = 16 - 8\,V_{OL} + V_{OL}^2$$

and $V_{OL} = 7.8$ or $\underline{0.19}$ Only the 2nd is has physical significance

For inverter B, when $V_{IN} = V_{DD}$ V_O becomes V_{OL}
M2 does not conduct since $V_{SG1} < 1V$
M1 is fully conductive
Hence $V_{OL} = 0V$.

Note that the assumption made, that $V_{OL_A} \lesssim 1V$ is seen to be confirmed

(b) M3 must have the same ON conductance as M1 in order to equalise the delays. Since the same $|V_{GS}|$ of 5V is applied to both devices, it is only necessary to ensure that

$$K_3 = K_1 \quad \text{or} \quad \frac{W_3}{L_3} \times 5 \times 10^{-6} = 2 \times 10^{-5}, \text{ or } \frac{W_3}{L_3} = 4$$

3 (cont) (iii) If the input switches abruptly, the delay is given by the time taken for C_L to charge from V_{OL} to $(V_{OH}+V_{OL})/2$

For inverter A, as V_{IN} falls M1 switches off and C_L charges via the channel of M_2 towards V_{OH}. Since M2 is at all times in saturation it may be regarded as a constant current source with current I_D given by:-

$$I_D = \frac{K_2}{2}(V_{DD} - V_O - V_{T2})^2 = 10^{-6}(4-V_O)^2$$

I_D falls to a very small value as V_O approaches $V_{DD} - V_{T2}$

Using $\frac{dV}{dt} = \frac{I}{C}$ we can write:-

$$\frac{dV_O}{dt} = \frac{I_D}{C_L} = \frac{10^{-6}}{10\times10^{-12}}(4-V_O)^2$$

$$\text{or } T_{del} = 10\times10^{-6}\int\frac{dV_O}{(4-V_O)^2}$$

where the limits of the integration are the initial value of V_O (V_{OL}) and $(V_{OL}+V_{OH})/2$, or 0.19V and 2.1V.

$$T_{del} = \left[\frac{1}{4-V_O}\right]_{0.19}^{2.1} \times 10^{-5} \text{ s}$$

$$= \left(\frac{1}{1.9} - \frac{1}{3.21}\right)\times10^{-5} = 2.1\,\mu\text{S}$$

For inverter B, the initial and 50% values are 0 and 2.5V. In this instance, with $K_3 = K_1$ the delays have been equalised. As for inverter A, M_1 is switched off so M3 alone governs the delay. It passes through both regions of operation, with $|V_{GS}| = 5$V, and its V_{DS} is initially -5V, but falling towards -2.5V.

M3 remains unsaturation until $V_{DS} = -4$V (i.e. $V_O = 1$V) and in this interval acts as a current source with current:-

$$I_{D3} = \frac{K}{2}(-5+1)^2 = \frac{4}{2}\times10\times10^{-6}\times(-4)^2 = 32\times10^{-5}$$

With this current, the time taken to charge C_L from 0V to 1V is $t_{sat} = C_L \times 1/I_{D3} = 10^{-11}/32\times10^{-5} = 0.031\times10^{-6}$ s

$= 31$ nS

Q3(cont) (iii) ...

After V_o rises to 1V or above M3 enters its non-saturated region and its drain current thereafter depends on V_o

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad \text{Substitute:-}$$

$$V_{GS} = -5,\ V_T = -1,\ V_{DS} = V_{DD} - V_o = 5 - V_o$$

$$I_D = \frac{k}{2}\left[2(-5+1)(5-V_o) - (5-V_o)^2\right]$$

$$= -\frac{k}{2}\left[V_o^2 - 18V_o + 65\right] \quad \text{As before, } \frac{dV_o}{dt} = -\frac{I_D}{C_L}$$

$$\frac{dV_o}{dt} = \frac{k}{2C_L}\left[V_o^2 - 18V_o + 65\right], \text{ and}$$

$$dt = \frac{dV_{out}}{\frac{k}{2C_L}\left(V_o^2 - 18V_o + 65\right)} = \frac{2C_L\ dV_{out}}{k\ (V_o - 13)(V_o - 5)}$$

Integrate + put in limits, and simplify with partial fractions

$$T_{non\text{-}sat} = \frac{2C_L}{k}\frac{1}{8}\int_1^{2.5}\left(\frac{1}{V_o - 13} - \frac{1}{V_o - 5}\right)dV_o$$

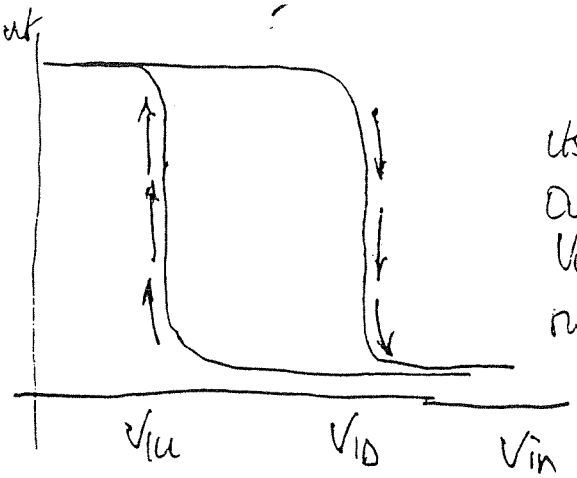
$$= \frac{2\times10^{-11}}{8\times4\times10^{-5}}\left[\ln(V_o - 13) - \ln(V_o - 5)\right]_1^{2.5}$$

$$= \frac{2\times10^{-11}}{32\times10^{-5}}\left(\ln\frac{10.5}{2.5} - \ln\frac{12}{4}\right) = 21\times10^{-9}\ s$$

Total delay = $T_{sat} + T_{non\text{-}sat}$ = 31 + 21 nS = 52 nS

	Advantages	Disadvantages
Example: nMOS (A)	Simple process, low cost No risk of latch up	Poor noise margin Slow rise time Significant power consumption Static sensitive Very poor drive ability
enMOS (B)	Excellent noise margins Fully restored levels Symmetric rising/falling delay possible Very low consumption at LF Popular, compact Compatible with linear MOS (B)	More complex process Possibility of latch up Static sensitive Relatively poor drive ability

4.



This represents a Schmitt inverter - its VTC exhibits a hysteresis loop

Output transitions :-

Vout makes its H→L transition when the rising edge exceeds $V_{in} = V_{ID}$

It makes the L→H transition when the falling edge drops below $V_{in} = V_{IL}$

The condition $V_{ID} > V_{IL}$ must be met

The hysteresis is defined as $V_{ID} - V_{IL}$, and must be > 0.

~~4 cont~~

The circuit given resembles an INVERTER but has a stack of 2 series connected PMOS devices (P1, P0) and two series NMOS devices (N0, N1) with all inputs common. The output is taken from the centre of the stack. As so far described the function (with a regular logic signal input) would be that of an inverter. Feedback devices N_F, P_F provide a form of +ve feedback and modify the VTC

1(a) With Vin at ground = 0V, the output is expected to be V_{OH}. N_1 is cut off and there is no current path in the stack. However P_1 is non-saturated and highly conductive, and its drain is at virtually V_{DD}. Hence V_{GS} for P0 is enough to bring it too to its non-saturation region. There is a highly conductive pull-up to V_{DD} and open cct to 0V. Since the drain currents are negligible, and assuming no current drawn from Vo, there is negligible drop across channels of P_1, P_0. Hence the output voltage is $V_{OH} = V_{DD}$ and is maintained provided $V_{IN} < V_{Tn}$.

By symmetry, if V_{IN} lies between V_{DD} and $V_{DD} - |V_{TP}|$ the output will be at V_{OL}, with open-circuit p-channel device and a conductive pull-down to 0V given that $V_{OL} = 0$

(b) for the output LOW to HIGH transition. When V_{IN} falls below $V_{DD} - |V_{TP}|$ P_I switches on. With the gate of PF at 0V and its drain (wired to to earth) at 0V, $V_{DS} = 0V$ and by definition PF is in its saturation mode. For the moment we will suppose P_I is also in saturation – which will be so if its V_{GS} only slightly exceeds the device's threshold voltage. We will verify this.

If V_{IN} is allowed to fall further, eventually PO will turn on. At this time, the output will make its L→H transition – we want to find the point where PO just begins to conduct. At this point its drain current is still zero, so equating currents P_I and P_F :–

$$\frac{K_{PI}}{2}(V_{DD} - V_{IN} + V_{TP})^2 = \frac{K_{PF}}{2}(V_{SG_{PF}} + V_{TP})^2$$

Solve for V_{SG} to get

$$V_{SG_{PF}} = \sqrt{\frac{K_{PI}}{K_{PF}}}(V_{DD} - V_{IN} + V_{TP}) - V_{TP}$$

We can deduce that the drain of P_I is at $V_{DD} - V_{IN} + V_{TP}$ and hence source of PF

$$V_{out} + V_{SG_{PF}} = 0 + V_{SG_{PF}} = \sqrt{\frac{K_{PI}}{K_{PF}}}(V_{DD} - V_{IN} + V_{TP}) - V_{TP}$$

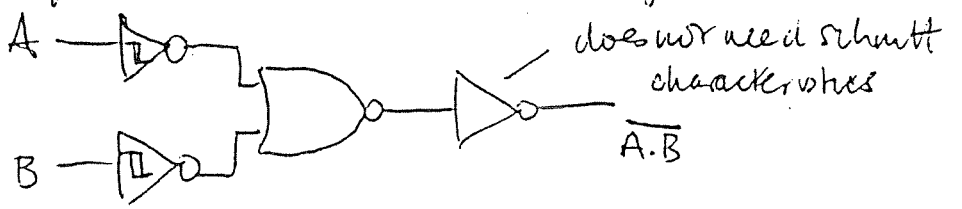
PF will turn on if its gate reaches the value + a further V_{TP} ie, if the input V_{IN} reaches

$$V_{IN} = \sqrt{\frac{K_{PI}}{K_{PF}}}(V_{DD} - V_{IN} + V_{TP}) - V_{TP} + V_{TP} = \sqrt{\frac{K_{PI}}{K_{PF}}}(V_{DD} - V_{IN} + V_{TP})$$

Solve for V_{IN}, and we get :–

$$V_{IN} = V_{IH} = \frac{\sqrt{\frac{K_{PI}}{K_{PF}}}(V_{DD} + V_{TP})}{1 + \sqrt{\frac{K_{PI}}{K_{PF}}}}$$ as required

(c) The circuit shown is effectively an inverter 
To implement a 2 input Schmitt NAND two of these are required. By de Morgan the gate level circuit needed is :-



Hence a suitable transistor level representation for the new parts of the circuit is :-