ENGINEERING TRIPOS PART IIA

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Wednesday 7 May 2003 2.30 to 4.00

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Module 3B2

INTEGRATED DIGITAL ELECTRONICS

Answer not more than ***three*** questions

All questions carry the same number of marks.

The ***approximate*** percentage of marks allocated to each part of a question is indicated in the right margin.

**You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator**

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1 (a) Describe briefly the main steps employed in the Quinne McClusky tabular method for minimising logic functions. [20%]

(b) Design and show the circuit implementation of a 3 bit synchronous counter that advances through the sequence 000, 010, 011, 101, 110, 000 and repeats. The unused states, 001, 100 and 111 are to be used as 'don't care' conditions to simplify the logic. The implementations should use T (toggle) bistables. [50%]

(c) During the power-up, the counter designed in (b) does not always operate correctly because it can start randomly in an unused state. Propose a simple solution to fix this problem by adding a few extra logic gates to the circuit already implemented, without redesigning the counter. [30%]

2 (a) Define a hazard in a logic system and briefly enumerate the types of hazards that can occur in an asynchronous circuit. [20%]

(b) A simple vending machine dispenses a drink for 15 pence in coins. The machine has a single coin slot and accepts 10p and 5p, one coin at a time. Outputs must be generated to operate the drink dispensing mechanism (DISPENSE), the indicator lights signalling that the machine is ready for operation (READY), and in operation waiting for the next coin (NEXT COIN).

Draw schematically the architecture of the vending machine. [20%]

Draw the state diagram and state table showing the allocation of states. [30%]

The circuit implementation of the vending machine is done with D bistables and a ROM. Complete the programmable links in the state logic block of Fig. 1, using the **separate** sheet attached to the back of the examination paper and hand in with your script. [30%]

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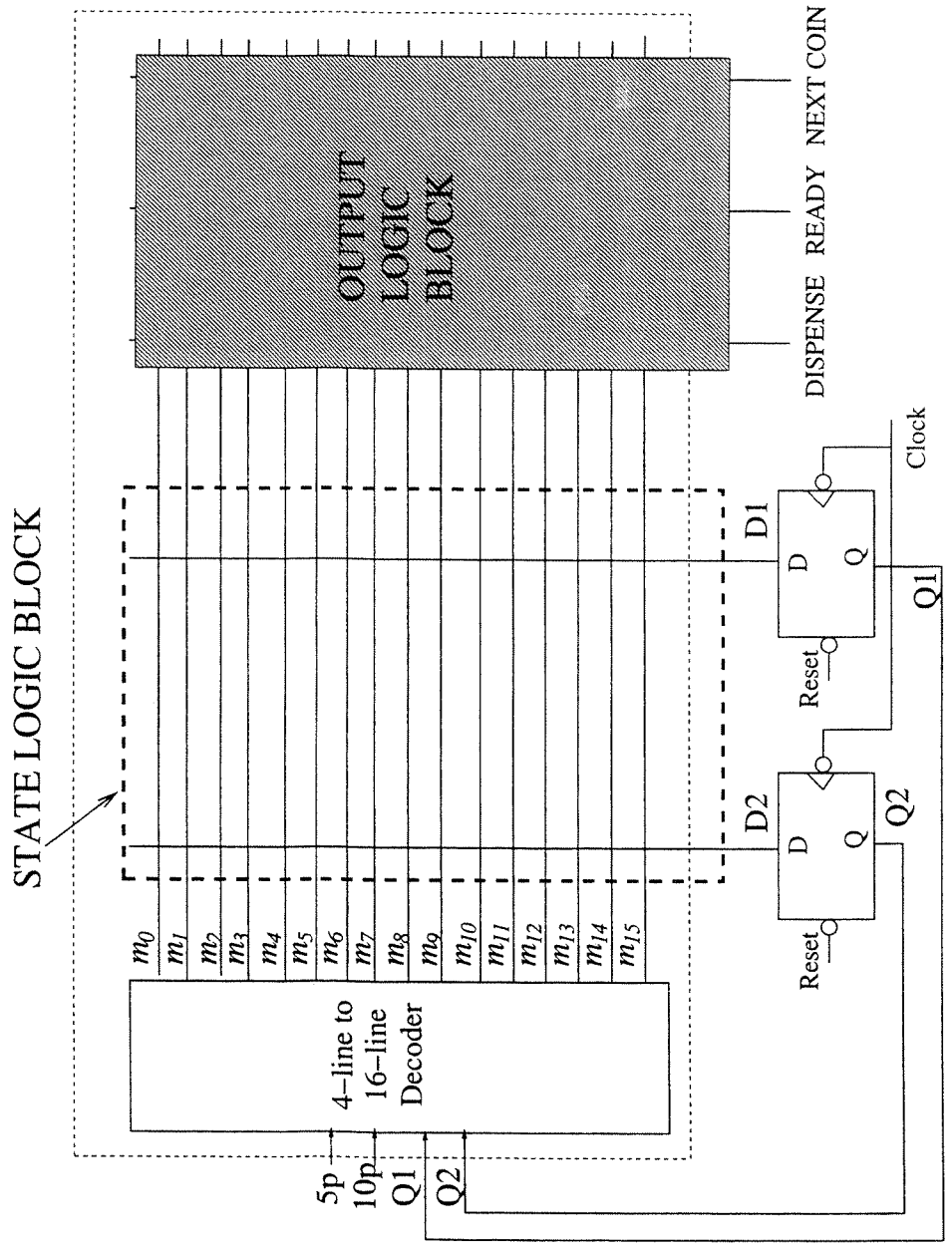


Fig. 1

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3 Figure 2 shows two digital inverter circuits based on MOS transistors. All n-channel transistors have a threshold voltage $V_{Tn}$ of 1 V and process transconductance parameter $k'$ = 10 μA $V^{-2}$. All p-channel devices have a threshold voltage $V_{Tp}$ of -1 V and process transconductance parameter $k'$ = 5 μA $V^{-2}$. In each circuit, the transistor M1 has aspect ratio (W/L) of 2. The transistor M2 has aspect ratio (W/L) of 0.2.

(a) Determine the output voltage $V_O$ for each circuit under the following conditions:

(i) input voltage $V_{IN} = 0$ ; [10%]

(ii) input voltage $V_{IN} = V_{DD}$ . [25%]

(b) Explain carefully how the channel dimensions for transistor M3 should be chosen in order to equalise the delay observed for rising and falling edges applied at the gate input. [15%]

(c) Each gate receives an input signal $V_{IN}$ which switches abruptly from 5 V to 0 V. Assuming the output load capacitance $C_L$ is 10 pF, determine, for the two inverter circuits, the delay between input and output, using the 50% convention for estimation of this delay. [50%]

You may assume the following equations for the drain current $I_D$ flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad \text{for} \quad V_{DS} < (V_{GS} - V_T);$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \quad \text{for} \quad V_{DS} \geq (V_{GS} - V_T)$$

where $k$ is the device transconductance parameter and the other symbols have their usual meaning.

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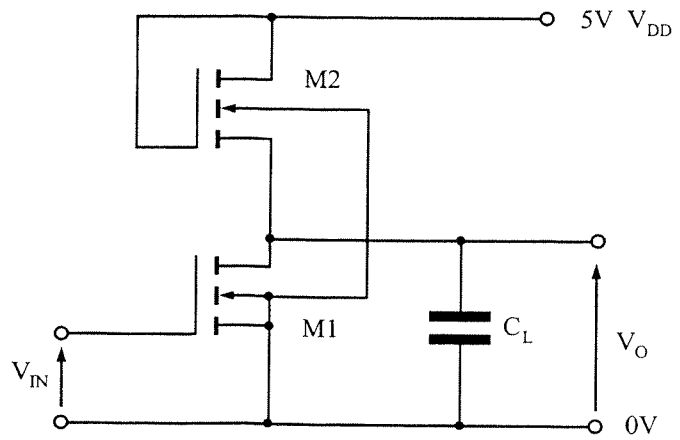


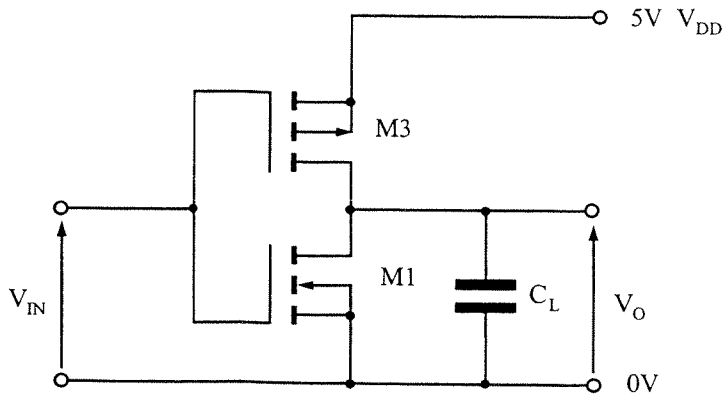


Fig. 2

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4 Sketch a graph depicting a typical voltage transfer characteristic for a Schmitt trigger, and explain the features of the *output high-to-low transition* and *output low-to-high transition*. [20%]

Fig. 3 shows the circuit schematic for a CMOS Schmitt trigger circuit implemented using MOS transistors PI, PO, PF, NI, NO and NF. The six transistors have corresponding device transconductances $k_{PI}$, $k_{PO}$, $k_{PF}$, $k_{NI}$, $k_{NO}$ and $k_{NF}$. You may assume that all three NMOS transistors have threshold voltage $V_{TN}$ and all three PMOS transistors have threshold voltage $V_{TP}$.

(a) Explaining your reasoning carefully, determine the values of $V_{OH}$ and $V_{OL}$ expected at the output with normal logic levels applied at the input. [20%]

(b) Stating any assumptions made, show that the output low-to-high transition will occur when the input voltage reaches the value: [40%]

$$V_{IN} = \frac{\sqrt{\frac{k_{PI}}{k_{PF}}}\,(V_{DD} + V_{TP})}{1 + \sqrt{\frac{k_{PI}}{k_{PF}}}}$$

(c) An efficient CMOS two-input Schmitt NAND gate is required for a communications application. Draw a suitable transistor-level schematic showing how the circuit of Fig. 3 may be used in the implementation of such a gate. [20%]

You may assume the following equations for the drain current $I_D$ flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad \text{for} \quad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \quad \text{for} \quad V_{DS} \geq (V_{GS} - V_T)$$

where $k$ is the device transconductance parameter and the other symbols have their usual meaning.

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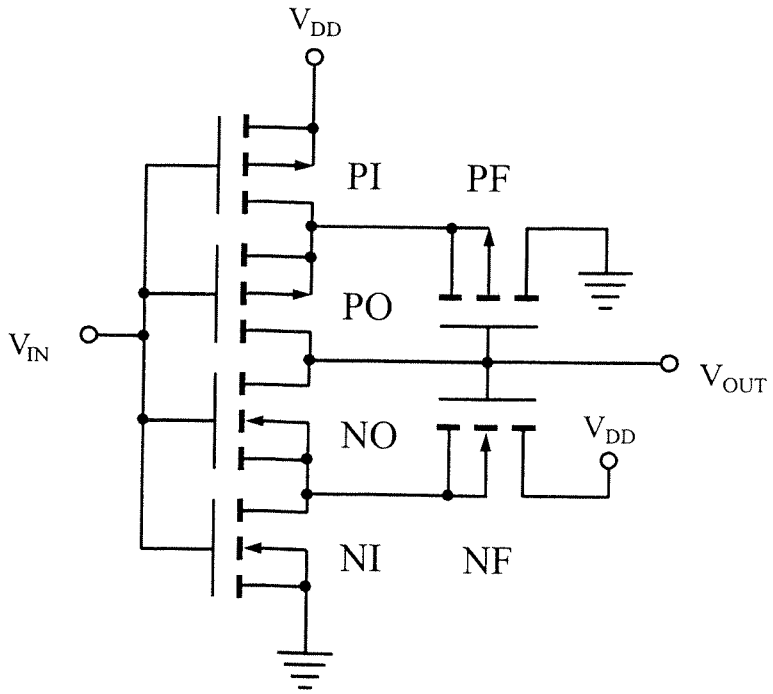


Fig. 3

**END OF PAPER**

**Answers 3B2 – Integrated digital electronics**

1.

(b) $T_A = \overline{A}B\overline{C} + \overline{B}C$

$T_B = A + \overline{B} + C$

$T_C = \overline{A}C + A\overline{C}$

(c) $\overline{R} = \overline{\overline{C}\overline{B}A + C\overline{B}\overline{A} + CBA}$

2.

$D_1 = \sum(2,4,5,6,9,10)$

$D_2 = \sum(1,5,6,8,10)$

3.

(a) (i) Inverter A: for $V_{IN}$=0, $V_{OH}$=4V
Inverter B : for $V_{IN}$=0, $V_{OH}$=5V
(ii) Inverter A: $V_{IN}$=$V_{DD}$, $V_{OL}$=0.19V
Inverter B: $V_{IN}$=$V_{DD}$, $V_{OL}$=0V

(b) $\frac{W_3}{L_3} = 4$

(c) Inverter A: $T_{del} = 2.1\mu s$
Inverter B: Total delay = 52 ns