ENGINEERING TRIPOS PART IIA

Tuesday 6 May 2003 2.30 to 4.00

Module 3F5

COMPUTER AND NETWORK SYSTEMS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1 (a) Describe in detail the main differences between a circuit switch and a packet switch in terms of the requirements of a telecommunications network and a computer data network. [40%]

(b) An X.25 packet switched network has a maximum packet length of 1024 bytes, a window length of 8 packets and a transmission rate of 1 Mbs^{-1} over a 25 km coaxial cable wide area link. The velocity of a pulse in the coaxial cable is 1×10^8 ms^{-1}.

(i) If each packet takes 2 ms to process at the receiving node, and if no errors occur, how long will it take before an acknowledgement is sent? [10%]

(ii) How long would the acknowledgement take if the packets had to experience a delay of 2 ms as they were buffered by a packet switch and there were 4 such packet switches over the wide area link? [10%]

(iii) Under the assumptions of case (ii) above, what would happen if an error occurred while transmitting a packet? [10%]

(c) Explain why such an X.25 wide area link as the one described in part (b) (i) would not be suitable for transmission of voice signals using a protocol such as the Transport Control Protocol / Internet Protocol (TCP/IP). How could the problem be minimized? [30%]

2 (a) What are the three main features of the synchronous digital hierarchy (SDH) which helped to correct the defects in the older plesiochronous digital hierarchy (PDH) used in the first generation of digital telephone networks? Explain why these three features make SDH a far superior telephone network structure. [30%]

(b) Sketch the basic structure of the SDH synchronous transport module or STM-1 frame. Why is this frame structure used in SDH instead of a single linear packet? What is the exact data transmission rate of the STM-1 frame? [30%]

(c) Describe how an ideal SDH wide area network would be constructed across a country such as the United Kingdom and describe each component used to create such a wide area network. Why is such a wide area network topology not possible in reality? [40%]

3 (a) (i) Draw a basic 1-bit Arithmetic Logic Unit (ALU) capable of performing AND, OR, plus and minus. [10%]

(ii) Explain what the SLT ("set if less than") MIPS instruction does, with reference to this example: SLT $r1, $r2, $r3. Add support for SLT to a 32-bit ALU obtained by cascading instances of the above 1-bit ALU. Ignore the problem of overflow during subtraction. [20%]

(iii) Design circuitry to detect overflow during addition or subtraction and show where this fits in the 32-bit ALU. [20%]

(iv) Now improve the design of part (ii) so that it works correctly even if overflow occurs during subtraction. [20%]

(b) Describe how to speed up the operation of a 4-bit adder using carry look-ahead and derive the appropriate equations. [30%]

4 (a) Using the symbols and definitions below, derive Amdahl's law as a formula expressing s_p, the speedup for the whole program, in terms of s_f, the speedup for the feature being improved, and u, the usage ratio of the feature. Perform a basic sanity check of your formula by trying a couple of extreme cases. [20%]

main symbol	t	execution time (seconds)
	s	speedup (dimensionless)
	u	usage (dimensionless)
"what" subscript	p	whole program
	f	feature being improved
	r	rest of program
"when" subscript	o	old
	n	new

$$s_p = \frac{t_{po}}{t_{pn}};\ s_f = \frac{t_{fo}}{t_{fn}};\ u = \frac{t_{fo}}{t_{po}}.$$

(b) On a given computer, a given program takes 30 minutes to run. If one were to make the memory subsystem 5 times faster, the program would take only 10 minutes, for an overall speedup of 3 times. What should the memory speedup be in order to achieve an overall speedup of 4 times? [10%]

(c) The main way to speed up memory access is through caching. Briefly explain how a cache works (covering writes as well as reads) and the principles on which caching is based. Draw a diagram of a cache, naming its parts, and explain the function of each field of a cache entry. [30%]

(d) Explain the differences between direct-mapped, set-associative and fully associative caches, listing advantages and disadvantages for each. [20%]

(e) You must build a 2-way set-associative cache for a computer with a 32-bit address space (in bytes). The available space on the motherboard being designed allows up to 32 sockets for 64 k × 4 bit SRAMs. Using a cache block size of one word (32 bits), what is the net data storage size, in bytes, of the largest cache you can build? Show the breakdown of the address into its cache access components. [20%]

END OF PAPER

3F5

1 (b) (i)

Acks will be sent every 84 ms.

1 (b) (ii)

Acks would be sent every 148 ms.

3 (a) (iii)

Calling a, b the two operands and s the sum of the MSB adder, there is overflow if and only if $ab\bar{s} \vee \bar{a}\bar{b}s$.

3 (a) (iv)

Calling n the sign bit of the MSB ALU, and v the overflow flag, a is less than b if and only if $n\bar{v} \vee \bar{n}v$. This is equivalent to $n \oplus v$.

4 (a)

$$s_p = \frac{1}{1 - u + \frac{u}{s_f}}.$$

4 (b)

The required memory speedup is 10 times.

4 (e)

The depth of the cache is 64 k sets. The number of chips used is 24. The net capacity of the cache is 512 kB.