# ENGINEERING TRIPOS PART IIA 2004

Solutions to Module 3B2
Integrated Digital Electronics
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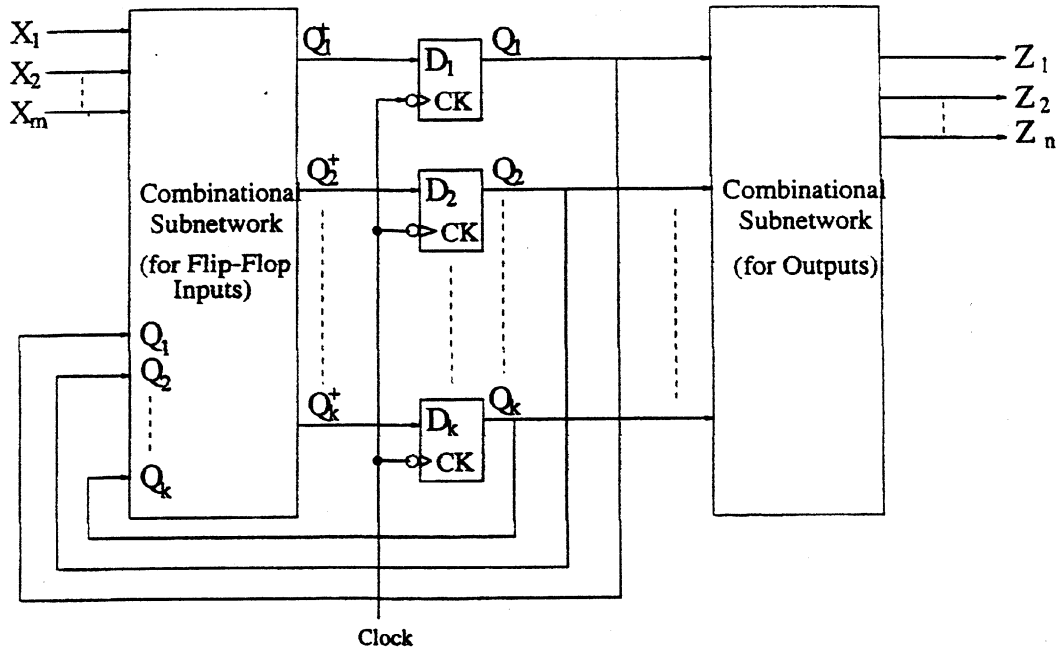
# PART IIA TRIPOS 2004. MODULE 3B2 CRIB.

1. (c) The Moore architecture is shown below:

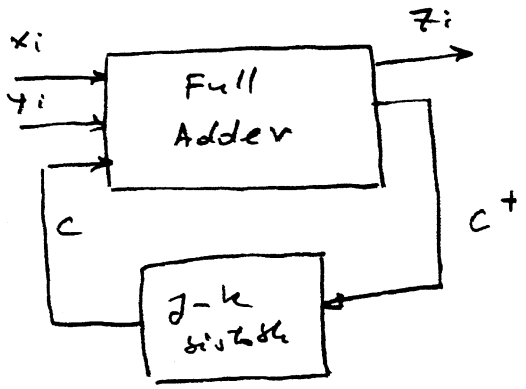



Moore sequential circuit model

$z = f(Q)$ and $Q^+ = f(x, Q)$

- output is only a function of the present state while next state ($Q^+$) is a function of both present state and primary inputs. [20%]

(b)




$c$ = carry bit (present state)

$c^+$ = next carry bit (next state)

| $x_i y_i$ | $c$ | $z_i$ | $c^+$ | $JK$ |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 x |
| 00 | 1 | 1 | 0 | x 1 |
| 01 | 0 | 1 | 0 | 0 x |
| 01 | 1 | 0 | 1 | x 0 |
| 10 | 0 | 1 | 0 | 0 x |
| 10 | 1 | 0 | 1 | x 0 |
| 11 | 0 | 0 | 1 | 1 x |
| 11 | 1 | 1 | 1 | x 0 |

$J$

| $c$ \ $x_i y_i$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 1 | x | x | x | x |

$J = x_i y_i$

$K$

| $c$ \ $x_i y_i$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | x | x | x | x |
| 1 | 1 | 0 | 0 | 0 |

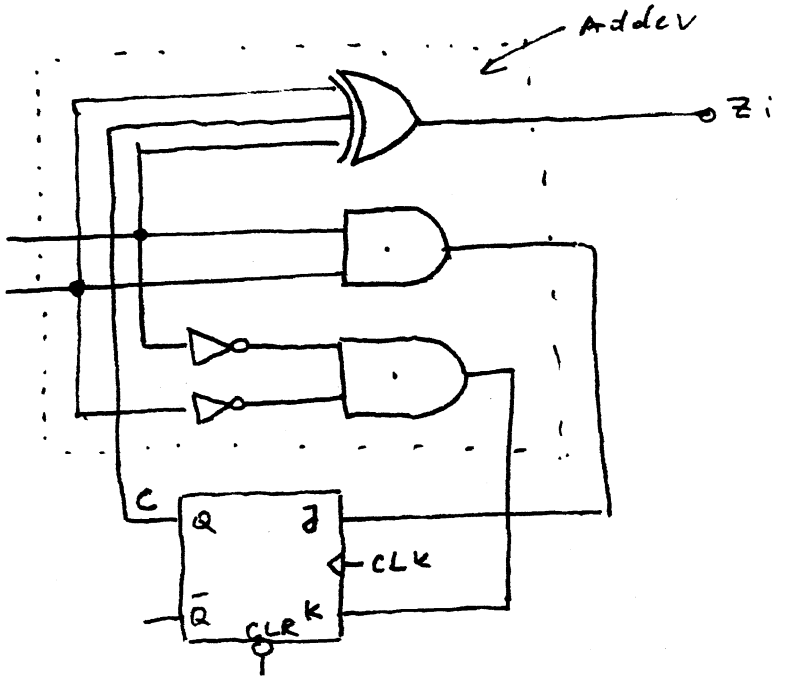
$K = \bar{x}_i \bar{y}_i$

$z_i$

| $c$ \ $x_i y_i$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

$z_i = x_i \oplus y_i \oplus c$

the implementation of the circuit is given below




[50%]

(c) • For 4 bit numbers the sequential adder will require four consecutive clock cycles to perform the 4-bit addition. The combinational ("parallel" or "ripple-carry") adder will perform the addition in a single step which equals to a single clock cycle

• When the number of bits increases (e.g 32 bits) the differences between the two designs becomes more prominent. The parallel adder will require a huge number of components compared to the serial (sequential) adder. [30%]

2. (a)

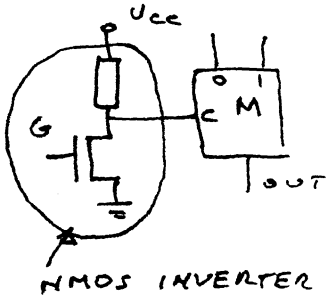
ROMS — AND array is hard-wired (decoder) and the OR array (memory array) is programmable.

PLAs — Both AND & OR arrays are programmable (most versatile but most expensive)

PALs — AND array is programmable and OR array is hard-wired. [20%]

(b) The control circuits connected to M1 & M2 are NMOS inverters.

G = 0 ⇒ C = 1
G = 1 ⇒ C = 0



NMOS INVERTER

• if $G_1 = 1 \Rightarrow C_1 = 0 \Rightarrow I/O_2$ is configured as input $I/O_2 = I$. The input I is selected at the M1 multiplexer and becomes an input in the PAL

In this case the macro-cell behaves as a single output combinational circuit with 3 inputs $x, y, I$. The logic function implemented is:

$$O_1 = \bar{x}\bar{I} + x + \bar{y} = x + \bar{y} + \bar{I}$$

- if $G_1 = 0$ & $G_2 = 1 \Rightarrow C_1 = 1, C_2 = 0$

$B_2$ is inactive and $I/O_2 = O_2$

The bistable is bypassed and the macro-cell behaves as a two output combinational network with two inputs.

$$\begin{cases} O_1 = \bar{x} + x + \bar{y} = 1 \rightarrow \text{remains active all the time} \\ O_2 = xy \end{cases}$$

- if $G_1 = 0$ & $G_2 = 0 \Rightarrow C_1 = 1, C_2 = 1$

$B_1$ & $B_2$ are short circuits, $M_1$ & $M_2$ select the input "1". The cell behaves as a MEALY sequential circuit with two outputs $O_1$ & $O_2$

Using reverse engineering method we work with $Q^+$ & $T$. [50%]

$$\begin{cases} Q^+ = Q & \text{if } T = 0 \\ Q^+ = \bar{Q} & \text{if } T = 1 \end{cases} \Rightarrow$$

$$\Rightarrow Q^+ = Q\bar{T} + \bar{Q}T$$

$$\begin{cases} T = \underline{\underline{\bar{Q}xy}} \\ Q^+ = Q\bar{T} + \bar{Q}T = Q(Q + x\bar{y}) + \bar{Q}xy = \\ \qquad = Q + \bar{Q}xy = \underline{\underline{Q + xy}} \end{cases}$$

$$O_1 = \bar{x}Q + x + \bar{y} = x + Q + \bar{y}$$

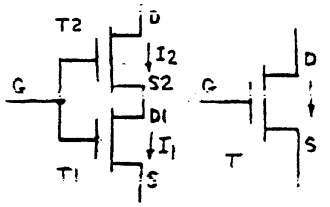
$$O_2 = Q.$$

| $Q$ | $Q^+$ for Input $xy$ = 00 | 01 | 11 | 10 | $O_2O_1$ output for $xy$ = 00 | 01 | 11 | 10 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 01 | 00 | 01 | 01 |
| 1 | 1 | 1 | 1 | 1 | 11 | 11 | 11 | 11 |

[30%]

2 (a)

Assume that all the devices are operating in the non-saturation mode; the circuits to be compared are shown, with identical voltages indicated




For T2, we can write for I2:-

$$I_2 = \frac{K'}{2}\frac{W}{L_2}\left[2(V_{GS_2} - V_T)V_{DS_2} - V_{DS_2}^2\right]$$

Hence $$I_2\frac{2L_2}{K'W} = \left[2(V_{GS_2} - V_T)V_{DS_2} - V_{DS_2}^2\right] \qquad (1)$$

Similarly, for $I_1$ in T1

$$I_1\frac{2L_1}{K'W} = \left[2(V_{GS} - V_T)V_{D,S} - V_{D,S}^2\right] \qquad (2)$$

Note that $V_{GS_2} = V_{GS} - V_{D,S}$ and $V_{DS_2} = V_{DS} - V_{D,S}$. Substitute into (1):

$$I_2\frac{2L_2}{K'W} = \left[2(V_{GS} - V_T - V_{D,S})(V_{DS} - V_{D,S}) - (V_{DS} - V_{D,S})^2\right]$$

$$= \left[2(V_{GS} - V_T)V_{DS} - 2(V_{GS} - V_T)V_{D,S} - 2V_{D,S}V_{DS} + 2V_{D,S}^2 + V_{DS}^2 - 2V_{DS}V_{D,S} + V_{D,S}^2\right]$$

$$= \left[\left(2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right) - \left(2(V_{GS} - V_T)V_{D,S} - V_{D,S}^2\right)\right]$$

By inspection, the second term is equivalent to the RHS of (2). Substituting:-

$$I_2\frac{2L_2}{K'W} = \left[\left(2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right)\right] - I_1\frac{2L_1}{K'W}$$

But $I_2 = I_1 = I$, say. Hence,

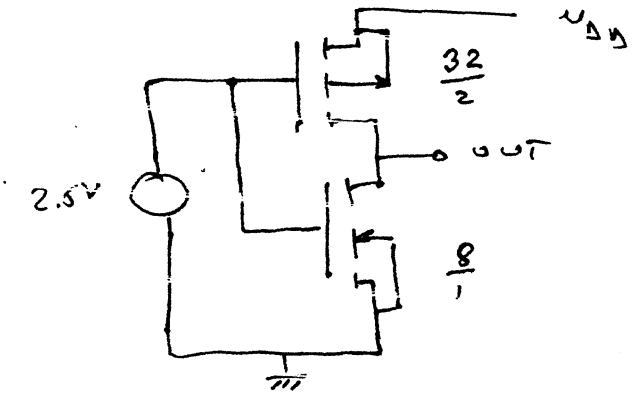
$$\frac{2I(L_2 + L_1)}{K'W} = \left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right], \text{ which gives:-}$$

$$I = \frac{K'}{2}\frac{W}{L_2 + L_1}\left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right]$$

This is the current that would flow in a single device of width W, length $(L_2 + L_1)$, and whose electrode voltages are $V_{GS}$, $V_{DS}$ as shown.

[50%]

3. (S). Using for argument of a → $L = L_1 + L_2$




For p-Type $L_1 + L_2 = L$

$$\Rightarrow k_p = \frac{k'_p W_p}{L_p} = \frac{10 \times 16}{1} = 160\,\mu A/V^2$$

The two n-type are in parallel

$$\Rightarrow k_n = \frac{k'_n \cdot W_n}{L_n} = \frac{20 \times 8}{1} = 160\,\mu A/V^2$$

Hence for symmetry $V_{out} = V_{DD}/2 = 2.5V$

Since for both transistors $V_{DS} > V_{GS} - V_T$

$$\Rightarrow I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2 = 80\,(2.5 - 1)^2 = 180\,\mu A$$ [3 3/4]

(c) The p-devices share a common substrate this must be connected to the most positive potential — $V_{DD}$.

The source-substrate potential for the two p-channel transistors will be different. The lower p-channel will have a greater $V_{SB}$ (source-body voltage) and therefore a lower conductance ($V_T$ is greater). This results in the conductance of the lower n-channel transistors being greater than in the upper p-channel transistors hence $V_{out}$ will be lower than calculated in (S)

[2 3/4]

4(a) Historically, logic circuit development began with bipolar devices operating between saturation and cut-off. Available process technologies encouraged this development in an evolutionary rather than revolutionary way. The only advantage of saturated bipolar technology are:-

- superiority over passive (diode-based) & mechanical logics
- technological simplicity
- suitable for integration and enhancement (by use of schottky diode technology etc)

Disadvantages:

- high device count per function
- high consumption
- low input resistance
- long propagation times
- limited enhancement through scaling (dimension reductions)

Nonetheless, TTL, S/LSTTL, ALSTTL were the primary technology on which much of the emergence of digital computing depended. Fastest logics (ASTTL) could run at c 100 and required a fixed supply of 5V.

The main problem with saturating logic is the undesirable switching delays as devices come out of saturation. This was partly resolved through use of Schottky diodes, but completely circumvented by ECL (current-mode or non-saturating logic).

Advantages:

- very high speed, up to 1GHz in most recent forms
- constant power consumption (approximately) leading to
- good overall noise characteristics

Disadvantages

- very high consumption
- poor suitability for Large scale integration

The excellent drive capability of bipolar technology can be put to good use with MOS gates in the use of Bi-CMOS which has superior performance when driving high current loads. The recent emergence of Ge-doped Si semiconductors is leading towards still greater speed improvements. Up to about 10GHz, are promised by this approach, which is likely to be beyond the limits of MOS technology.

The use of III/V semiconductors eg GaAs in MESFETs has offered propagation delays of < 10ps at room temp. but so far large scale integration has not been possible

4(a) cont'd The breakthrough that facilitated the full development of MOS technology was the introduction of ion implantation which facilitated accurate positioning of n dopants in p substrate & vice versa. This gave the necessary impetus for the rapid development of CMOS.

The main reasons for popularity (advantages) of CMOS:-
- Very low consumption for LF applications
- Very good noise immunity (theoretically up to 0.4 $V_{DD}$)
- Fully restored logic outputs (0V & $V_{DD}$)
- Operable over wide range of supply voltages
- Gate inputs are open circuit, easy to drive
- Highly suited to integration → VLSI, ULSI
- Scales well (consumption/speed improve as devices shrunk)

Hence ideal for portable, battery powered instrumentation.
- Very good packing density

Disadvantages:-
- Comparatively poor output drive capability
- Not as fast as the best bipolar forms (for significant loads)
- Sensitivity to static breakdown
- Liability to destructive latch-up (poor circuit design or peripheral failures)

The incorporation of bipolar output devices has led to improved output drive capability for large capacitance loads.

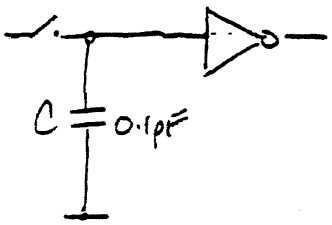
With CMOS, the dominant mode of power dissipation is dynamic dissipation. Straightforward approaches to logic involve multiple devices and significant capacitances, so much effort has gone into development of circuit abstractions (eg clocked logic, domino logic) which reduce the device count, & hence the capacitance & delay.

It is practicable, and often the case, that technologies may be mixed to give the best combination of properties, though this may pose considerable challenges for the designer.

[50%]

4(b) MOS technologies offer great flexibility, low consumption, high speed, excellent scalability and ability to integrate complex support functions. Bipolar technologies offer only speed as a significant advantage, and dimensionally scaled MOS technologies have surpassed bipolar devices even in these areas.

[10%]




Assume the inverter switches at $V_{sw} = V_{DD}/2$. That is, 2.5v.

If C loses half its charge having been set to logic 1, it will incorrectly represent logic 0.

Leakage occurs at a fixed rate, 0.1nA.

Hence the time taken to discharge to 2.5V is:-

$$C \times (5 - V_{sw}) / I_{leak} = \frac{0.2 \times 10^{-12} \times (5 - 2.5)}{0.1 \times 10^{-9}}$$

$$= 5mS$$

Hence the capacitor must be refreshed more often than this

If refresh IS performed at 5mS intervals and uses one clock cycle, the proportion lost at fck = 1MHz is:-

$$\frac{1 / 5 \times 10^{-3}}{10^6} = \frac{200}{10^6} = \frac{1}{5000}$$

ie 1 cycle in 5000 lost owing to need to refresh

[40%]