UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIA

Friday 7 May 2004 2.30pm -4pm

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

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1. (a) Draw and describe briefly the architecture of a Moore sequential circuit. [20%]

(b) The circuit shown in Fig.1 adds two binary numbers. The numbers are fed to the adder serially starting with the least significant bit, at the input X_i and Y_i. The sum Z_i appears in a serial form at the output while the carry bit is fed back through a bistable to the input. Implement the circuit using a J-K bistable and logic gates. State any assumptions made. [50%]

(c) Compare the operation and performance of the sequential adder shown in Fig. 1 with those of a combinational ('parallel') adder that would perform a similar function. [30%]

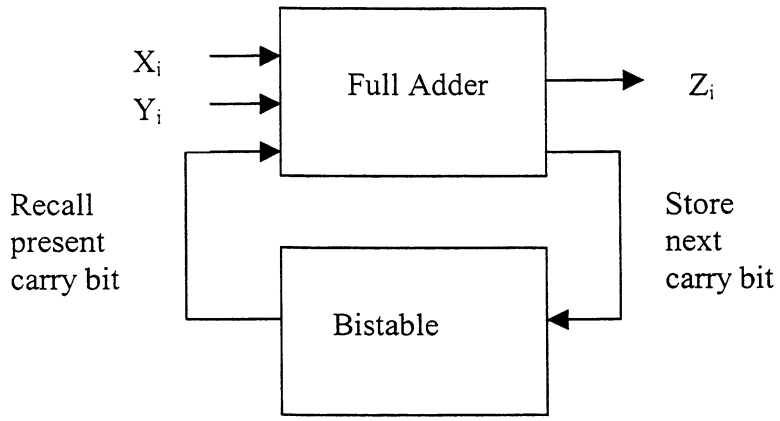

Fig. 1

2. (a) State the main differences between a Programmable Logic Array (PLA), a Programmable Array Logic (PAL) and a Read Only Memory (ROM) . [20%]

(b) A macro-cell, part of a complex combinational/sequential PAL has been programmed as shown in Fig. 2. The binary gate signals on the two n-channel MOSFET switches, G1 and G2, control the 2-1 multiplexers and the non-inverting tri-state buffers B1 and B2. The tri-state buffers act as a short-circuit when the control is 'high' and an open-circuit when the control is 'low'. There are two main inputs labelled X and Y and one output labelled O1. The I/O2 pin can be configured as either an extra input or the second output of the macro-cell.

Note that the bistable is of 'toggle' type (T).

Describe the multiple operation of the macro-cell and find the logic functions for all combinations of the gate signals G1 and G2. [50%]

Derive the state table if the macro-cell is operated as a state-machine. [30%]

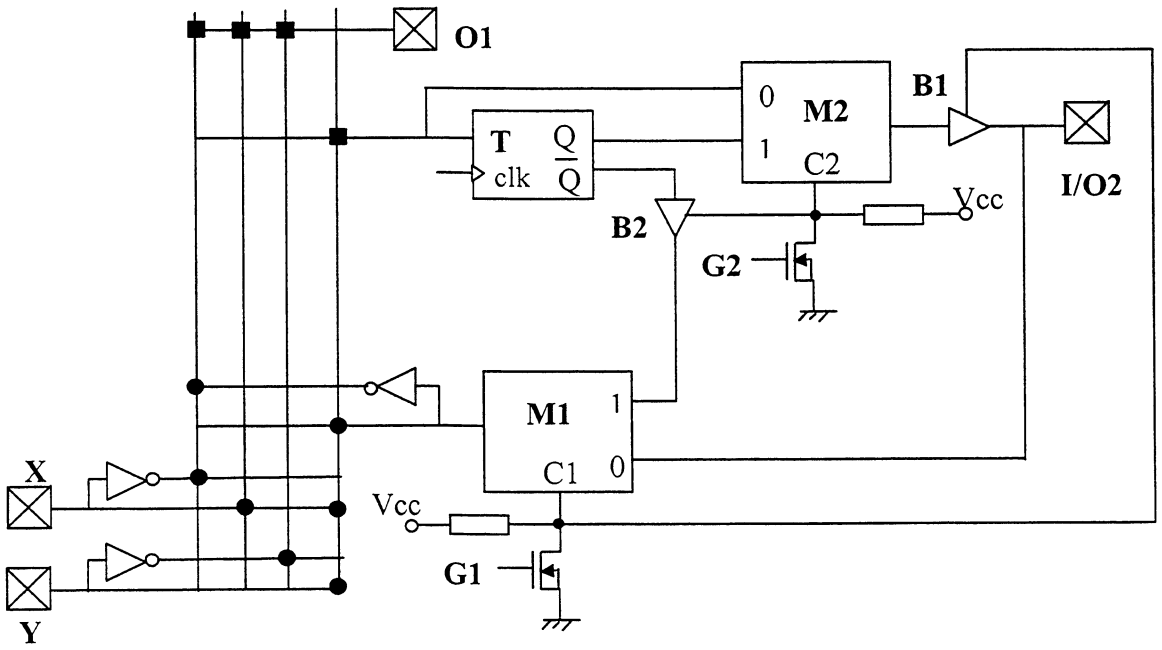

Fig. 2

3. (a) Two MOS transistors with channel lengths *L1* and *L2* and equal channel widths *W* are connected in series and have their terminals connected as shown in Fig. 3 (a). Neglecting the body effect, show that in this configuration the two transistors acting together have a current-voltage characteristic that is the same as that of a single transistor with a channel length equal to *L1* + *L2*. State any other assumptions made. [50%]

(b) Fig. 3 (b) shows a two-input NOR gate implemented as a CMOS circuit using MOS transistors with channel dimensions *W/L* as indicated. Determine the supply current drawn if inputs A and B are linked together and connected to a supply of 2.5 V. Take $V_{DD} = 5$ V, $V_{TN} = 1$ V, $V_{TP} = -1$ V and $k = k'\,W/L$, with $k'_N = 20\ \mu A/V^2$ and $k'_P = 10\ \mu A/V^2$. [30%]

(c) In practical implementations of the circuit shown in Fig. 3(b), the series connected p-channel devices share a common substrate connection. Explain qualitatively how this would be expected to affect the result calculated in part (b). [20%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad \text{for} \quad V_{DS} < (V_{GS} - V_T);$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \quad \text{for} \quad V_{DS} \geq (V_{GS} - V_T)$$

where k is the device transconductance parameter and the other symbols have their usual meaning.

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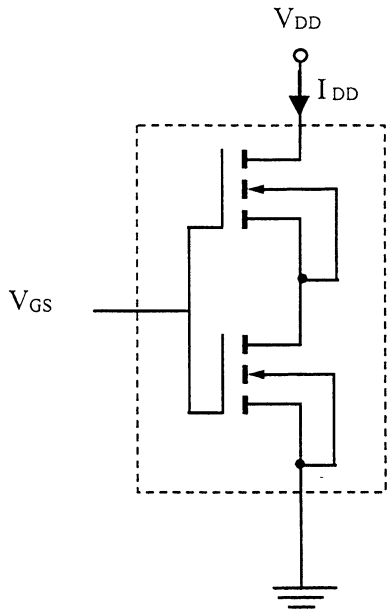

Fig. 3 (a)

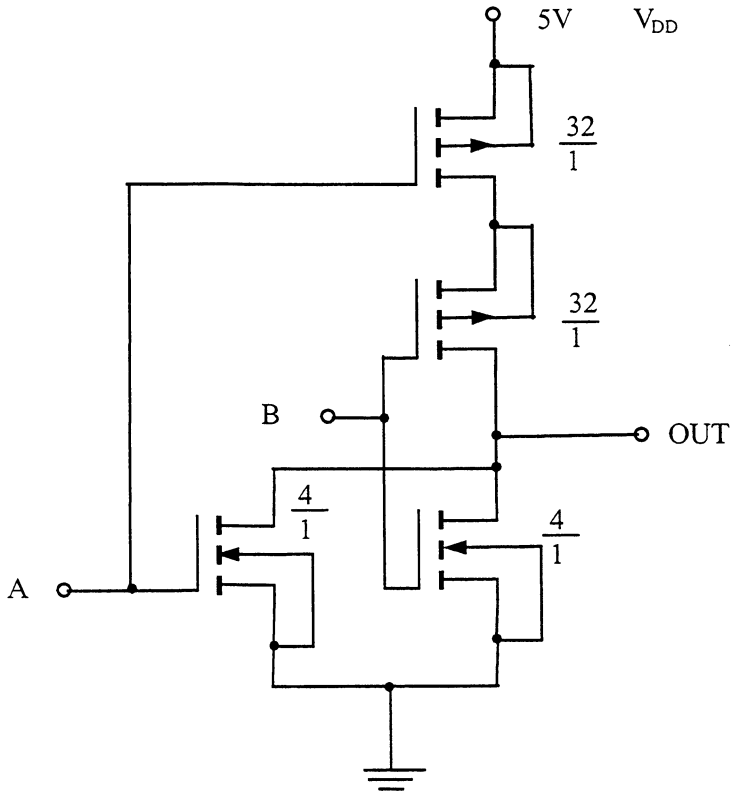

Fig. 3 (b)

4. (a) Discuss the advantages and disadvantages of the major digital logic families based on emitter-coupled logic, CMOS and BiCMOS. In your account indicate briefly under what circumstances each family can provide desirable properties. Why is CMOS currently regarded as the most popular technology? [50%]

(b) Discuss briefly why the vast majority of read-write memory devices available today are based on MOS rather than bipolar technologies. [10%]

(c) A dynamic read-write memory cell is modelled as a switch *S*, a storage capacitor *C* and an inverter as shown in Fig. 4. The storage capacitor has a capacitance of 0.2 pF and is charged to 5 V to represent logic 1. Logic 0 is represented by 0 V. If the leakage current due to the switch and other parasitics is constant at 0.1 nA, how often must the cell be refreshed ? State any assumptions made.

If access to the memory is controlled by a 1 MHz clock, estimate the proportion of clock cycles lost through the need to refresh. [40%]

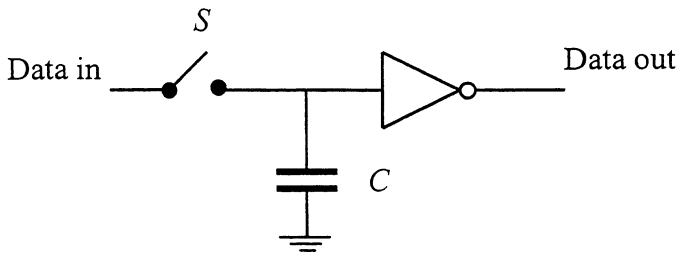

Fig. 4

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