CRIB

PART IIA 2005
3B2: Integrated digital electronics
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*Datasheet: None*

1. (a) The Quine-McClusky tabular method is based on building lists with adjacent blocks containing the same number of 'High' variables. By comparing, and if appropriate, combining each term from one block with the block below we build subsequent lists . The terms that did not combine in each list (including the last) are termed 'Prime Implicants' (PIs). The 'Prime Implicant table' is formed of the PIs and the original terms of the logic function. The idea is to select the minimal and the simplest PIs which cover all the original terms. This can be done by visual inspection or by a formalised method.

If the logic function is not in a canonical form (or not brought to a canonical form) it is difficult to deal with terms that have fewer variables. Such terms may be introduced in the second or subsequent lists but this results in missing the chance to combine parts of them (canonical components of such terms) with other terms from the first list (or previous lists) and thus . the method does not always deliver an optimal solution. [30%]

(b) By using the reverse engineering method from Fig 1 we can obtain:

$J_0 = Q_2Q_1 + \overline{Q_2}\,\overline{Q_1}$
$K_0 = Q_2\overline{Q_1} + \overline{Q_2}Q_1$
$J_1 = \overline{Q_2}Q_0$
$K_1 = Q_2Q_0$
$J_2 = Q_1\overline{Q_0}$
$K_2 = \overline{Q_1}\,\overline{Q_0}$

In a J-K bistable the next state $Q^+$ function of the present state Q is given by :
$Q^+ = J\overline{Q} + \overline{K}Q$
Thus we can calculate the next states $Q_0^+$, $Q_1^+$, $Q_2^+$

$Q_0^+ = Q_2Q_1 + \overline{Q_2}\overline{Q}1$
$Q_1^+ = \overline{Q_2}\overline{Q_1}Q_0 + \overline{Q_2}Q_1 + \overline{Q_0}Q_1$
$Q_2^+ = Q_1\overline{Q_0}\overline{Q_2} + Q_1Q_2 + Q_0Q_2$

The k-maps obtained from the expressions above will help to build the state table:

$Q_0^+$

| $Q_2 Q_1$ \ $Q_0$ | 0 | 1 |
|---|---|---|
| 00 | 1 | 1 |
| 01 | 0 | 0 |
| 11 | 1 | 1 |
| 10 | 0 | 0 |

$Q_1^+$

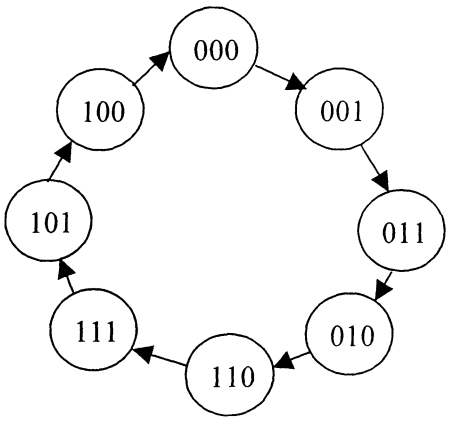
| $Q_2 Q_1$ \ $Q_0$ | 0 | 1 |
|---|---|---|
| 00 | 0 | 1 |
| 01 | 1 | 1 |
| 11 | 1 | 0 |
| 10 | 0 | 0 |

$Q_2^+$

| $Q_2 Q_1$ \ $Q_0$ | 0 | 1 |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 1 | 0 |
| 11 | 1 | 1 |
| 10 | 0 | 1 |

From these K-maps we can build the state table and the state diagram. Since this is a counter (there are no inputs) it makes sense to write the states in the counting sequence:

| Present state | Next state |
|---|---|
| 000 | 001 |
| 001 | 011 |
| 011 | 010 |
| 010 | 110 |
| 110 | 111 |
| 111 | 101 |
| 101 | 100 |
| 100 | 000 |
| 000 | |




[50%]

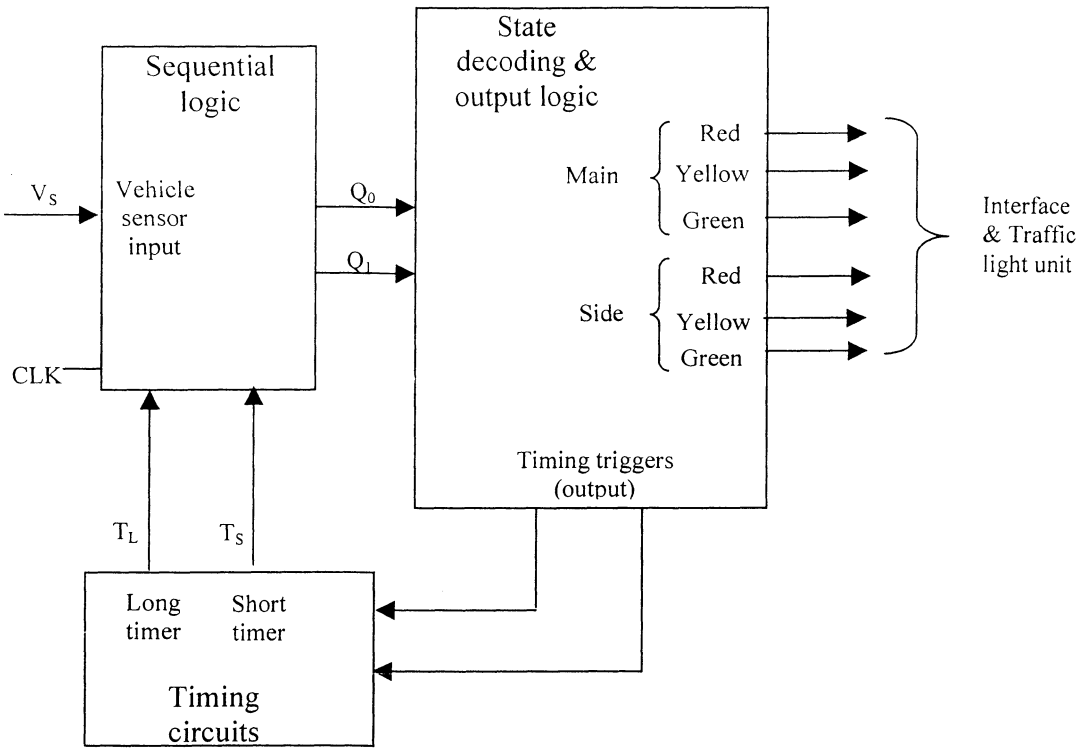
One can see that from the one state to another only one bit changes at a time. This is therefore a 3-bit Gray code counter ! [20%]

2. (a) The design rules to implement a combinational circuit free of static or dynamic hazards using only NOR gates are:

(i) All the adjacent terms in the K-map of the complement of the function should be covered by a common 0-term

(ii) There should be no 0-terms that contain both a variable and its complement. [20%]

(b) The block diagram is shown below (other schematic variants can also be correct):



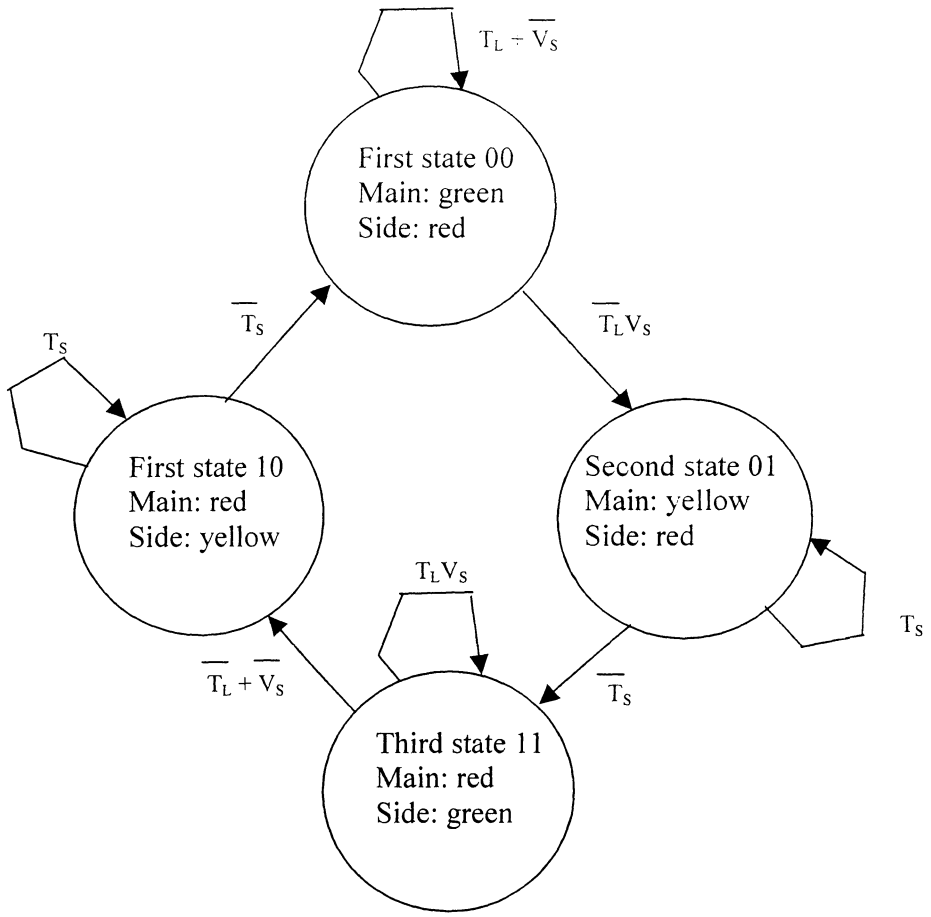

[20%]

**First state.** The Gray code for this state is 00. The main street light is green and the side street light is red. The system remains in this state for at least 25 seconds when $T_L$ is 1 or as long as there is no vehicle on the side road, $V_s$=0. The system goes to the next state when the 25 s timer is off ($T_L$ becomes 0) and there is a vehicle on the side street ($V_s$=1).

**Second state**: Gray code is 01. The main street light is yellow and the side street is red. The system remains in this state for 4 seconds when the short timer is on ($T_s$ is 1) and goes to the next state when $T_s$ becomes 0 (after 4seconds – counted by the timing circuit).

**Third state:** Gray code is 11. The main street light is red and the side street light is green. The system remains in this state when $T_L$ is 1 and there is a vehicle on the side road, $V_s$=1. The system goes to the next state when the 25 s timer is off ($T_L$ becomes 0) or there is no vehicle on the side street ($V_s$=0), whichever comes first.

**Fourth state**: Gray code is 10. The main street light is red and the side street is yellow. The system remains in this state for 4 seconds when the short timer is on ($T_s$ is 1) and goes to the first state when $T_s$ becomes 0 (after 4seconds – counted by the timing circuit).




[30%]

| Present state | Light outputs | | | | | | Trigger outputs | |
|---|---|---|---|---|---|---|---|---|
| | MR | MY | MG | SR | SY | SG | Long | Short |
| 00 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 01 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 10 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 11 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

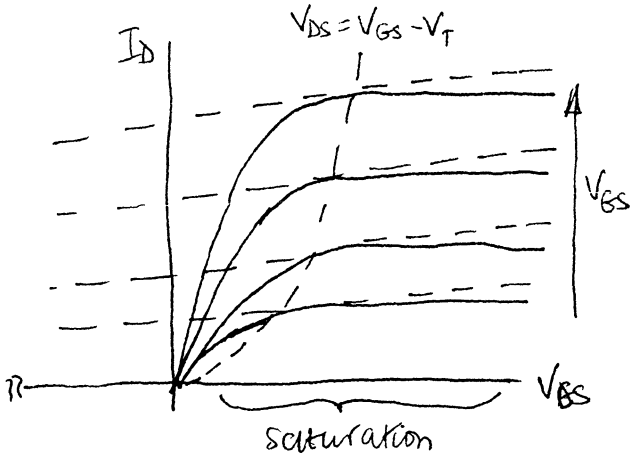
[30%]

3B2 2005 Qn 3

a) (i) For MOS transistors saturation describes the region of operation where the channel is pinched off near the drain. This typically corresponds to high values of $V_{DS}$.
The necessary condition is (for n-channel)

$$V_{DS} > V_{GS} - V_T$$

If $V_{DS} = V_{GS} - V_T$, pinch-off happens right at the drain. As $V_{DS}$ increases, the pinch-off region advances progressively towards the source. To a first approximation $I_D$ remains unchanged as $V_{DS}$ increases, and the device acts as a constant current source/sink. A MOSFET biased so its gate is marginally above $V_T$ and with high $V_{DS}$ will therefore be in the saturation region.
In fact, as $V_{DS}$ increases the resultant shortening of the channel (channel length modulation) slightly enhances the conductance and there is a gradual increase in $I_D$




The near-constant current is a useful characteristic in linear circuits.
Also, a FET connected with D & G shorted is by definition in saturation, and may be used as a load in place of a resistor - it also occupies less space

(ii) For bipolar devices saturation is observed when the base potential $V_{BE}$ causes a large collector current to flow. Assuming a load is connected between collector & supply $V_{CE}$ falls to a low limiting value $V_{CEsat}$ (typically ~0.2 V) and is less than $V_{BE}$ (typically about 0.8 V)
In this saturation $V_{CB} < 0$ (NPN), and the C-B junction becomes forward biased, and the collector injects electronic charge into the base, accounting for some excess base current.
In bipolar, saturation gives a clearly defined low $V_{CE}$ with a typically high $V_{BE}$ and $I_B$, and a large $I_E$. The low $V_{CE}$ can be used to define a logic level (as in saturated mode logic)
The excess charge stored in the base has to be removed before the device can leave saturation & stop conducting. This takes ~(50ns) & limits switching speed available with saturated mode logic.

3B2 2005 Qn3 (cont)

b) In this cct, for T2 $V_{DS} \equiv V_{GS}$ since D shorted to G
Hence $V_{DS} > V_{GS} - V_T$ so T2 is in saturation by definition.
We cannot know for certain the state of T1 since $V_{OUT}$ is unknown, but we will assume that, because $V_{GS}$ is high $V_{DS}$ will likely be low with the device in its non-saturation region.
We must verify this at the end.
Hence use 1st equation for T1, 2nd eqn for T2.
Assuming no current drawn from output, equate $I_D$ for T1 + T2.

$$I_D = \frac{K_1}{2}\left(2(V_{GS_1} - V_T)V_{OUT} - V_{OUT}^2\right) = I_{D_2} = \frac{K_2}{2}(V_{GS_2} - V_T)^2$$

For T1, $V_{GS_1} = 5V$. For T2 $V_{GS_2} = V_{DD} - V_{OUT} = 10 - V_{OUT}$

$$\frac{80}{2}\left(2(5-1)V_{OUT} - V_{OUT}^2\right) = \frac{15}{2}(10 - V_{OUT} - 1)^2$$

$$128V_{OUT} - 16V_{OUT}^2 = 243 - 54V_{OUT} + 3V_{OUT}^2$$

$$19V_{OUT}^2 - 182V_{OUT} + 243 = 0 \qquad \text{Solving,}$$

$$V_{OUT} = \frac{182 \pm \sqrt{182^2 - 4\times19\times243}}{38} \qquad \text{Hence } V_{OUT} = 4.79 \pm 3.18$$

$= 1.61$ or ~~7.97~~ V  The second root is not consistent with T1 in non-saturation ($V_{OUT} < 4V$). Hence first root applies

$\rightarrow$ $\underline{V_{OUT} = 1.61\ V}$

c) $\sigma$ describes the degree of saturation of the bipolar circuit.
$\sigma = 1$ means the circuit is not saturated; $\sigma = 0.1 \equiv$ heavily sat.

$\sigma$ is defined as $I_C/h_{FE}I_B$. If $\sigma = 0.2$, the base current drive is 5× that required to sustain collector current $I_C$, and the circuit is well into saturation so $V_{CE}$ may be taken as $V_{CEsat}$

Hence $I_C = \frac{V_{CC} - 0.1}{R_L} = \frac{4.9}{3000} = 1.63mA$

And $I_B = I_C/\sigma h_{FE} = 1.63\times10^{-3}/0.2\times50 = 163\mu A$

If $V_{BEsat} = 0.7V$, apply KVL to get $V_B$, which is given by

$V_B = I_B R_B + V_{BEsat} = 163\times10^{-6}\times5000 + 0.7 = \underline{1.52\ V}$

3B2 2005 Qn 4

a) Logic swing is 1.2V, symmetric about $V_R = -1.5$

$V_{OH} = V_R + \frac{1}{2} \times 1.2 = -1.5 + 0.6 = -0.9V$
$V_{OL} = V_R - \frac{1}{2} \times 1.2 = -1.5 - 0.6 = -2.1V$

and $V_{OH} - V_{OL} = 1.2$ as required.

The max. available $I_E$ should be used when possible to maximise switching speed so take $I_E = 5mA$. When input A is high (-0.9 V),

$V_{E1} = V_{OH} - V_{BE1} - V_{EE}$ and

$R_E = (V_{OH} - V_{BE1} - V_{EE})/I_{E1} = (-0.9 - 0.8 + 6)/5\times10^{-3} = 860\Omega$

We must choose $R_1$ so the NOR o/p is at $V_{OL} = -2.1V$ when $T_3$ on and $I_{E1} = 5mA$ also

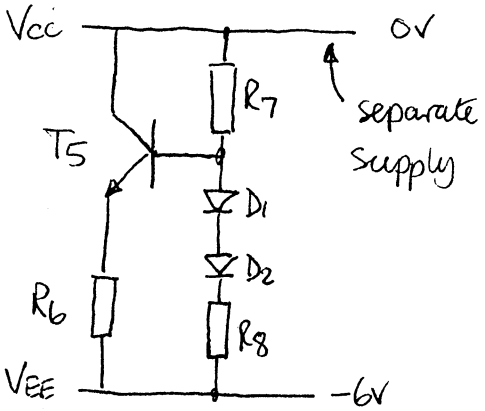
$R_1 = V_{CC} - (V_{CC} + V_{BE3})/I_{E1} = (0 + 2.1 - 0.8)/5\times10^{-3} = 260\Omega$

$R_2$ is not just the same as $R_1$, since $V_R$ is held fixed at -1.5V Choose it so the OR output is at $V_{OL} = -2.1$ when A is low.

$I_{E2} = (V_R - V_{BE2} - V_{EE})/R_E = (-1.5 - 0.8 + 6)/860 = 3.7/0.86 = 4.2m$ (which is 5mA as required)

Hence $R_2 = (V_{CC} - (V_{OL} + V_{BE4}))/I_{E2} = (0 + 2.1 - 0.8)/4.2\times10^{-3} = 309\Omega$

b) Typical circuit



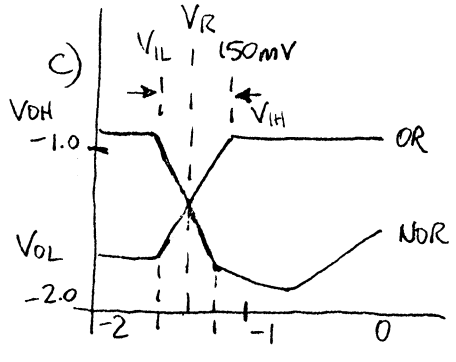

$R_7, R_8, D_1, D_2$ are a potential divider to set $V_{B5}$ to $(-1.5 + 0.8)V$

$D_1, D_2$ enhance temperature stability

$T_5$ is an emitter follower: choose $R_6$ for acceptable reference current, few mA

$V_{B5} \sim V_{CC} - (V_{CC} - 2V_{diode} - V_E)\, R_7/(R_7 + R_8)$

c)




$V_{IH} = -1.5V + 150/2 mV = -1.425V$
$V_{IL} = -1.5 - 150/2 mV = -1.575V$

$NM_H = V_{OH} - V_{IH} = -0.9 + 1.425 = 0.525V$
$NM_L = V_{IL} - V_{OL} = -1.575 + 2.1 = 0.525$

3B2 2005 Qn 4 (cont)

d) If $\beta_{T4} = 50$ then $I_{B4} = I_{E4}/51$. $I_{B4}$ flows thru $R_2$ and slightly reduces $V_{B4}$ and hence $V_{OH}$, so eroding the NM. If the gate does not drive other gates:

$$I_{E4} = (V_{OH} - V_{EE})/R_4 = (-0.9+6)/50\times10^3 \sim 102\mu A$$

Hence $I_{B4} = 102/51 = 2\mu A$.

This extra current which flows thru $R_2$, will increase the voltage drop across this component by $2\times10^{-6}\times309 \sim 600\mu V$ hence reducing $V_{OH}$ to $-0.90006$ V. The difference is quite negligible.

e) Each driven stage consumes a small amount of current from the output of the driving stage. The greater the current, the greater the fall in drive voltage, until the noise margin drops to an unacceptable level.

The noise margin can drop by 525/10 mV owing to loading. We do not know how much current each subsequent gate requires at its input, so estimate. If the gates are of the same family with $I_E \sim 5mA$ and $\beta \sim 50$, then the required base current is $\sim 100\mu A$.

Owing to the emitter follower $T_4$ (and $T_3$) the increase in base current $I_{B4}$ due to each additional driven input is about $100\times10^{-6}\times R_2/51$. Taking worst case, $R_2 = 309\Omega$, $\Delta V_{OH} \simeq 620\mu V$.

If a reduction of 52 mV is allowable, this corresponds to >80 driven gates

In practice the capacitance of driven gate inputs will limit the switching times achievable, and the fanout should probably not be allowed to exceed 10.

Draft Examiner's report for qns 3 & 4

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Question 3, on saturation in MOS and bipolar transistor circuits, was attempted by 59 candidates. Most were able to solve the problems involving MOS and bipolar devices, but some appeared unaware of the different meaning of saturation in the two families. There was some evidence of candidates treating this as their final question and committing insufficient time to it. The mean mark was 54.4%.

Question 4, on emitter-coupled logic, was attempted by 24 candidates. Most were able to calculate plausible resistance values, but not all were able to describe a voltage reference or estimate the fanout. Some candidates clearly treated this as their final question and had insufficient time. The mean mark was 51.0%.