UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIA

Friday 13 May 2005 2.30pm -4pm

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1. (a) In the Quine-McClusky tabular method give the definition of 'prime implicants' and briefly explain the use of the 'prime implicant table' . Explain why if a logic expression is not in a canonical form, or is not brought to a canonical form, the Quine-McClusky tabular method may not always give an optimally simplified solution. [30%]

(b) By using the reverse engineering method analyse the logic circuit shown in Fig.1. Derive the state table and the state diagram. [50%]

What specific function does the circuit perform ? [20%]

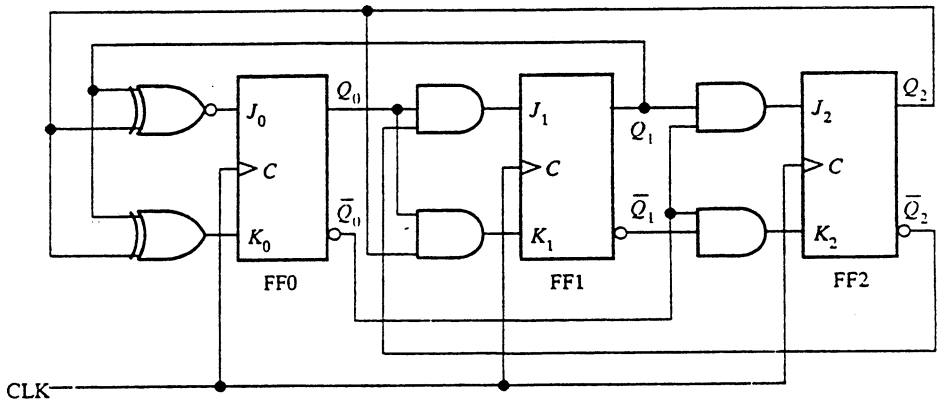


Fig. 1

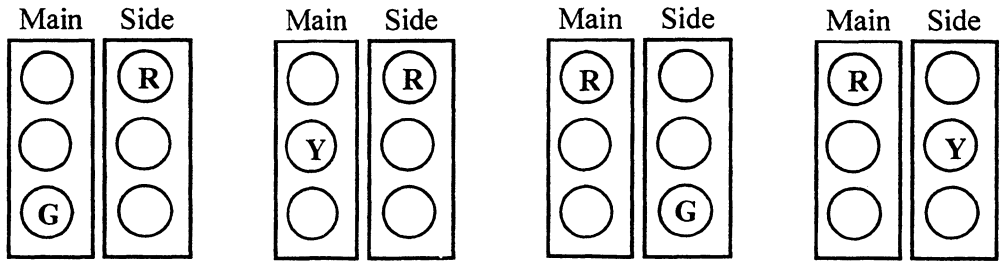
2. (a) State the design rules to implement a combinational circuit free of static or dynamic hazards using only NOR gates. [20%]

(b) A logic controller is required to control a traffic light at the crossroad of a busy main street and an occasionally used side street. The main street is to have a green light for a minimum of 25 seconds or as long as there is no vehicle on the side street. The side street is to have a green light until there is no vehicle on the side street or for a maximum of 25 seconds. There is to be a 4 seconds caution light (yellow) between changes from green to red on both the main street and the side street. These requirements are illustrated in Fig. 2 where R=Red, Y=Yellow and G = Green.

(i) Develop a schematic block diagram of the system indicating the logic blocks, the timing circuit block and the inputs and outputs. [20%]

(ii) Describe the state diagram using Grey coding for a Moore architecture. [30%]

(iii) Derive the output table. There is no need to develop or show the actual circuit implementation. [30%]



First state: 25 s minimum or as long as there is no vehicle on side street

Second state: 4 s

Third state: 25 s maximum or until there is no vehicle on side street

Fourth state: 4 s

Fig. 2

3. (a) Describe what is meant by the term *saturation* when it refers to:

(i) MOS transistors;

(ii) bipolar transistors

in the context of logic gates made from these devices. Your answer should clearly indicate instances where saturation can be used to advantage in the design of logic gates, and indicate where it could be disadvantageous. [30%]

(b) Fig. 3a shows a logic gate based on MOS transistors T_1 and T_2 whose device transconductances k_1 and k_2 are shown.

Calculate the logic 'low' output voltage V_{OL} for this gate assuming the threshold voltage for both transistors V_T = 1 V, and V_I = 5 V when $V_{OUT} = V_{OL}$. Indicate clearly which device, if any, is in its saturation mode. [40%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad \text{for} \quad V_{DS} < (V_{GS} - V_T);$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \quad \text{for} \quad V_{DS} \geq (V_{GS} - V_T)$$

where k is the device transconductance parameter and the other symbols have their usual meaning.

(c) For the bipolar transistor inverter circuit shown in Fig. 3b, the value of σ is 0.2. Explain the significance of this value. If the values of $V_{CE\,sat}$ and $V_{BE\,sat}$ for the device are 0.1 V and 0.7 V respectively, calculate for this circuit the input voltage V_B which would produce this value of σ. [30%]

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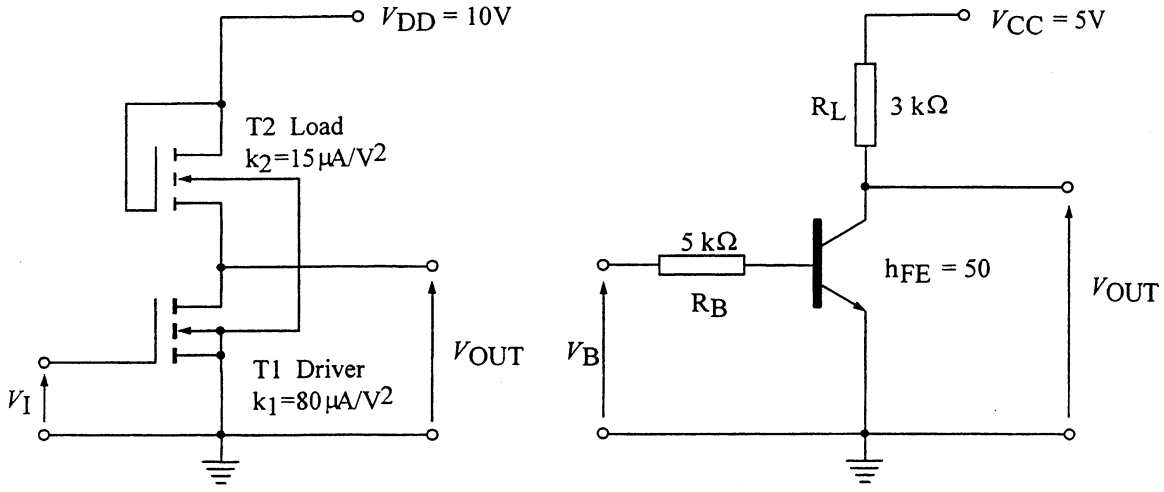
V_{DD} = 10V
T2 Load
k_2=15 μA/V2
V_{OUT}
V_I
T1 Driver
k_1=80 μA/V2
V_{CC} = 5V
R_L
3 kΩ
5 kΩ
R_B
h_{FE} = 50
V_{OUT}
V_B

(a) (b)

Fig. 3

4. The circuit shown in Fig. 4 represents a form of emitter-coupled logic gate in which V_{CC} = 0 V, V_{EE} = −6 V, V_R = −1.5 V. The logic output swing is required to be 1.2 V symmetrical around the reference voltage, V_R. For all transistors, $V_{BE(on)}$ = 0.8 V, and the emitter current of any device must not exceed 5 mA.

(a) Calculate the values of *R1*, *R2* and R_E such that the logic levels for the circuit are consistent for input and output. You may assume that all base currents are negligibly low for the purposes of this calculation. [20%]

(b) Sketch a suitable circuit to generate the reference voltage V_R (component values are not required), and state briefly how it works. [20%]

(c) Determine the noise margins NM_H and NM_L. To estimate V_{IH} and V_{IL} you may assume that the width of the transition region of the voltage transfer characteristic is 150 mV, symmetrically placed around V_R. [10%]

(d) By how much will the output voltage at the OR terminal change owing to the base current drawn by T4 if the current gain, β, of T4 is 50 ? [20%]

(e) Determine the maximum fan-out of the circuit assuming that it is limited by the reduction in the high level noise margin, NM_H, because of loading by the driven gates. Assume that a 10% reduction in NM_H can be tolerated. Explain why the calculated fan-out is unlikely to be realised in practice. [30%]

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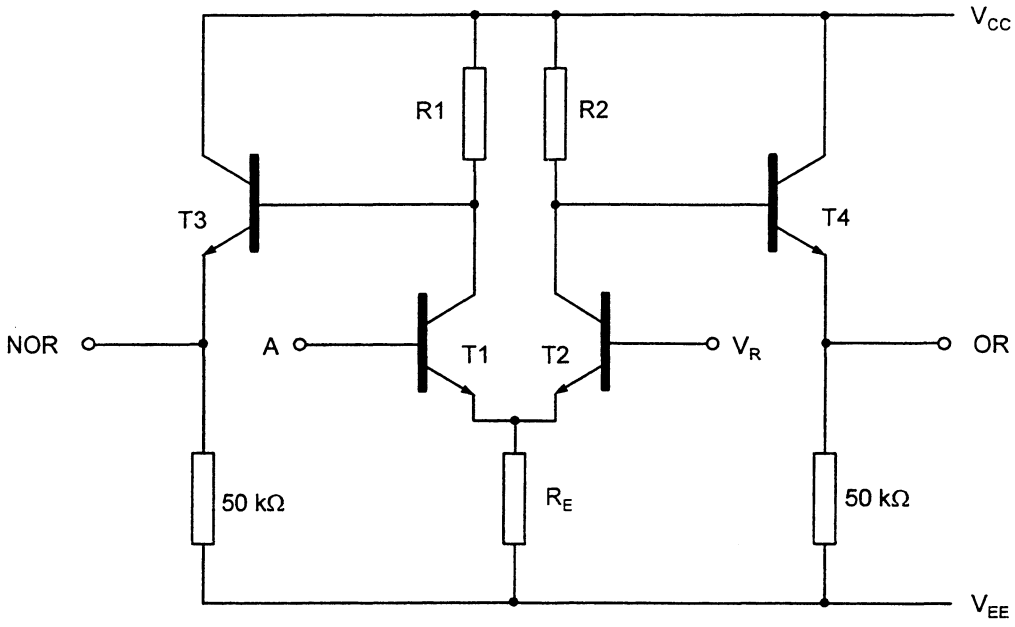

Fig. 4

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PART IIA 2005

3B2 Integrated digital electronics

Answers 3B2 –2005 –

Principal Assessor: **Dr F Udrea**

1.

(b) $Q_0^+ = Q_2Q_1 + \overline{Q_2}\,\overline{Q1}$

$Q_1^+ = \overline{Q_2}\,\overline{Q_1}Q_0 + \overline{Q_2}Q_1 + \overline{Q_0}Q_1$

$Q_2^+ = Q_1\overline{Q_0}\,\overline{Q_2} + Q_1Q_2 + Q_0Q_2$

Present state	Next state
000	001
001	011
011	010
010	110
110	111
111	101
101	100
100	000
000	

(c) 3-bit Gray code counter

2.

(c)

Present state	Light outputs MR	MY	MG	SR	SY	SG	Trigger outputs Long	Short
00	0	0	1	1	0	0	1	0
01	0	1	0	1	0	0	0	1
10	1	0	0	0	0	1	1	0
11	1	0	0	0	1	0	0	1

3.

(b) $V_{out} = 1.61$ V

(c) $I_C = 1.63$mA, $I_B = 163\ \mu$A, $V_B = 1.52$V

4. (a) $V_{OH} = -0.9$V, $V_{OL} = -2.1$V, $R_E = 860\Omega$, R1$= 260\Omega$, $I_{E2} = 4.2$mA, R2$= 309\Omega$

(c) $V_{IH} = -1.425$V, $V_{IL} = -1.575$V, $NM_H = 0.525$V, $NM_L = 0.525$V

(d) $I_{E4} = 102\mu$A, $I_{B4} = 2\ \mu$A

(e) 80 gates