UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIA

Wednesday 11 May 2005 9 to 10.30

Module 3B3

SWITCH-MODE ELECTRONICS

*Answer not more than **three** questions*

All questions carry the same number of marks

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1 (a) The two phase diode bridge in Fig. 1a is supplied from a 50 Hz AC voltage of 240 V rms. The output capacitance is 25 mF and is loaded by a smooth current of 80 A. Calculate the output voltage ripple and conduction angle. You may assume that the diodes are ideal. [20%]

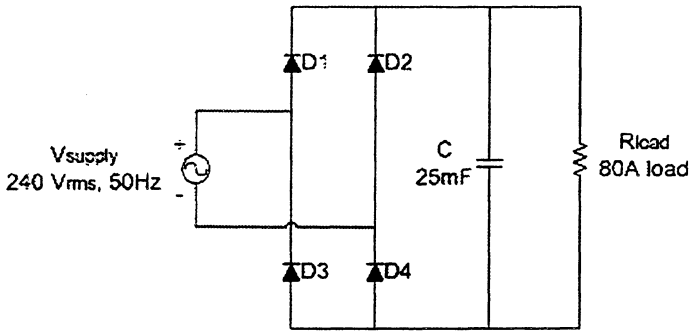

Fig. 1a

(b) Fig. 1b shows a two phase thyristor bridge driven from a 50 Hz 100 V_{pp} supply. It is to deliver a peak load of 50 A. Given that the load time constant is significantly greater than 10 ms, sketch the output voltage wave forms and supply currents for delay angles of 0° and 30° ignoring commutation effects and thyristor forward drop. [20%]

The supply has an evenly distributed internal inductance of 200 μH.

(i) Calculate the worse case commutation overlap for the delay angles above; [30%]

(ii) Estimate the average output voltage in each case. [30%]

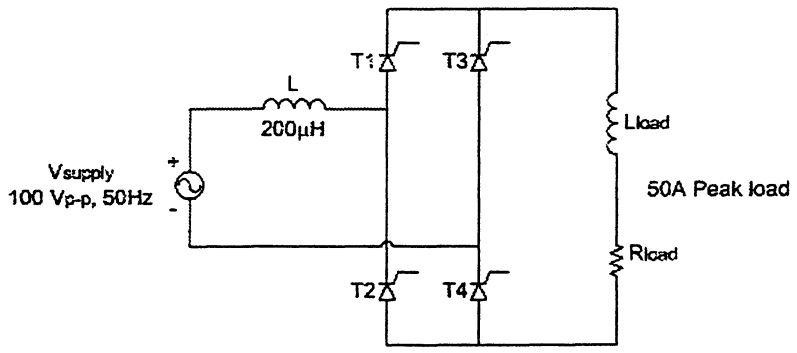

Fig1b

2 (a) The n Channel MOSFET in Fig. 2 is used to switch a clamped inductive load with a smooth 10A current. Given that the load resistance is 24Ω estimate the duty cycle for the switch. *Vgg* has a pulsed rectangular waveform from 0 to 10V.

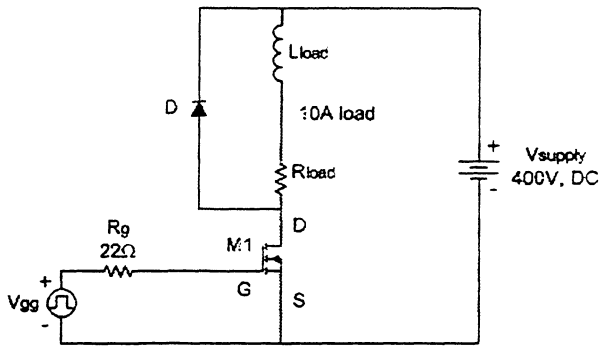

Fig. 2

(b) The gate of the MOSFET is driven via a 22Ω resistor, R_g, by an ideal, rectangular pulse voltage source, V_{gg} that switches from 0 to 10V. Using the MOSFET characteristics given below accurately sketch waveforms for V_{DS}, V_{GS} and I_D for the rising and falling edges of V_{GG}. [40%]

(c) For the turn-on transient, estimate the following:

(i) the time from V_{gg} going high until I_D rises to 10; [10%]
(ii) the fall time for the drain voltage V_{DS}; [20%]
(iii) the energy dissipated in the MOSFET during turn-on. [20%]

You may neglect the output capacitance (C_{oss}= 400pF) in these calculations. What effect would increasing R_g to 100Ω have on the turn-on behaviour of this circuit? [10%]

You should assume the following MOSFET Characteristics.

$I_{DS} = 2.5(V_{GS} - V_T)^2$
V_T=3V
C_{iss} = 2nF Gate-Source Capacitance
C_{rss} = 100pF Drain-Gate Capacitance
C_{oss} = 400pF Drain-Source Capacitance
Ron = 0.3Ω

3 (a) Fig. 3 shows a step down DC/DC converter used to produce a regulated 200W 15V supply from an unregulated supply voltage of between 40 V and 50 V. Accurately sketch the following for a supply voltage of 45V: Voltage V_x, inductor current, and supply current. Assume the diode to be ideal. [20%]

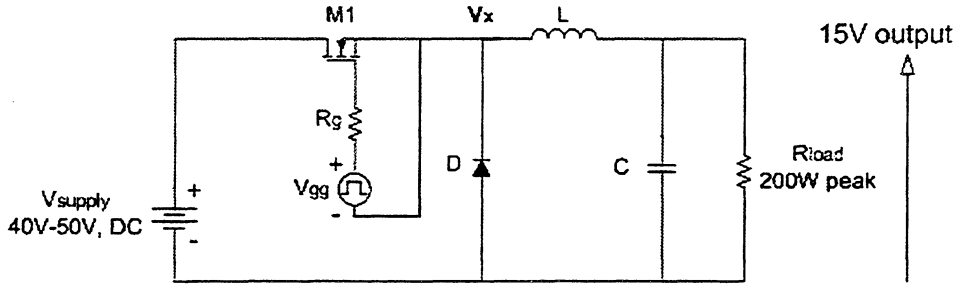

Fig. 3
Vgg: Pulse Width Modulated Gate Signal

(b) (i) Derive an expression for the ripple current in terms of the input voltage and inductance. [25%]

(ii) If the inductance is 100 μH, calculate the switching frequency that must be used to ensure continuous current down to 10% of rated output power, for all input voltages. [25%]

(c) Explain how feedback should be used to obtain a regulated output voltage. Your answer should include a typical control scheme in block diagram form explaining the significance of each block. [30%]

4 Fig. 4 shows a series resonant converter used in an electro heat application. The circuit is supplied from a 600V DC rail with MOSFET pairs T1, T2 and T3, T4 switched in antiphase. Explain how this circuit acts to reduce switching loss and how power transfer to the load is controlled. Sketch waveforms for the load current and inverter output voltage V_{AB} when working at resonance and slightly above resonant frequency. L=1mH, R=50Ω, C=4nF. [20%]

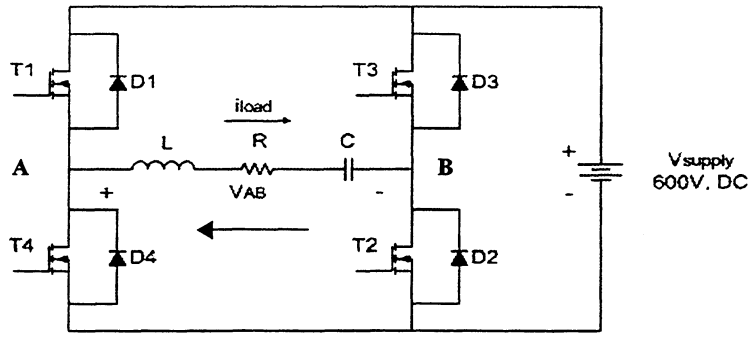

Fig. 4

i) Now assume L=1mH, R=50Ω and C=4nF. What switching frequency should be used to minimise switching loss? Explain what will happen to the switching loss as the frequency is varied from this value. [30%]

ii) By considering the fundamental component of the output V_{AB} estimate the power transferred to the load resistor when switching at the resonant frequency. [20%]

iii) What frequency should be used to reduce the output power to 90% of its peak value? What effect will this have on switching loss? [30%]

END OF PAPER