

ENGINEERING TRIPOS PART IIA

Tuesday 10 May 2005 2.30 to 4

Module 3F5

COMPUTER AND NETWORK SYSTEMS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Attachments:

Diagram for question 2 (1 page), to be submitted with the solution.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1 (a) The following MIPS program fragment was meant to copy a null-terminated block of memory from one location to another. It is syntactically correct but it contains bugs.

```

back:   lw      $3, 0($4)
        addi   $2, $2, 1
        sw     $3, 0($5)
        addi   $4, $4, 1
        addi   $5, $5, 1
        bne   $3, $0, back

```

- (i) Explain the function of all the registers used.
- (ii) Point out the bugs and provide fixes for them.
- (iii) Write down your bug-free version, with line-by-line comments. [40%]

(b) *Pseudoinstructions* are assembly language instructions that are not part of the instruction set of the physical processor. The assembler translates each pseudoinstruction into a short sequence of genuine machine instructions.

For each pseudoinstruction in the following table, write down the shortest sequence of MIPS instructions that performs the same operation. You may have to use the special reserved register \$1, also known as \$at (assembler temporary). The identifiers int16 and int32 represent a 16-bit and a 32-bit constant respectively. The notation $a := b$ in the “semantics” column denotes assignment: register a is assigned the value b.

	Pseudoinstruction	Semantics
(i)	li \$8, int16	\$8 := int16
(ii)	li \$8, int32	\$8 := int32
(iii)	lw \$8, int32(\$9)	\$8 := Memory[\$9+int32]
(iv)	addi \$8, \$9, int32	\$8 := \$9 + int32
(v)	beq \$8, int16, label3	if (\$8 == int16) go to label3
(vi)	ble \$8, \$9, label3	if (\$8 <= \$9) go to label3

[30%]

(c) Explain what the “slt” MIPS instruction does. If this instruction did not exist, and if the only branch instructions available were “beq” and “bne”, how could you obtain the same effect as “slt \$8, \$9, \$10”? Actual assembly code is not required. [30%]

Caveat: MIPS will raise an exception if an arithmetic operation results in overflow. Your solution is not allowed to generate any exceptions.

2 (a) An imaginary computer has a set-associative cache with 1-byte words, 2 words per block, 2 blocks per set, 2 sets, LRU replacement strategy. Assume that, starting from an empty cache, the CPU reads from the following 20 memory addresses in sequence, with no intervening writes: 12 13 14 15 24, 13 12 13 14 20; 22 20 12 24 25, 12 13 14 15 20. (*Punctuation irrelevant, only there for readability. Addresses are in decimal.*)

(i) Define the terms *word*, *block*, *set*, *LRU*. Explain how a set-associative cache works, as opposed to other types of cache. Don't waste time explaining the general principles of caching.

(ii) Trace the above sequence of memory accesses, in the following way. Draw a table to represent a trace. Use one line per memory access. Column 1: address being accessed. Column 2: hit or miss. Other columns, one for each word in the cache: new content of any cache words that just changed, writing N for Memory[N].

(iii) Say how many hits and how many misses there were and show the final content of the cache. [40%]

(b) What is a *multicycle* datapath? What advantages does it offer compared to a *single-cycle* implementation? What is the difference between a multicycle datapath and a *pipelined* datapath? [30%]

(c) You wish to add a new instruction to the MIPS-like machine whose multicycle datapath is depicted in the attached diagram. This instruction, called *add3*, sums together the contents of three register operands:

`add3 $8, $9, $10, $11` $\$8 := \$9 + \$10 + \11

(i) What would be the format of this instruction? Are there any problems with the bit pattern? If so, how would you address them?

(ii) What changes are required to the multicycle datapath shown in the attached diagram in order to allow the processor to execute the *add3* instruction? Add any necessary datapath elements and control signals to the diagram and explain how your solution would work. Return the clearly marked diagram together with your exam script. [30%]

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3 (a) Explain the importance of the seven-layer *open systems interconnect* (OSI) reference model in setting up a modern network protocol. What is the purpose of the model and how is it implemented? Identify the individual layers and explain what is meant by *application oriented processes* and *network dependent processes*. [30%]

(b) Describe the functionality of layer 1 in the seven-layer OSI reference model. Compare the relative merits of the following three media for transmitting computer data across a network: coaxial cable, twisted pair cable and single mode optical fibre. [40%]

(c) The *internet protocol* (IP) is described as having a roughly layer 3 function under the OSI reference model. Given the IP packet format in Fig. 1, explain what features of IP are indeed layer 3 functions and also highlight features of IP which are not layer 3 functions. [30%]

Version	Internet header length (IHL)	Type of service		Total length
Identification		Flags	Fragment offset	
Time to Live	Protocol		Header checksum	
Source address				
Destination address				
Options			Padding	
Data				

Fig. 1

- 4 (a) Describe what is meant by the term *packet switched network*. Describe the function of a simple packet switch and highlight the potential for packet delay. Describe the differences between *path oriented routing* and *datagram based routing* in packet switches. Give an example of a protocol based on each type of switching. [40%]
- (b) Describe how *multi-protocol label system* (MPLS) can be used to reduce delays in a complex network such as the Internet. Is MPLS an example of path oriented routing or datagram routing? Give reasons for your answer. [30%]
- (c) If you were setting up an MPLS network to carry a *voice over internet protocol* (VoIP) service, describe the performance required to guarantee quality of service similar to that offered by existing telephony networks, such as the *synchronous digital hierarchy* (SDH). Identify what might be the key issues in setting up the process for combining packets into an MPLS stream at the edge of the network. [30%]

END OF PAPER

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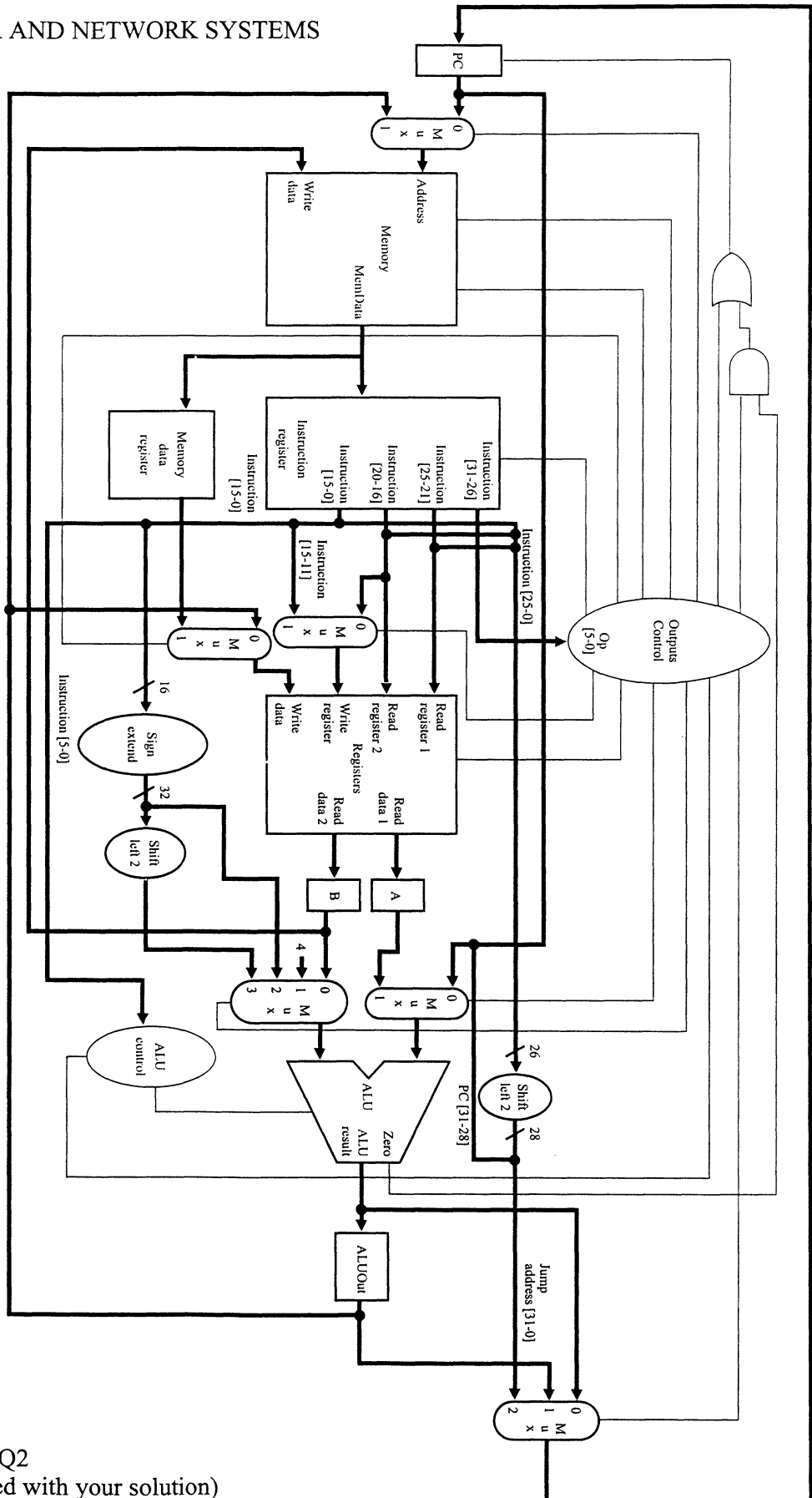


Diagram for Q2
 (to be returned with your solution)