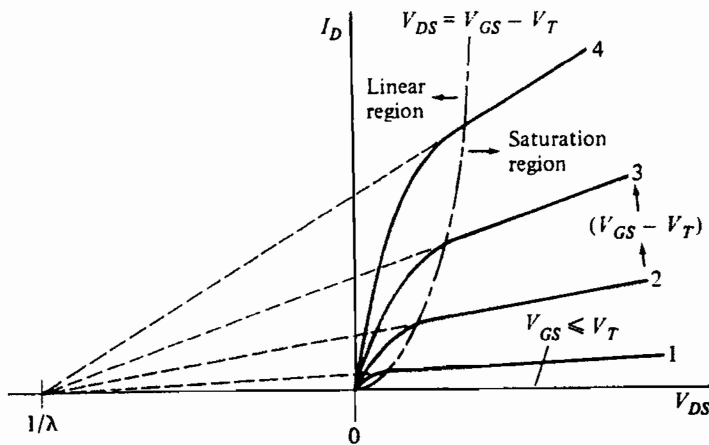
PART IIA 2006
3B2: Integrated digital electronics
Principal Assessor: **Dr F Udrea**

2006 – Part IIA Module 3B2 – Integrated Digital Electronics

1.



Eq 1
Linear region

Eq 2
Saturation region

←Increasing V_{GS} (1-4)

n-channel enhancement mode MOSFET

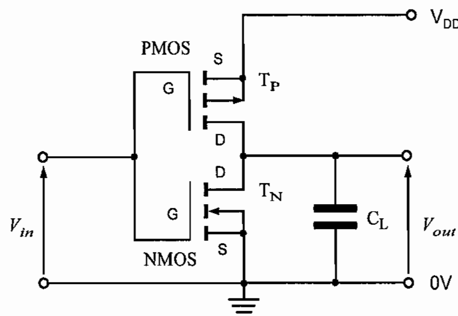
Vertical scale greatly exaggerated to emphasise channel-length modulation effect

Equation 2 predicts that I_D is independent of V_{DS}. The observed behaviour is a gradual increase in I_D with V_{DS}, owing to shortening of the channel – the gradual extension of the pinch off region as V_{DS} rises beyond $V_{GS}-V_T$. This can be modelled as follows:

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad 2'$$

λ is referred to as the *channel length modulation coefficient* and is typically 0.01 – 0.1 V^{-1}. The same $(1+\lambda V_{DS})$ factor may be applied to Equation 1 to ensure continuity at the point $V_{DS} = V_{GS} - V_T$. Another factor affecting I_D is the body effect, in which the potential of the source electrode relative to the substrate affects the channel conductance.

(b) The circuit for the complementary MOS inverter is shown.



Note that since both devices have the same k and $|V_T|$, delays and rise/fall times are the same for both transitions, 0-1 and 1-0.

We shall assume that (i) equations 1 and 2 can be used as given, (ii) that the input changes abruptly, and (iii) there is no load apart from the 5 pF capacitance; (iv) V_{OH} and V_{OL} for the inverter are V_{DD} and 0 V.

(b) The rise time corresponds to the output making its transition from 0 to 1. This is caused by the input switching from 1 to 0; the abrupt transition means that T_N switches off instantly, and we need only consider the charging of C_L thru T_P. We now consider the changing conditions for this device. At the instant T_P begins to conduct, V_{out} is 0 V, V_{SG}= 3 V and V_{SD} is 3 V. Noting this is a p-channel device, we see it is clearly in its saturation region, in which it will remain until V_{SD} falls to $V_{SG} - |V_T|$, or until V_{out} rises to 1 V. The remainder of the rise happens with T_P in its non-saturation/linear region.
We are interested in the 10-90% rise time, i.e. the interval between V_{out} passing through 0.3 V and 2.7 V. This interval comprises two periods that have to be found:

t_{SAT} - C_L charges from 0.3 V to 1.0 V (T_P in saturation region – Eqn 2)
$t_{NON\text{-}SAT}$ - C_L charges from 1.0 V to 2.7 V (T_P in non-sat'n region – Eqn 1).

For t_{SAT}, T_P in its saturation region acts as a constant current source with current:

$$I_D = \frac{k}{2}(V_{SG} - |V_T|)^2 = \frac{k}{2}(3-1)^2 = 2k$$

The time t_{SAT} taken to charge C_L through 0.7 V at constant current is:

$$t_{SAT} = C_L \times 0.7 / I_D = 0.7C_L / 2k = 0.35\frac{C_L}{k}$$

As V_{out} reaches 1 V, T_P enters its non-saturation region and the current thereafter depends on its V_{SD} and hence on V_{out}. The expression for I_D (PMOS case) is:

$$I_D = \frac{k}{2}\left[2(V_{SG} - |V_T|)V_{SD} - V_{SD}^2\right]$$

and noting that $V_{SD} = V_{DD} - V_{out}$, we can substitute:

$$I_D = \frac{k}{2}\left[2(3-1)(3-V_{out}) - (3-V_{out})^2\right] = \frac{k}{2}(3 + 2V_{out} - V_{out}^2) = \frac{k}{2}(1+V_{out})(3-V_{out})$$

Using $\frac{dV_{out}}{dt} = \frac{I_D}{C_L}$ we can write: $\int_0^{t_{NON-SAT}} dt = t_{NON-SAT} = \frac{2C_L}{k}\int_1^{2.7}\frac{dV_{out}}{(1+V_{out})(3-V_{out})}$

This can be simplified using partial fractions to: $\frac{2C_L}{k}\int_1^{2.7}\frac{1}{4}\left(\frac{1}{1+V_{out}} - \frac{1}{3-V_{out}}\right)dV_{out}$

$$\text{Hence } t_{NON-SAT} = \frac{C_L}{2k}\left[\ln\frac{1+V_{out}}{3-V_{out}}\right]_1^{2.7} = \frac{C_L}{2k}\left(\ln\left(\frac{3.7}{0.3}\right) - \ln\left(\frac{2}{2}\right)\right) = 2.51\frac{C_L}{2k}$$

The total rise time is the sum of the intervals in the saturation and non-saturation regions.

Hence a suitable expression is: $\underline{t_{rise} = t_{SAT} + t_{NON-SAT} = \frac{C_L}{2k}(0.70 + 2.51).}$

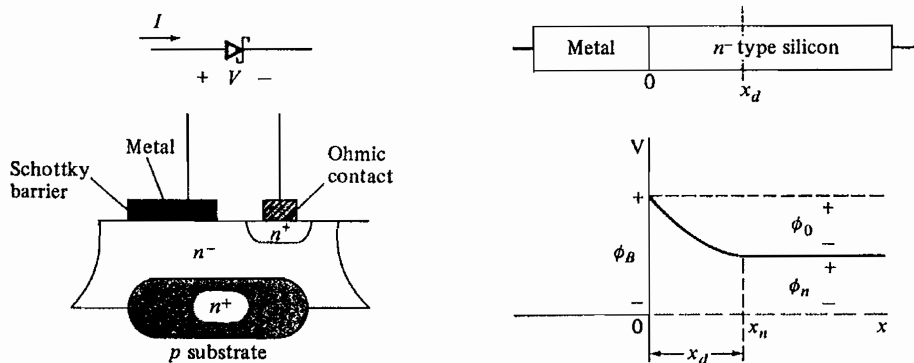
Substituting values, $t_{rise} = \frac{5\times10^{-12}}{2\times10\times10^{-6}}\times 3.21 = \underline{0.80\ \mu S}$

Another possible way to approach this problem is to note that the devices have the same k and $|V_T|$. Hence 10-90% rise time t_r and 10-90% fall time t_f are the same for abruptly changing inputs. Determining t_f is slightly simpler since V_{DS}, V_{GS} and I_D are all positive and substitution in equations 1 and 2 is more convenient.

To reduce the switching time, reduce C or consider increasing V_{DD}: but note that this will increase power consumption. Increasing k by increasing W/L is also worth considering, as it may bring about an improvement, but note that this will also increase the contribution to parasitic capacitance made by T_N and T_P. The effectiveness of this approach will depend on how C_L is distributed between the drains of the FETs and the wiring and driven capacitances, and we are not told this.

Examiner's note: this question was popular, and by and large was well done. The most common difficulty was in identifying the transition between saturation and non-saturation mode.

2. A Schottky (or Schottky-barrier) diode is made by creating a microscopically clean contact between a lightly-doped n-type semiconductor and certain metals.

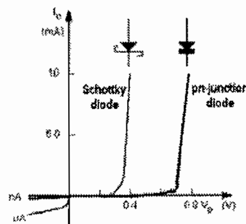


A characteristic **potential barrier** ϕ_B at the metal-semiconductor interface impedes the flow of electrons from metal to semiconductor. The height of the barrier depends only on the two materials used, but is typically 0.6 - 0.8 V. A depletion region is set up in the semiconductor close to the interface. However, electrons in the semiconductor far from the interface may acquire energy sufficient to surmount the barrier and escape to the metal, giving rise to a reverse leakage current. The SBD diode is a "majority carrier" semiconductor device. Only n-type carriers (mobile electrons) play a significant role in normal operation of the device. No slow, random recombination of n- and p- type carriers is involved, so the SBD can cease conduction faster than a p-n junction diode. Advantage of this feature is taken in Schottky bipolar logic circuits.
Detailed analysis gives a result similar to that for the p-n junction diode.

$$I = I_0\left(e^{V/V_0} - 1\right)$$

Reverse bias - adds to the height of the barrier that has to be surmounted
- increases the width of the depletion region

Forward bias - reduces the barrier
- electrons flow more easily from semiconductor to metal

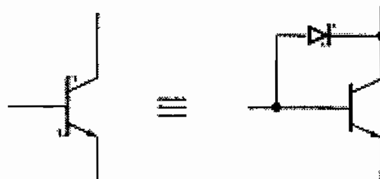


The value of I_0 is much larger than that for the p-n junction diode.

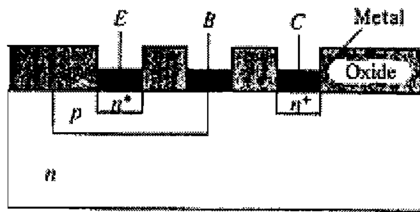
$I_{0(schottky)} \sim 10^{-11}$ A, $I_{0(Si\text{-}Si)} \sim 10^{-15}$ A

Thus a S-B diode of given size typically has a *lower forward voltage* than a comparable p-n junction diode operating at the same forward current.

When a p-n junction is saturated, there is a surplus of minority carriers injected across the junction. In order for the device to stop conducting these minority carriers must be removed. Since the removal depends substantially on diffusion, it has a long time constant, from 10-1000 ns. This leads to slow switching.



The effect can be alleviated if the p-n device can be prevented from entering saturation. The performance of gates in TTL - which depend on saturation - can be much improved by use of *Schottky transistors*.



A SBD is connected across base-collector junction of each bipolar transistor liable to saturate, forming a *clamp* and preventing the junction becoming forward biased by more than approximately 0.5 V, insufficient to allow substantial charge to accumulate in the base region. Schottky transistors switch from saturation about 3-5 times faster than unmodified TTL.

(b) The RAM cell consists of a pair of cross-coupled inverters (M2, M3 and M4, M5). This forms a bistable unit which can be in either of two stable states corresponding to a stored **logic 0** or **logic 1**.

If inverter (M2,M3) generates **logic 1**, that will cause inverter (M4,M5) to output **0**, which will cause (M2,M3) to output **1** ... so maintaining the original values stable.

A similar argument holds if inverter (M2,M3) generates **logic 0**, giving **logic 1** at the output of (M4,M5).

Hence the cell may assume only two states, and if isolated from external influences will retain its state while power is applied.

MOSFETs M1 and M6 allow the inverter inputs to be accessed from outside for writing a value (**0** or **1**), and the outputs, for reading. Both are controlled by the ‘word’ line which would normally be controlled by decoding an address bus.

The state may be changed by driving the ‘bit’ and ‘$\underline{\text{bit}}$’ lines to new complementary values and operating switching transistors M1 and M6 by setting ‘word’ **high**. The new value is forced on to the inputs/outputs, of the two inverters, which assume the new state.

To read out data, both bit lines are preset to precisely the same potential, typically $V_{DD}/2$. They are fed to the inputs of a sensitive comparator, which will initially indicate the equivalence between the lines. The switching MOSFETS M1, M6 are then enabled. One inverter will drive its corresponding but line high, the other low, by a few mV. This is because the inverters are by design weak, and the bit lines are a substantial capacitive load.

The comparator then indicates 0 or 1 according to the sense of the perturbations introduced to the bit lines.

When the ‘word’ lines are deselected, M1 and M6 cease conducting and the inverters revert to their former logic values.

This only works if:

(a) the gates driving ‘bit’, ‘$\underline{\text{bit}}$’ are strong (low impedance sources)

(b) M1 and M6 are highly conductive

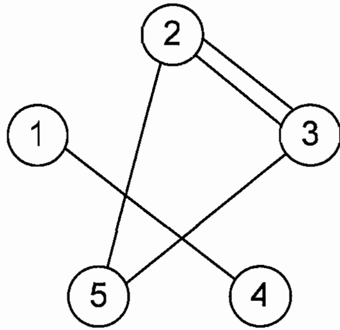
(c) the devices M2, M3 and M4, M5 are weak (high impedance), so can be overridden by ‘bit’, ‘$\underline{\text{bit}}$’ applied via M1, M6.

Hence M1, M6 have a relatively large W/L, while M2-M5 have much smaller W/L.

Examiner's note: most candidates described some features of the SBD, *but a number failed to mention its electrical (I/V) characteristics or compare it with the p-n diode.*

In the second part, most candidates were able to explain how the memory circuit works. Common difficulties were the purposes of the control signals or how to optimise the MOSFETs.

3. Only one merging can be done (2 &3) with identical outputs. This reduces the state table to 4 states.

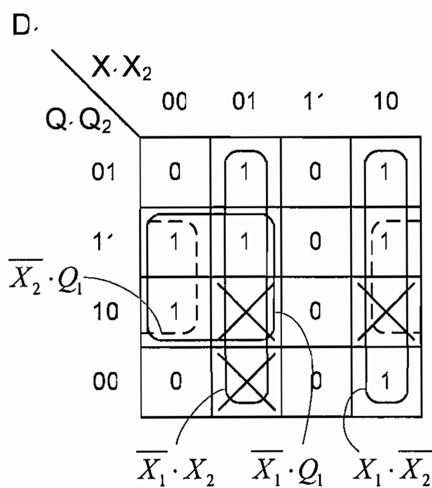


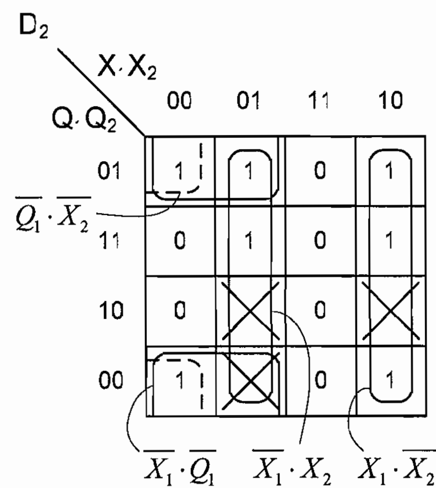
Present State	Next state for X_1X_2 = 00	01	11	10	Z_1Z_2
①	①	2	4	3	0 1
② ③	5	②	4	③	1 1
④	1	--	④	3	0 0
⑤	5	--	4	--	1 0

Present State $Q_1Q_2 \equiv Z_1Z_2$	Next state for X_1X_2 = 00	01	11	10	Input D_1 for bistable whose output is Z_1, X_1X_2 = 00	01	11	10	Input D_2 for X_1X_2 = 00	01	11	10
① 0 1	0 1	1 1	0 0	1 1	0	1	0	1	1	1	0	1
② ③ 1 1	1 0	1 1	0 0	1 1	1	1	0	1	0	1	0	1
④ 0 0	0 1	- -	0 0	1 1	0	- -	0	1	1	- -	0	1
⑤ 1 0	1 0	- -	0 0	- -	1	- -	0	- -	0	- -	0	- -

A B

The bistable inputs D1 and D2 are the next states. The outputs are the same as Q1 and Q2. The k-maps are shown below:





So $D_1 = \overline{X_1}\cdot X_2 + X_1\cdot\overline{X_2} + \overline{X_1}\cdot Q_1 + Q_1\cdot\overline{X_2}$ *

$D_2 = \overline{X_1}\cdot X_2 + X_1\cdot\overline{X_2} + \overline{X_1}\cdot\overline{Q_1} + \overline{Q_1}\cdot\overline{X_2}$ *

* Added terms to make logic hazard free

3. (b) When power is first applied, the capacitor will charge up to 5V. This acts as power-up reset. When *START* is pressed Q_D goes **high** and stays **high** after the button is released. With Q_D **high** the counter begins to count. This is a usual counter that counts in a decimal sequence 0-1-2-3-4-5. When 5 is reached then the output of the NAND gate goes **low** turning on the LED (the LED needs a voltage drop across it and a minimum current to be lit). The **low** output of the NAND gate also appears at the input of the AND gate which will disable the clock input. The counter will then stay at 5 and the LED lit.

To reset the counter to zero one can press the *RESET* button so that Q_D goes **low** and will stay **low** until the start button is pressed again. Without the *RESET* button, the LED will stay lit.

The current that flows through the LED is all sank by the output of the NAND gate (the AND gate will have a high impedance input and therefore will not sink any current). This current is (5 V - 1.7 V)/300 Ω = 11 mA. Therefore the NAND gate should be able to sink 11 mA without burning out !

4. The system has 8 inputs $D_0 - D_7$, there other terminals S_0-S_2 and one output D_{out}.

One can extract the following function[1]:

$$
\begin{aligned}
D_{out} \quad = \quad & \overline{S_0}\,\overline{S_1}\,\overline{S_2}D_0 + S_0\overline{S_1}\,\overline{S_2}D_1 + \\
& \overline{S_0}S_1\overline{S_2}D_2 + S_0S_1\overline{S_2}D_3 + \\
& \overline{S_0}\,\overline{S_1}S_2D_4 + S_0\overline{S_1}S_2D_5 + \\
& \overline{S_0}S_1S_2D_6 + S_0S_1S_2D_7
\end{aligned}
$$

This is the function of a multiplexer having inputs $D_0 - D_7$, control terminals S_0-S_2 and one output D_{out}. For example when S_0=0, S_1=0 and S_2=0, D_{out}=D_0, etc.

The p-channel operates in the linear region when the drain-source voltage drop is **low** and in the saturation region (or close to saturation region) when its drain-source voltage drop is **high** (close to V_{DD}) Its gate-source voltage is always -V_{DD}.

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[1] note that other forms of logic functions can describe a multiplexer

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4 (b). To perform the function of the multiplexer, the structure in Fig. 5 shows a tree like implementation. When the gate is high the voltage drop across the n-channel devices becomes low. Thus D_{out} should be equal to D_0 when S_0=0 , A=0 and E=0. When that is compared to the multiplexer function, A= $\overline{S_1}$ and E= $\overline{S_2}$. Similarly B=S_1, C=$\overline{S_1}$, D= S_1, F= S_2

The implementation in Fig.5 uses less transistors but the one in Fig. 4 is much faster as there are fewer n-channel transistors in series between any node and ground. The implementation in Fig.4 also can be laid out in a tight grid-like structure leading to smaller area consumption.

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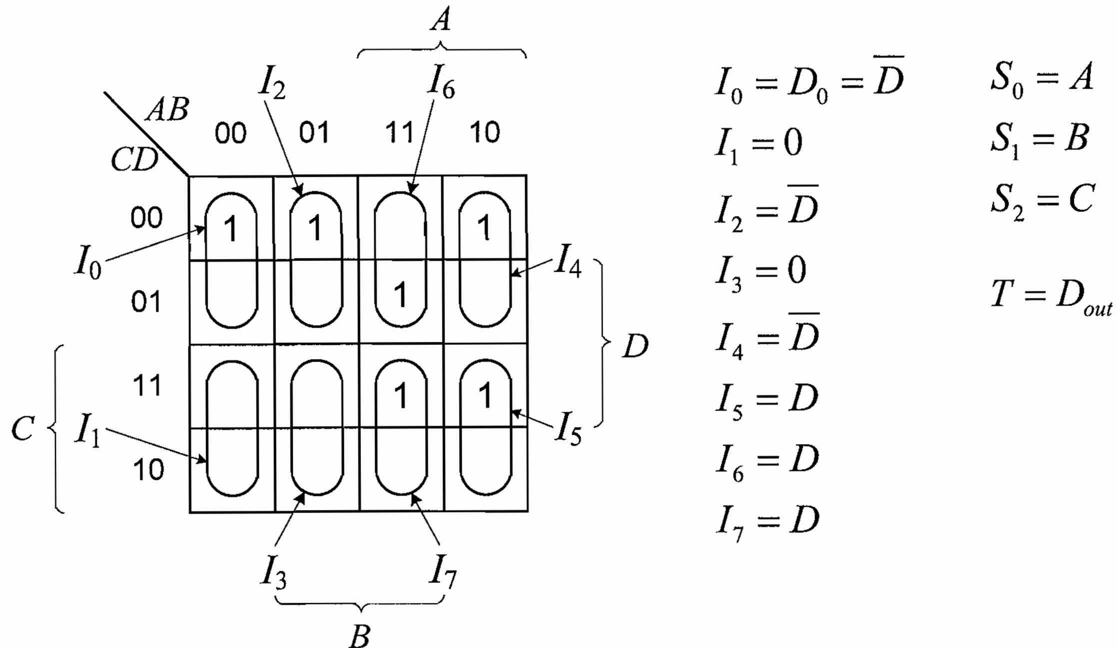

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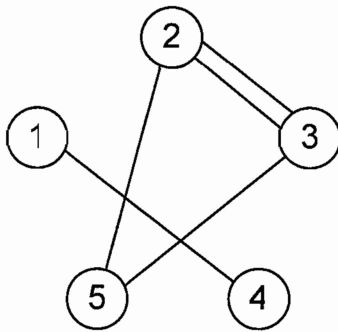

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A   *B*

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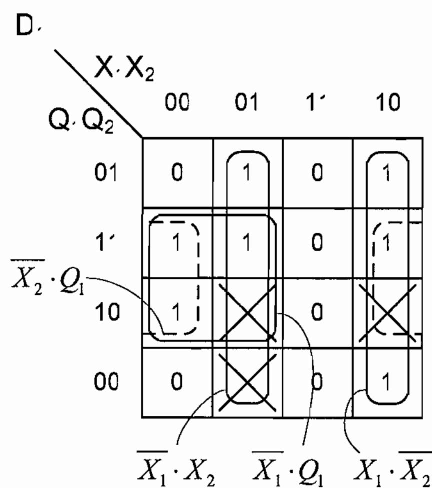

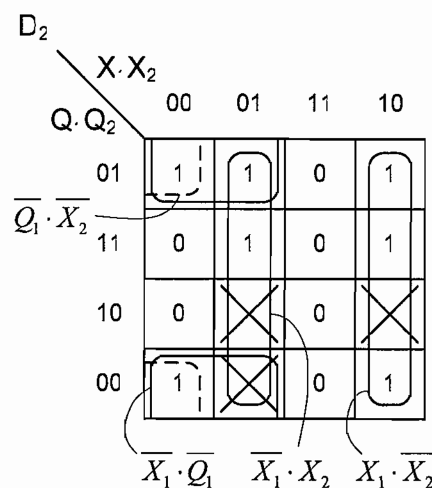

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& \overline{S_0}\,\overline{S_1}S_2D_4 + S_0\overline{S_1}S_2D_5 + \\
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This is the function of a multiplexer having inputs $D_0 - D_7$, control terminals S_0-S_2 and one output D_{out}. For example when S_0=0, S_1=0 and S_2=0, D_{out}=D_0, etc.

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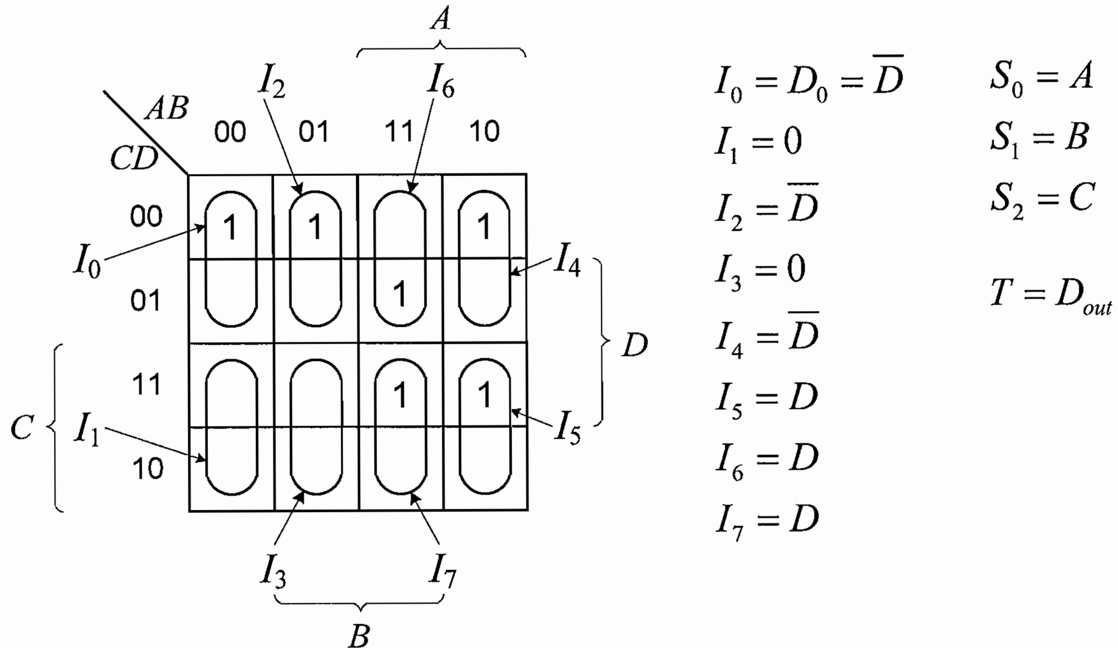

PART IIA 2006 3B2 NUMERICAL ANSWERS

1. $t_{rise} = \dfrac{1.6\,C_L}{k} = 0.8\mu S$

3. (a)

$$D_1 = \overline{X_1}\cdot X_2 + X_1\cdot\overline{X_2} + \overline{X_1}\cdot Q_1 + Q_1\cdot\overline{X_2}$$

$$D_2 = \overline{X_1}\cdot X_2 + X_1\cdot\overline{X_2} + \overline{X_1}\cdot\overline{Q_1} + \overline{Q_1}\cdot\overline{X_2}$$

3. (b) This is a usual counter that counts in a decimal sequence 0-1-2-3-4-5. The counter will then stay at 5 and the LED lit. The NAND gate should sink 11 mA.

4. Multiplexer

$$\begin{aligned} D_{out} = {} & \overline{S_0}\,\overline{S_1}\,\overline{S_2}D_0 + S_0\overline{S_1}\,\overline{S_2}D_1 + \\ & \overline{S_0}S_1\overline{S_2}D_2 + S_0S_1\overline{S_2}D_3 + \\ & \overline{S_0}\,\overline{S_1}S_2D_4 + S_0\overline{S_1}S_2D_5 + \\ & \overline{S_0}S_1S_2D_6 + S_0S_1S_2D_7 \end{aligned}$$

4 (b) A= $\overline{S_1}$, E= $\overline{S_2}$, B=S_1, C= $\overline{S_1}$, D= S_1, F= S_2

4 (c)

$I_0 = D_0 = \overline{D}$

$I_1 = 0$

$I_2 = \overline{D}$

$I_3 = 0$

$I_4 = \overline{D}$

$I_5 = D$

$I_6 = D$

$I_7 = D$

$S_0 = A$

$S_1 = B$

$S_2 = C$

$T = D_{out}$