ENGINEERING TRIPOS PART IIA

Friday 12 May 2006 2.30 to 4

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1. (a) The drain current I_D for a MOSFET may be modelled either by equation (1) or by equation (2) according to the region in which the device is operating. Sketch a typical output characteristic for a MOSFET and show clearly on your graph the regions in which the two equations may be applied. Name the regions. [20%]

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad \text{for} \quad V_{DS} < (V_{GS} - V_T) \qquad (1)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \quad \text{for} \quad V_{DS} \geq (V_{GS} - V_T) \qquad (2)$$

Discuss the limitations of equation (2) for describing the behaviour of the device in the second region, and suggest how the equation can be modified to model the observed dependencies more accurately. [20%]

(b) A complementary MOS inverter is fabricated from two transistors each of device transconductance k, and is run from a 3 V supply. The threshold voltages of the NMOS and PMOS devices are 1 V and –1 V respectively. The output terminal is connected to a purely capacitive load C_L.

Derive an expression for the 10-90% rise time at the output, assuming that the input voltage changes abruptly. State any other assumptions made. [40%]

If k = 10 μA V^{-2} and the external load C_L is 5 pF, determine the rise time under these conditions. Discuss briefly how the switching speed might be improved. [20%]

2. (a) With the aid of a diagram describe the electrical characteristics of the Schottky Barrier diode, emphasising how they differ from those of the silicon p-n junction diode. [20%]

Discuss how advantage has been taken of this device, in the development of faster forms of integrated bipolar logic, and explain how the speed improvement was achieved. [20%]

(b) Fig. 1 shows a simple CMOS static random access memory cell. Explain the mode of operation of this circuit, and explain the role of the signals *word*, *bit,* and $\overline{bit}$ in allowing data to be written and read. Describe briefly the special design criteria that apply to the MOSFETs M1 - M6. [60%]

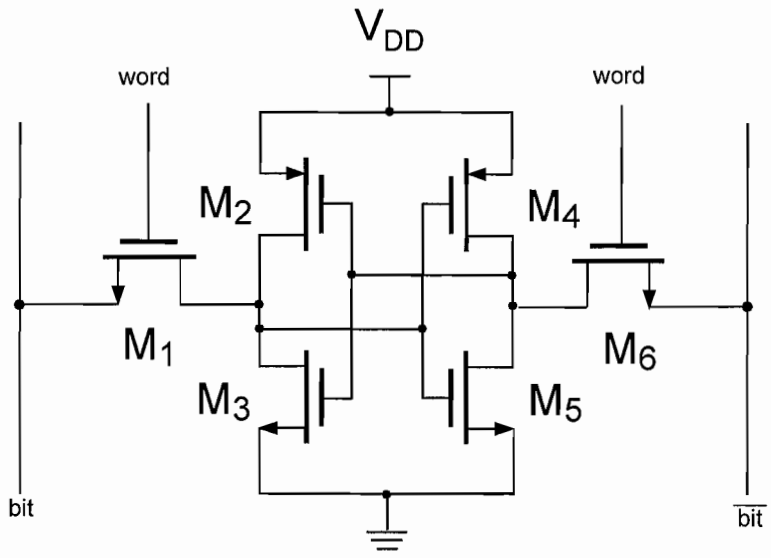

Fig. 1

3. (a) Fig. 2 shows a reduced state table for a certain system for which merging is to be done. Draw a Merger diagram and show a reduced state table suitable for a Moore architecture. [20%]

The bistable allocation for the states is required to be identical to the outputs Z_1 Z_2. Using D-type bistables, find what the inputs D_1 and D_2 should be for the two bistables [40%]

(b) Fig. 3 shows a sequential system containing a counter, a start-up circuit, logic gates, and an LED. There are two push buttons that determine the 'START' and the 'RESET' of the circuit.

Describe the operation of the various blocks in the circuit and determine the basic function that the circuit performs when the 'START' button is pressed. Why does the circuit require a 'RESET' button? [30%]

If the on-state voltage drop across the LED is 1.7 V determine the maximum current that needs to be absorbed by the NAND gate. [10%]

X_1X_2 00	01	11	10	Z_1Z_2
(1)	2	4	3	01
5	(2)	--	3	11
5	2	4	(3)	11
1	--	(4)	3	00
(5)	--	4	--	10

Fig. 2

(cont.

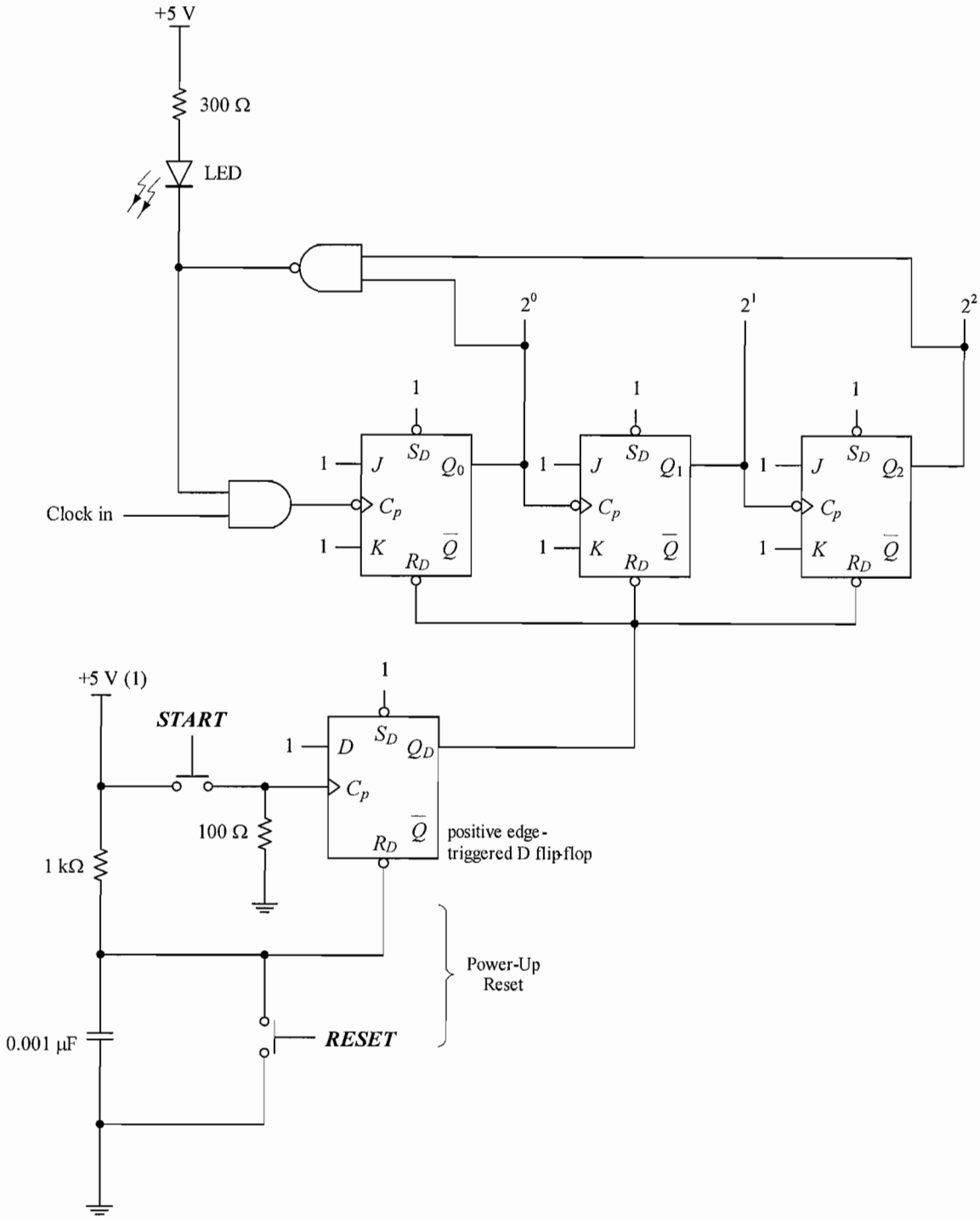

Fig. 3

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4. (a) Fig. 4 shows a PLA-like implementation of a combinational circuit. Determine what logic function the circuit performs and explain the operation of the circuit function of different signals on the various n-channel MOSFETs. Comment on the operation regime for the p-channel and n-channel MOSFETs and their relative on-state resistance when the devices are ON. [30%]

(b) Fig. 5 shows a possible, alternative implementation of the combinational circuit described by Fig. 4. Determine the inputs to the n-channel MOSFET gates A, B, C, D, E, F, as a function of the inputs S_0-S_2 and/or D_0-D_7 in order that the circuit shown in Fig. 5 performs the same function as that shown in Fig. 4. What are the advantages and disadvantages of the two implementations? [30%]

(c) Use the circuit in Fig. 4 to build the following logic function:

$$T = \Sigma\ (0,4,8,11,13,\ 15).$$ [40%]

There is no need to draw the actual circuit implementation.

(cont.

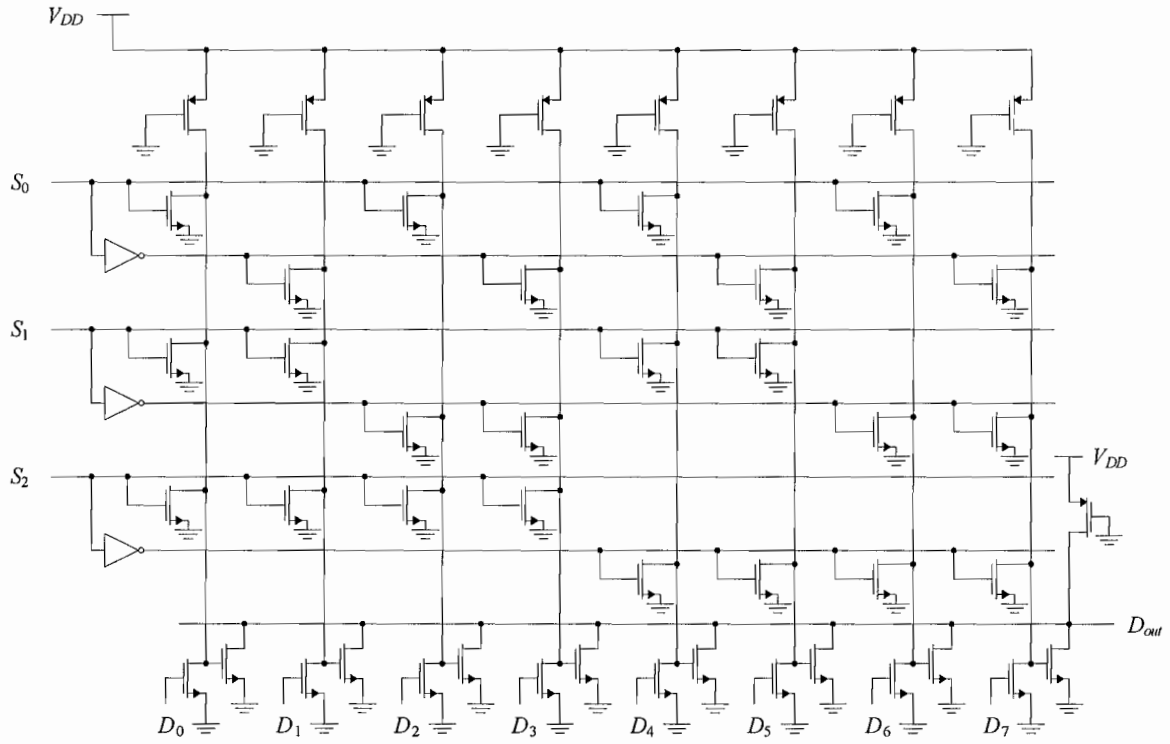

Fig. 4

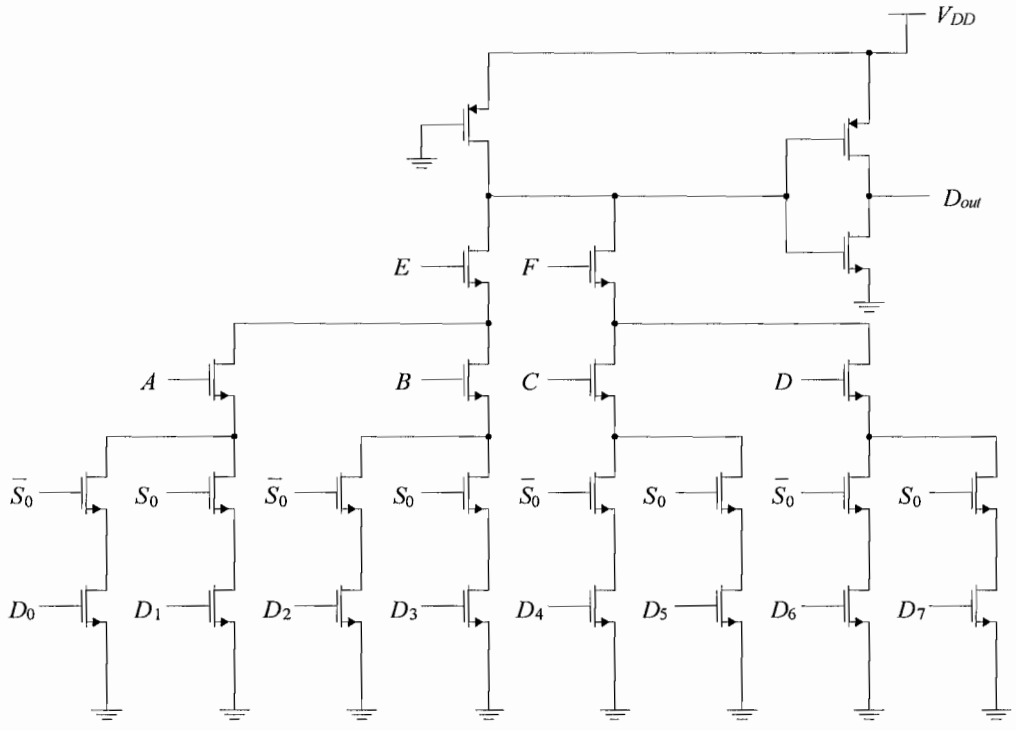

Fig. 5

END OF PAPER

PART IIA 2006 3B2 NUMERICAL ANSWERS

1. $t_{rise} = \frac{1.6\,C_L}{k} = 0.8\mu S$

3. (a)

$$D_1 = \overline{X_1}\cdot X_2 + X_1\cdot\overline{X_2} + \overline{X_1}\cdot Q_1 + Q_1\cdot\overline{X_2}$$

$$D_2 = \overline{X_1}\cdot X_2 + X_1\cdot\overline{X_2} + \overline{X_1}\cdot\overline{Q_1} + \overline{Q_1}\cdot\overline{X_2}$$

3. (b) This is a usual counter that counts in a decimal sequence 0-1-2-3-4-5. The counter will then stay at 5 and the LED lit. The NAND gate should sink 11 mA.

4. Multiplexer

$$\begin{aligned} D_{out} = {} & \overline{S_0}\,\overline{S_1}\,\overline{S_2}D_0 + S_0\overline{S_1}\,\overline{S_2}D_1 + \\ & \overline{S_0}S_1\overline{S_2}D_2 + S_0S_1\overline{S_2}D_3 + \\ & \overline{S_0}\,\overline{S_1}S_2D_4 + S_0\overline{S_1}S_2D_5 + \\ & \overline{S_0}S_1S_2D_6 + S_0S_1S_2D_7 \end{aligned}$$

4 (b) A= $\overline{S_1}$, E= $\overline{S_2}$, B=S_1, C= $\overline{S_1}$, D= S_1, F= S_2

4 (c)

$I_0 = D_0 = \overline{D}$ $\quad S_0 = A$

$I_1 = 0$ $\quad S_1 = B$

$I_2 = \overline{D}$ $\quad S_2 = C$

$I_3 = 0$ $\quad T = D_{out}$

$I_4 = \overline{D}$

$I_5 = D$

$I_6 = D$

$I_7 = D$