ENGINEERING TRIPOS PART IIA

Tuesday 9 May 2006 2.30 to 4

Module 3F5

COMPUTER AND NETWORK SYSTEMS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Explain what is meant by a pipeline *hazard*. Distinguish between data and branch hazards. [20%]

(b) The following series of MIPS instructions is executed on the pipelined datapath shown in Fig. 1.

```
lw $8,0($9)          # $8 loaded with data at address $9+0
add $9,$9,$10        # $9 loaded with $9+$10
add $9,$9,$8         # $9 loaded with $9+$8
sw $9,0($10)         # $9 stored at address $10+0
```

If hazards are resolved by stalling the pipeline, how many clock cycles are required to execute the instructions (i) without data forwarding, and (ii) with data forwarding? [20%]

(c) The datapath in Fig. 1 is modified to allow superscalar operation, with up to two instructions issued each clock cycle. When two instructions are issued, one of them must be an arithmetic/logic operation or a branch, while the other must be a load/store.

(i) Describe qualitatively the hardware changes required for this type of superscalar operation. [25%]

(ii) Assuming the pipeline has data forwarding, how many clock cycles will the instructions in (b) take to execute now? [10%]

(d) Explain why a superscalar pipeline's resources might be better exploited by simultaneous multithreading (SMT). What further hardware changes are required for SMT? How might the memory system compromise SMT performance? [25%]

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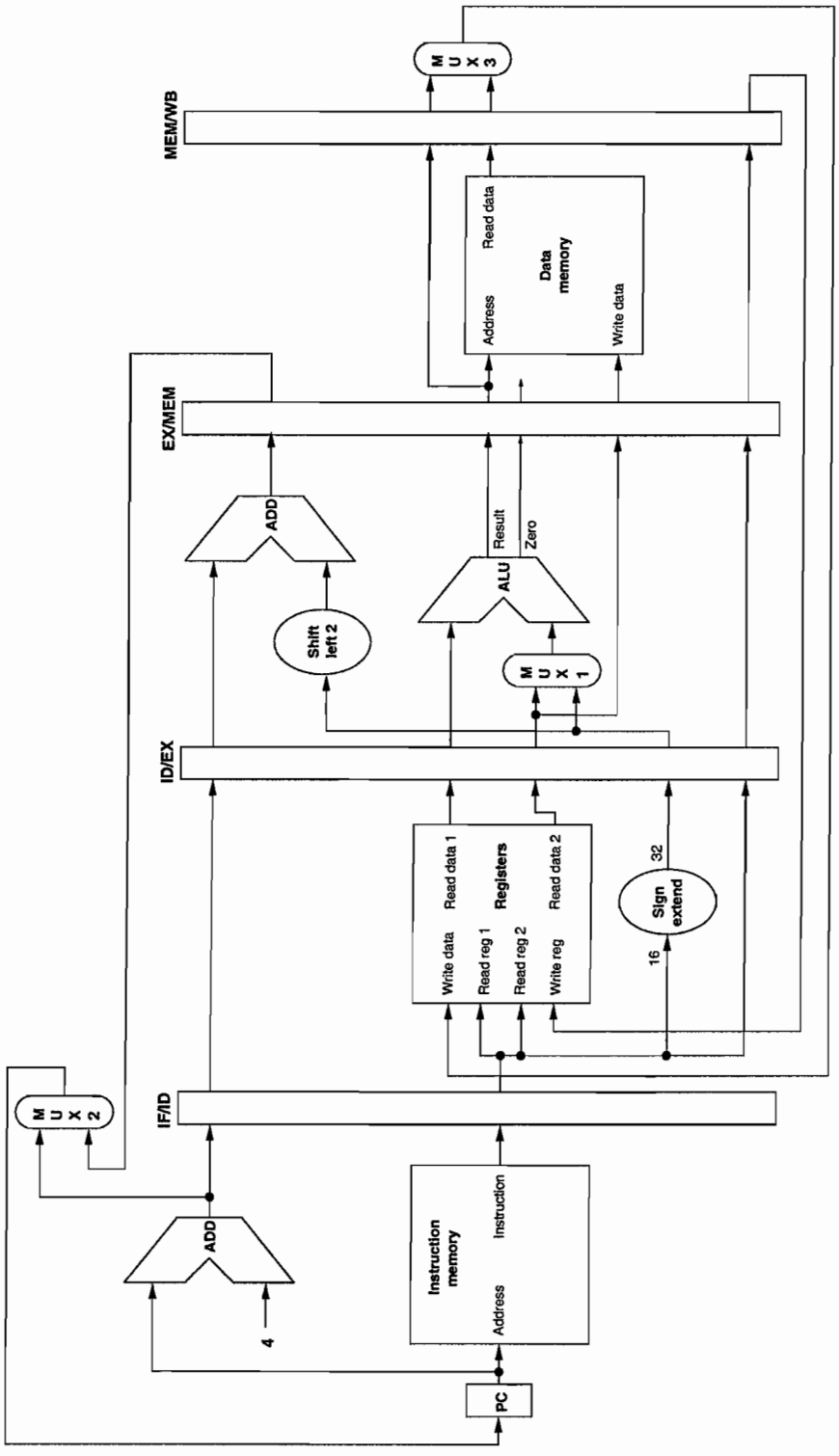

Fig. 1

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2 (a) Compare and contrast synchronous and asynchronous buses. Give examples of where each type of bus might be used in a modern computer system. [25%]

(b) Discuss the relative advantages and disadvantages of polling, interrupt-driven I/O and direct memory access (DMA). For each method, suggest one common I/O task for which it might be used. [25%]

(c) What precautions must be taken when using DMA in conjunction with caches and virtual memory systems? [25%]

(d) Explain the reasons behind the recent trend to replace parallel I/O buses with serial point-to-point networks. Give one specific example of such a transition in consumer PC hardware. [25%]

3 (a) Define the purpose of the open systems interconnect (OSI) reference model. Sketch the model for two computers interconnected via a network. Explain how each layer passes information across the model. [30%]

(b) Describe the functions of layer 2 and layer 3 in the OSI model. Explain why layer 2 is split into two sub-layers when considering local area networks (LANs). [20%]

(c) One of the key features of the medium access control sub-layer is the hardware address structure used in LANs and network equipment. What is the format of this address and why has it evolved in layer 2? Is this layer appropriate for this address? [30%]

(d) When using the transmission control protocol/ internet protocol (TCP/ IP) in a LAN, one of the most important functions of a router is to convert between network and hardware addresses. What is the name of this protocol and how does it work? What might happen if an unknown hardware address is converted? [20%]

4 (a) A circuit switched network is to be constructed to connect four separate groups of three subscribers (twelve in total), as shown in Fig. 2. There are six trunks available to interconnect these groups.

(i) Explain how circuit switching works and why it is a good mechanism for constructing this network. Why is a full mesh not appropriate? [20%]

(ii) Sketch the layout of the circuit switch and label all the relevant elements in the system. Connect A–B″, A′–D′, A″–C″, B–C′, B′–D″ and C–D. What are the limits of connectivity? [20%]

(iii) What happens if a connection is needed between the subscribers in each of the four groups? How could this be implemented? [15%]

(b) Circuit switched networks were eventually replaced by plesiochronous digital hierarchies (PDH). Explain how PDH works and why it is a more efficient system than circuit switching. [25%]

(c) PDH was subsequently phased out in favour of synchronous digital hierarchies (SDH). Explain why SDH is better than PDH and describe the process of integrating a PDH channel into SDH. How is this process managed? [20%]

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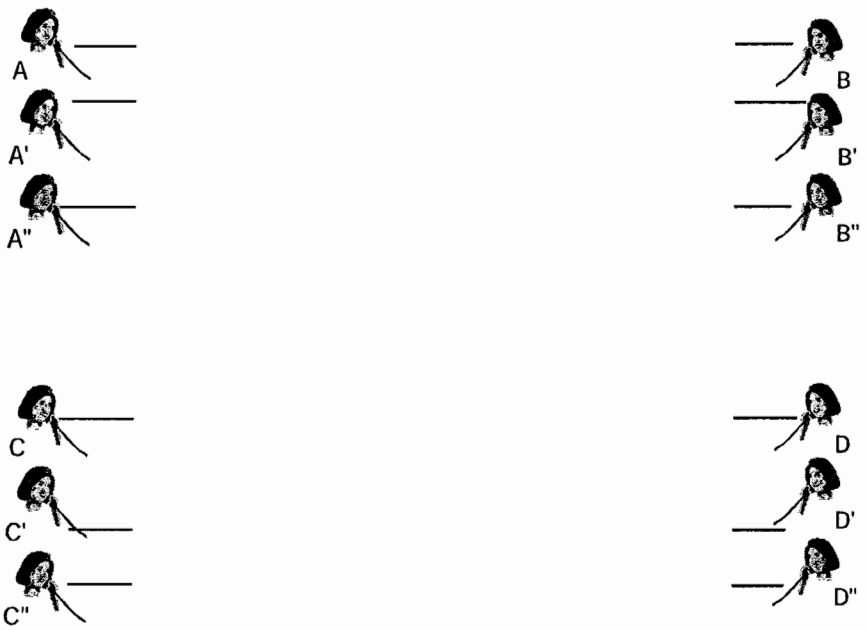

Fig. 2

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