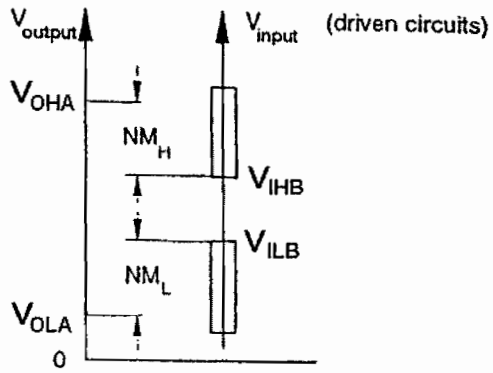
1. (a) **Main reasons for popularity of CMOS**:

- Gate inputs are effectively open-circuit, very high impedance, easy to drive
- Power supply current for static/low frequency apps is very low, ideal for battery-powered portable devices
- Very good noise immunity, ~0.4 V_{DD} for inverter both low and high states (not quite so high for multi-input gates)
- Fully restored logic levels V_{DD} and 0V
- Can operate over wide range of supply voltages
- Creates little electrical noise
- Easily integrated with linear circuitry for complex mixed-signal designs

Main disadvantages:

- Not as fast as GaAs or some forms of bipolar
- Comparatively sensitive to static breakdown
- Liable to destructive latch-up as compound doped layers form thyristor-like structures

(b)



V_{OHA} and V_{OLA} represent respectively:

- the lowest voltage supplied by logic circuit A delivering logic '1', and
- the highest voltage supplied by an output delivering logic '0'

V_{IHB} and V_{ILB} represent respectively:

- the lowest input to B acceptable as logic '1'
- the highest input to B acceptable as logic '0'

If the output of A is connected to the input of B, the noise margins observed in the High and Low states are:

$$NM_H = V_{OHA} - V_{IHB} \quad \text{and} \quad NM_L = V_{ILB} - V_{OLA}$$

Both noise margins must be positive if the pair of circuits is to operate consistently. Their magnitude must be δ or greater if superimposed noise of voltage magnitude up to δ is to be rejected.

Note that the voltages V_{OH} and V_{OL} are liable to depend on the magnitude of the current flowing in the corresponding output devices – i.e. they depend on fan-out.

(c) (i) Bipolar drives CMOS

$N_{MH} = V_{OHbip} - V_{IHcmos} = 7.4 - 8.5 = -1.1$ V

$N_{ML} = V_{ILcmos} - V_{OLbip} = 1.0 - 0.4 = 0.6$ V

(ii) CMOS drives bipolar

$N_{MH} = V_{OHcmos} - V_{IHbip} = 9.9 - 2 = 7.9$ V

$N_{ML} = V_{ILbip} - V_{OLcmos} = 0.8 - 0.1 = 0.7$ V

(d) (i) would not work since $N_{MH} < 0$

(ii) will work satisfactorily but note that it will be significantly more susceptible to noise in the low state.

If 10 inputs were driven, the bipolar → CMOS margins (for operation assumed to be static or low-frequency) would be unaffected, since the table indicates that CMOS gates draw no input current.

The CMOS → bipolar noise margins are liable to be affected.

With the CMOS output high, the gate must source $10 \times 40 = 400$ μA when delivering '1' to the following 10 gates. This is not a particularly onerous demand.

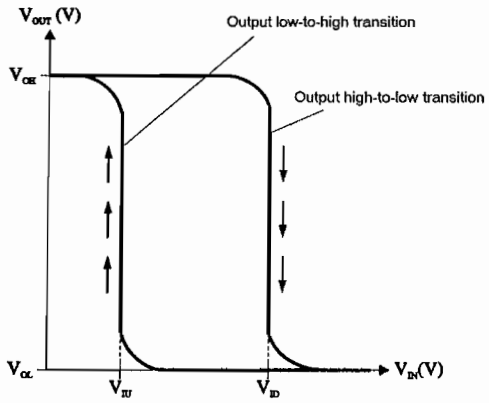
With the CMOS output low, the gate must sink $10 \times 1.6 = 16$ mA at its output, from the following inputs. This might be beyond its capacity, or if not, it is liable to raise V_{OLcmos} and erode still further the already poor noise margin in the low state.

In either case, with 10 inputs driven, the additional capacitance will affect the rise/fall time achieved. Full analysis calls for more information about the devices in use and their dimensions, which determine the ability of the output stages to source/sink current to charge/discharge this parasitic load, but drivers implemented in CMOS are often limited cf some bipolar families in terms of available output current.

Examiner's note: this question was very popular, and by and large was well done. Not all were able to come up with 2 advantages and 2 disadvantages of CMOS, though several know more. A few were not sure which V_{IL}, V_{OH} to use, and the final section on fan-out was done with mixed success.

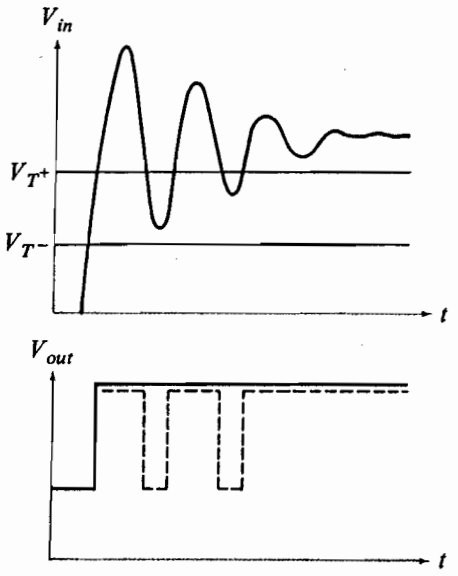
2. In the conventional CMOS logic inverter, the low-to-high and high-to-low transitions occur at the same input voltages. In the Schmitt gate the phenomenon of HYSTERESIS is exhibited, where the L-H and H-L transitions occur at different input voltages.

The voltage transfer characteristic exhibits a hysteresis loop as shown in the Schmitt inverter characteristic.



- V_{OUT} makes its H-L transition when the *rising* input voltage exceeds
  $V_{IN} = V_{ID}$
- V_{OUT} makes its L-H transition when the *falling* input voltage drops below
  $V_{IN} = V_{IU}$
- The condition $V_{ID} > V_{IU}$ must hold.
- $V_{ID}–V_{IU}$ is referred to as the hysteresis of the gate.

If the input V_{IN} exhibits noise, the hysteresis characteristic is helpful in cleaning up and conditioning the signal for digital processing. This may be used to advantage in luie receiver applications. Because of the fast transition times in high speed digital systems, and the intrinsic parasitic series inductance and parallel capacitance of a signal wire, the voltage pulse seen at the end of a long line might be as below (characteristic ringing).



The output of a simple inverter with switch level V_{ID} would exhibit additional spurious pulses.

Setting the switching level to V_{IU} would not necessarily solve the problem as it might cause triggering on other noise events.

The output of a Schmitt inverter with thresholds V_{ID}, V_{IU}, as described would alleviate this effect in a single step, as required.

The Schmitt inverter can also be used for converting non-digital signals (e.g. sine waves) to a digital pulse train.

The circuit shown resembles a CMOS inverter in that it comprises a stack of two series-connected PMOS devices (PI, PO) and two series-connected NMOS devices (NI, NO), with the inputs common. The output is taken from the centre of the stack. As so far described the function would be that of a simple inverter. The provision of additional devices (NF, PF) provides a form of positive feedback.

(b) With V_{IN} at ground, NI is cut off, hence no current path is available in the stack. However, PI is highly conductive (in the non-saturated mode), and its drain is therefore at a virtual VDD potential. Hence VGS for PO is sufficient to bring it into its non-saturation region. There is thus a conductive pull-up to V_{DD}, and since the drain current in the NMOS devices is zero, there is negligible voltage drop across PI and PO. Hence the output voltage is:

$$V_{OH} = V_{DD}$$

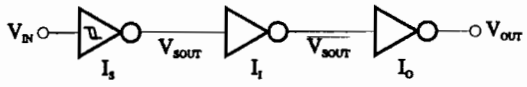
This would remain for V_{IN} between 0V and V_{TN}. By symmetry, if V_{IN} lay between V_{DD} and V_{DD}-$|V_{TP}|$, the output would lie at a low level, with conductive pull-down to 0V such that:

$$V_{OL} = 0$$

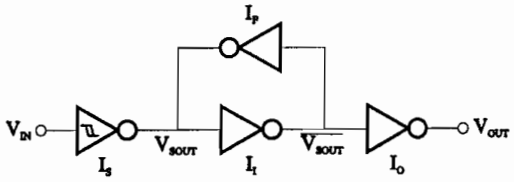
The purpose of the circuit is functionally an inverter. Comparing the input circuitry with that of a standard inverter, we see the input drives 4 gate electrodes (cf 2 in the inverter proper). For unit current comparability, the W/L ratio for the Schmitt transistors (being in series) must be twice those of the standard inverter. Assuming both designs use the same L value, it follows that the there are in the Schmitt gate twice as many transistors each of twice the area, so that the previous stage must drive about 4 times the capacitance of an inverter of equivalent drive strength.

Increasing the size of the Schmitt transistors to increase the drive capability could increase the input capacitance to an unmanageable level.

Hence, if a CMOS Schmitt inverter with large current drive is required, it is best to use the smallest practicable transistors in the Schmitt stage itself, but to follow it with a further inverter (or pair of inverters to achieve the correct polarity).



Buffered Schmitt Inverter



Buffered Schmitt inverter with feedback

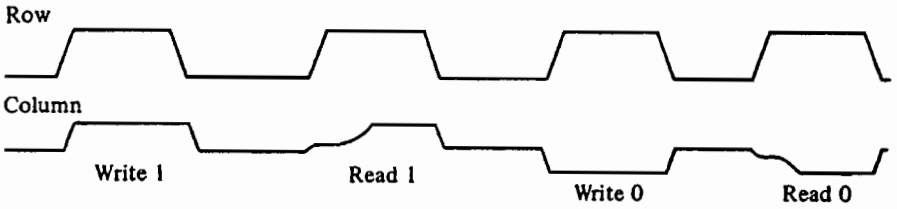
The dimensions of P2/N2 may be made greater than those of P1/N1 to achieve still greater drive capacity. A figure of 3× is commonly used.

Optionally the feedback inverter I_F may be incorporated. This applies positive feedback to the input of the first stage, improving the transient response when the input is extremely noisy. I_F must be made from transistors with lower current capability than P1 and N1 – typically their conductance might be 1/3 of the corresponding parameter for P1, N1, and is often referred to as a trickle inverter.

(c) (i) The diagram shows a dynamic memory cell. Data are stored as a presence or absence of a packet of electronic charge on capacitor C1. Transistor M1 serves as a switch to allow data to be input to the cell, and for data to be output from the cell via the column line.

Writing. The cell is selected by bringing the corresponding ROW line high making T1 conduct. A value is written to the capacitor C1 by forcing a high or low value on the corresponding COLUMN line. The ROW line is then brought low, isolating the cell.

Reading. The COLUMN line is initially precharged to a level midway between the two logic levels. The ROW line is brought high, causing the charge on C1 to be shared with that of the COLUMN line, C2, typically 20 or more times larger than C1. Thus the change in potential of the column line may be no more than a few tens of mV. This is sensed by a sensitive comparator (sense amplifier), one to every column line, whose reference input is connected to a 'dummy' column line also precharged to the standard level. Sense amplifier design is a very critical aspect of the overall circuit for reliable detection.



Timing diagram for Read and Write

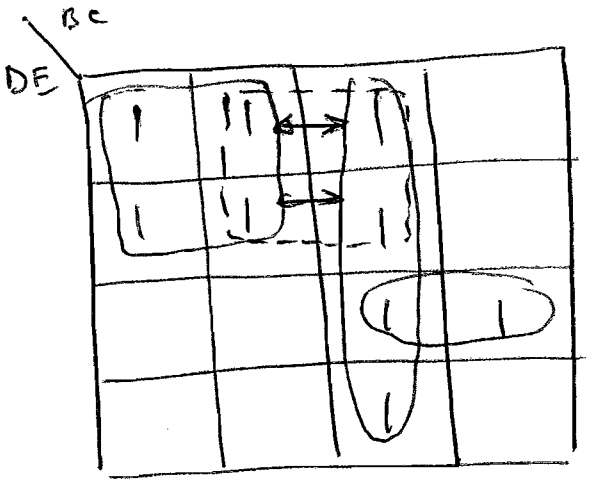
(ii) C1 is typically very small, o(30 fF) in order that the cell be compact. C2 is made as small as possible to maximise the potential sensed on reading, but since the COLUMN line has to serve a substantial number of cells, it is inevitably orders of magnitude greater. In some architectures the array of cells is split, doubling the number of column lines (and sense amplifiers) to limit C2.

Stored data must be regenerated every time it is read, as readout is destructive; and it must also be refreshed every few ms, since the stored charge is liable to leak away even if the cell is not accessed.

Examiner's note: this question was done by about half the candidates, and was on the whole reasonably done. Most knew the basic operating principle of the Schmitt trigger, but very few were able to explain how buffering the output could enhance the drive capability and the input characteristics. In the section on the dynamic memory, a number were uncertain of the origins of the capacitances observed. The most common misunderstanding was the charge-sharing phenomenon encountered when attempting to read data from the cell.

3. (a) $T = \sum (16, 17, 20, 21, 27, 29, 30, 31)$

$T = \sum 2^4 [0, 1, 4, 5, 11, 12, 13, 14, 15]$



Simplest SOP

$T = A[BC + \bar{B}\bar{D} + BDE]$

$= ABC + A\bar{B}\bar{D} + ABDE$

[3 %]

static hazards when adjacent 1's are not linked by the same 1-term.

$\begin{cases} A=1, B=0, C=1, E=0 & D=0 \to 1 \\ A=1, B=0, C=1, E=1 & B=0 \to 1 \end{cases}$

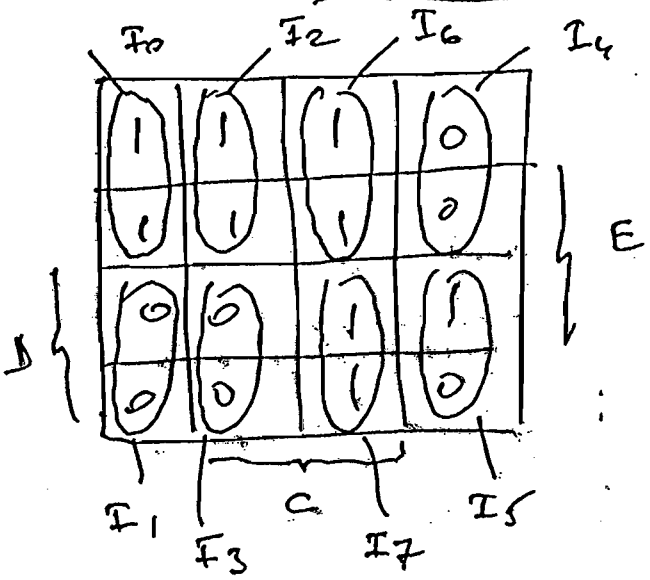
They can be corrected by coding $C\bar{D}$ in k-map

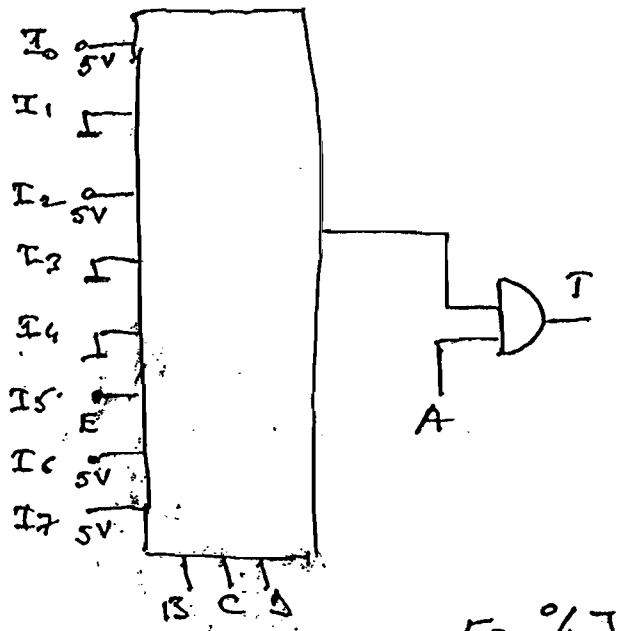
$T = ABC + A\bar{B}\bar{D} + ABDE + AC\bar{D}$

[10 %]

there are no dynamic hazards.

The implementation used for k-map for the 8-to-1 multiplexer.





$I_0 = 1$; $I_1 = 0$; $I_2 = 1$
$I_3 = 0$; $I_4 = 0$; $I_5 = E$
$I_6 = 1$; $I_7 = 1$

[20%]

(b) By inspection:

$$O_1 = \left[\overline{I_1 I_2} \cdot (I_1 + I_2)\right] \bar{C} + \overline{I_1 \cdot \bar{I}_2} \cdot (\bar{I}_1 + I_2) \cdot C$$

($\overline{I_1 I_2} = \bar{I}_1 + \bar{I}_2$)

$$O_1 = \left[(\bar{I}_1 + \bar{I}_2)(I_1 + I_2)\right] \underset{\text{XOR}}{\oplus} C = \boxed{I_1 \oplus I_2 \oplus C}$$

I_1	I_2	C	O_1
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

O_1 is the sum of bit I_1 and bit I_2 with C as the Cin from a previous addition.

So I_1 = LSB of A

I_2 = LSB of B

$\boxed{C = C_{in}}$ from another circuit.

$$O_2 = I_3 \oplus I_4 \oplus \underbrace{\left[\overline{I_1 + I_2} + \overline{I_1 I_2 + C} \right]}_{\text{call this } M}$$

$$M = (I_1 I_2 + C) \cdot (I_1 + I_2) = I_1 I_2 + C(I_1 + I_2)$$

$M = 1$ when (i) $I_1 = 1$, $I_2 = 1$

or (ii) either I_1 or $I_2 = 1$ and $C = 1$

That means M is the CARRY OUT BIT from the BIT 0 (LSB) ADDITION

$$M = C_{out}|_0$$

$$\boxed{O_2 = I_3 \oplus I_4 \oplus C_{out}|_0}$$

This is the sum of bit 1 of A and bit 1 of B.

By extrapolation and symmetry:

$$\boxed{\begin{aligned} O_3 &= I_5 \oplus I_6 \oplus C_{out}|_1 \\ O_4 &= I_7 \oplus I_8 \oplus C_{out}|_2 \\ D &= C_{out}|_3 = C_{out} \end{aligned}}$$

The circuit is a 4-BIT, PARALLEL BINARY ADDER with C_{in} and C_{out}.

[40%]

4.(c) • Multiplexers are suitable for single output functions, (preferably with few variables).

- ROMs are better for multiple-output functions but they become expensive and less efficient for a very high number of variables
- PLAs are good for multiple-output functions with lots of variables. There are expensive unless the number of variables are too high for a ROM. [20%]

(5) Unique sequences of inputs which lead to releasing the drink.

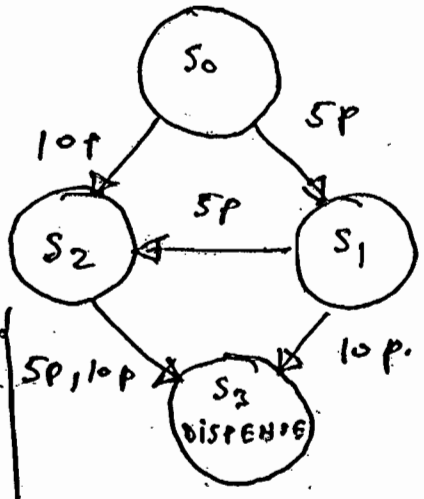
(1) 5p + 5p + 5p

(2) 5p + 5p + 10p (no next given)

(3) 5p + 10p.

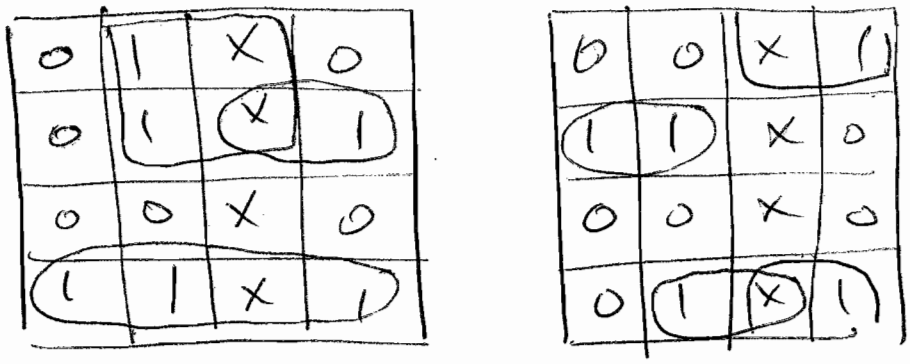
(4) 10p + 5p

(5) 10p + 10p.



Present State	Next state for 5p 10p 00 01 11 10				DISPENSE
S_0	00	00	10	01	0
S_1	01	01	11	10	0
S_3	11	00	00	00	1
S_2	10	10	11	11	0

k map for D_1 & D_2



$$D_1 = Q_1\bar{Q}_2 + 1op\,\bar{Q}_1 + 5p\,\bar{Q}_1 Q_2$$
$$D_2 = 5p\,\bar{Q}_2 + 1op\,Q_1\bar{Q}_2 + \overline{5p}\,Q_1 Q_2$$

OUTPUTS :

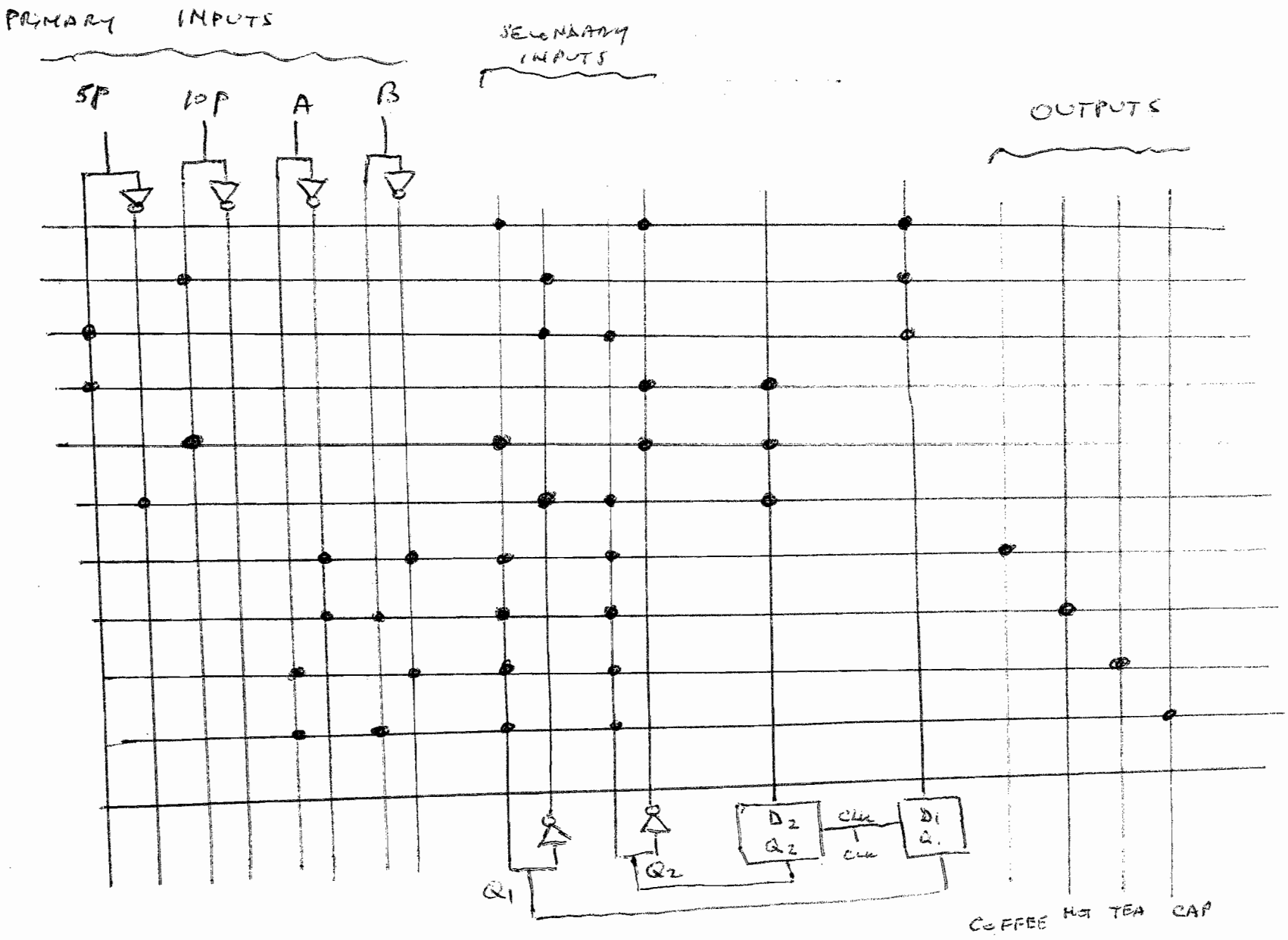
$$GFFEE = Q_1 Q_2 \bar{A}\bar{B}$$
$$HOT = Q_1 Q_2 \bar{A} B$$
$$tEst = Q_1 Q_2 A\bar{B}$$
$$CAL = Q_1 Q_2 AB$$

[3%]

see diagram next page

There are no essential hazards as 5p, 1op, A, B are inputted sequentially by hand. These inputs cannot change as fast as the outputs. The time for the secondary inputs (Q_1, Q_2, Disp) to be available at the input is orders of nano seconds. Primary inputs cannot change as fast.

[20%]


PRIMARY INPUTS
SECONDARY INPUTS
OUTPUTS
5P
10P
A
B
D_2
Q_2
D_1
Q_1
CLK
CLK
Q_2
Q_1
COFFEE
HOT TEA
CAP

[30%]

Module 3B2 – 2007 **Integrated Digital Electronics**

Numerical answers

1
(i) $NM_H = -1.1$ V, $NM_L = 0.6$ V (ii) $NM_H = 7.9$ V, $NM_L = 0.7$ V

2
$V_{OH} = V_{DD}$, $V_{OL} = 0$