ENGINEERING TRIPOS PART IIA

Friday 11 May 2007 2.30 to 4

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Give two main advantages and two main disadvantages of CMOS technology in the design of digital logic systems. Your answer may include references to: implementation, compactness, input and output levels, and drive capability, as well as any other factors you consider important. [30%]

(b) With the aid of a diagram, show how to determine the noise margins from the input and output logic levels V_{IL}, V_{IH}, V_{OL} and V_{OH}. [20%]

(c) The characteristics of bipolar and CMOS inverter gates from a certain manufacturer are given in Table 1 for a 10 V supply. The tabulated information shows input and output logic levels as well as the maximum gate input currents in the high and low states. A negative input current signifies a current which flows out from the gate's input terminal.

	V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{IHmax}	I_{ILmax}
Bipolar logic	**0.8 V**	**2.0 V**	**0.4 V**	**7.4 V**	**40 μA**	**-1.6mA**
CMOS logic	**1.0 V**	**8.5 V**	**0.1 V**	**9.9 V**	**0**	**0**

Table 1

Determine the noise margins that will apply when:

(i) a bipolar inverter drives a single CMOS inverter;

(ii) a CMOS inverter drives a single bipolar inverter.

Comment on these results. [30%]

How would you expect the noise margins to be affected in each case if twenty inputs were driven instead of one? State any assumptions made. [20%]

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2 (a) Briefly describe the principles of operation of a Schmitt inverter. Sketch a graph depicting a typical voltage transfer characteristic for a Schmitt inverter, and explain the significance of the output high-to-low transition and output low-to-high transition. How might such a gate be used in a digital system as a line receiver, and what advantages would this be expected to give? [30%]

(b) Figure. 1 shows the circuit schematic for a Schmitt inverter implemented as a CMOS circuit using MOS transistors PI, PO, PF, NI, NO and NF. The six transistors have corresponding device transconductances k_{PI}, k_{PO}, k_{PF}, k_{NI}, k_{NO} and k_{NF}. You may assume that all three NMOS transistors have threshold voltage V_{TN} and all three PMOS transistors have threshold voltage V_{TP}.

Determine the values of V_{OH} and V_{OL} expected at the output with normal logic levels applied at the input. [20%]

Explain why it is desirable to buffer the output of such a gate, and indicate how this might be achieved. [20%]

(c) Figure. 2 shows a simplified circuit of a memory cell based on a single MOS transistor M.

(i) Explain briefly the principle of operation, and with the aid of a timing diagram indicate how the operations of READ and WRITE would be carried out.

(ii) What is the significance of capacitances C_1 and C_2, and how do they interact with other essential circuit elements in a practical memory circuit to influence its performance? [30%]

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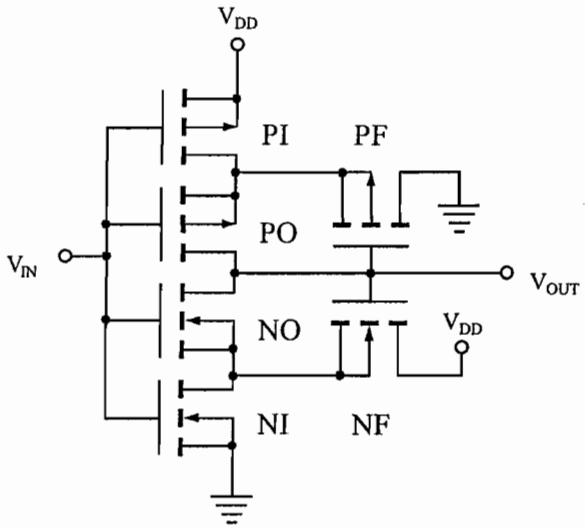

Fig. 1

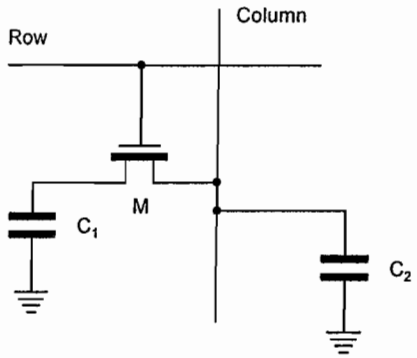

Fig. 2

(TURN OVER

3 (a) Find the simplest sum-of-products (SOP) expression for the following function:

$$T = \Sigma (16, 17, 20, 21, 27, 28, 29, 30,31)$$ [30%]

For the simplest SOP form, determine if there are any potential static or dynamic hazards and if there are, derive a simple expression that has no hazards. [10%]

Implement the function above using a single 8 to 1 multiplexer and a single two-input logic gate. [20%]

(b) Figure 3 shows the logic gate implementation of a multiple-output combinational circuit. Determine what function the circuit performs and explain briefly the operation of the circuit as a function of the inputs I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, C. The outputs of the circuit are O_1, O_2, O_3, O_4 and D. *[Hint: Calculate first O_1]* [40%]

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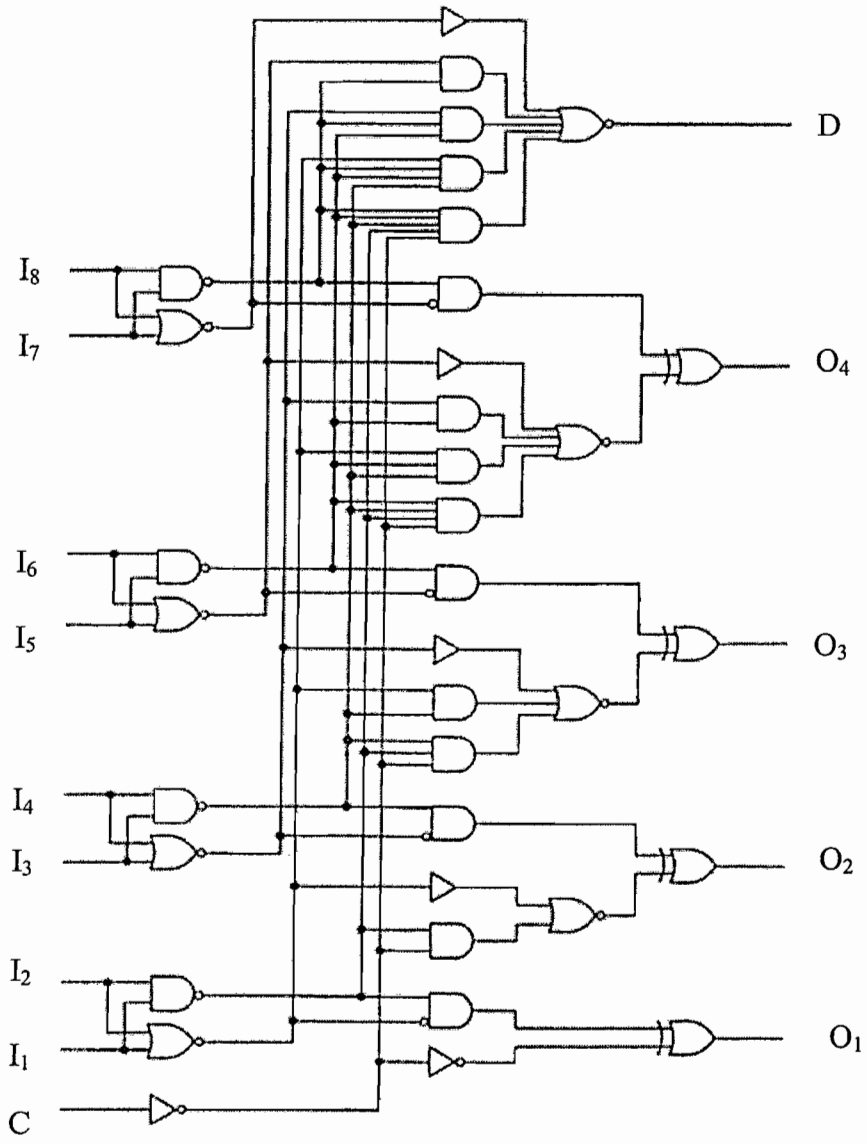

Fig. 3

4 (a) Briefly discuss the advantages and disadvantages of implementing logic functions with ROMs, Multiplexers and PLAs . [20%]

(b) The diagram of a vending machine that dispenses four drinks, coffee (COFFEE), Hot chocolate (HOT), Tea (TEA) and Cappuccino (CAP) is shown in Fig 4. The machine has a single coin slot and accepts 10p and 5p, one coin at a time. When 15 pence is received the drink dispensing mechanism (DISPENSE) is activated and one of the four drinks is released as a function of the control inputs A and B (coming from the keypad) as shown in the Table 2. For simplicity assume that the user selects the type of drink before inserting any coins. State any other assumptions made.

Design the control logic for the vending machine that dispenses a drink for 15 pence in coins and selects one of the 4 outputs as shown in Table 2. Draw the state diagram and state table showing the allocation of states. [30%]

Draw the circuit implementation of the control using a single PLA and D bistables. [30%]

Comment on the existence of essential hazards, if any, in the implemented circuit. [20%]

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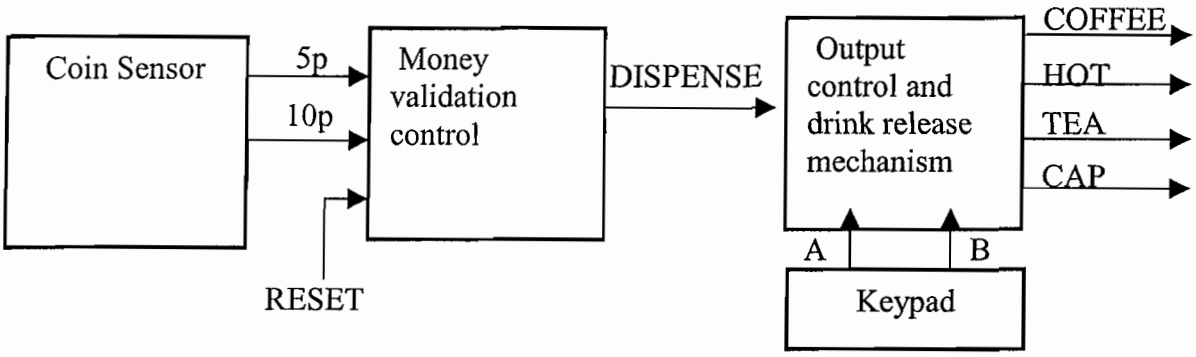

Fig. 4

INPUTS AB	OUTPUTS
00	COFFEE
01	HOT (CHOCOLATE)
10	TEA
11	CAP(PUCCINO)

Table 2

END OF PAPER

Module 3B2 – 2007 **Integrated Digital Electronics**

Numerical answers

1
(i) $NM_H = -1.1$ V, $NM_L = 0.6$ V (ii) $NM_H = 7.9$ V, $NM_L = 0.7$ V

2
$V_{OH} = V_{DD}$, $V_{OL} = 0$