1) (A) TEXT BOOK 382 2008 Dr A Ferrari (5)

(a) STATIC-1 HAZARD IS WHEN A SIGNAL GIVEN BY $(y + x\bar{z})$ SHOULD BE HIGH FOR BOTH CONDITIONS OF x - AND YET IS LOW BRIEFLY DUE TO THE INVERTOR DELAY FORMING $\bar{x}$

A FUNCTIONAL HAZARD IS CAUSED BY CHANGES OF 2 OR MORE INPUT VARIABLES AT ATIME-

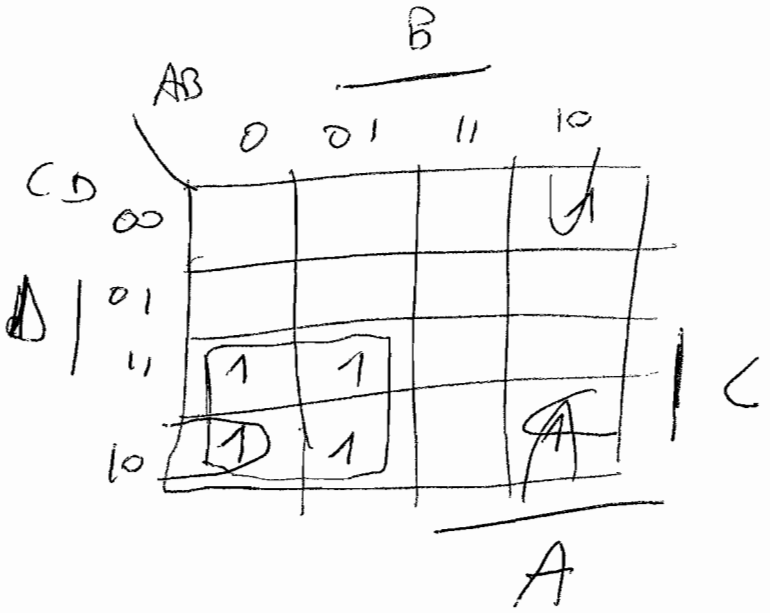
A DYNAMIC HAZARD IS WHERE A SINGLE OUTPUT CHANGE IS EXPECTED AND YET $\sqcup\sqcap$ OR $\sqcap\sqcup$ IS FOUND. MORE THAN ONE INPUT CHANGES AT A TIME

AN ESSENTIAL HAZARD IS CAUSED BY A RACE BETWEEN AN INPUT SIGNAL CHANGE AND AN OUTPUT CHANGE

(b) A POS EXPRESSION WILL NOT CONTAIN STATIC AND DYNAMIC HAZARDS IF:

1. ALL ADJACENT "0" SQUARES IN THE K-MAP OF THE COMPLEMENT OF THE SWITCHING FUNCTION ARE COVERED BY A COMMON O-TERM
2. THERE ARE NO O-TERMS THAT CONTAIN BOTH A VARIABLE AND ITS COMPLEMENT

$T = \Sigma(2, 3, 6, 7, 8, 10)$ (2)



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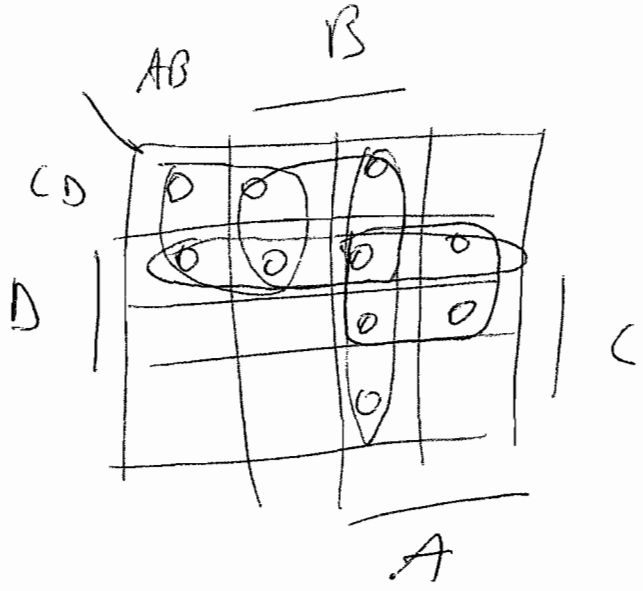


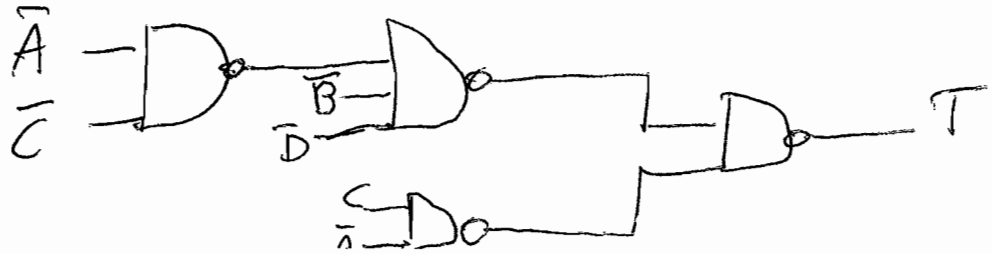
NOR

1) NAND: GOT $\overline{T}$ BY MAPPING "1"S IN THE K-MAP. MAKE SURE THAT ALL ADJACENT 1s ARE COVERED BY A COMMON LOOP

$$\overline{T} = C\bar{A} + A\bar{B}\bar{D} + \bar{B}\bar{D}C$$

$$T = C\bar{A} + \bar{B}\bar{D}(A+C) = \overline{C\bar{A} \cdot \bar{B}\bar{D}(A+C)}$$

$$= \overline{C\bar{A}} \cdot \overline{\bar{B}\bar{D}} \cdot \overline{\bar{A}C}$$



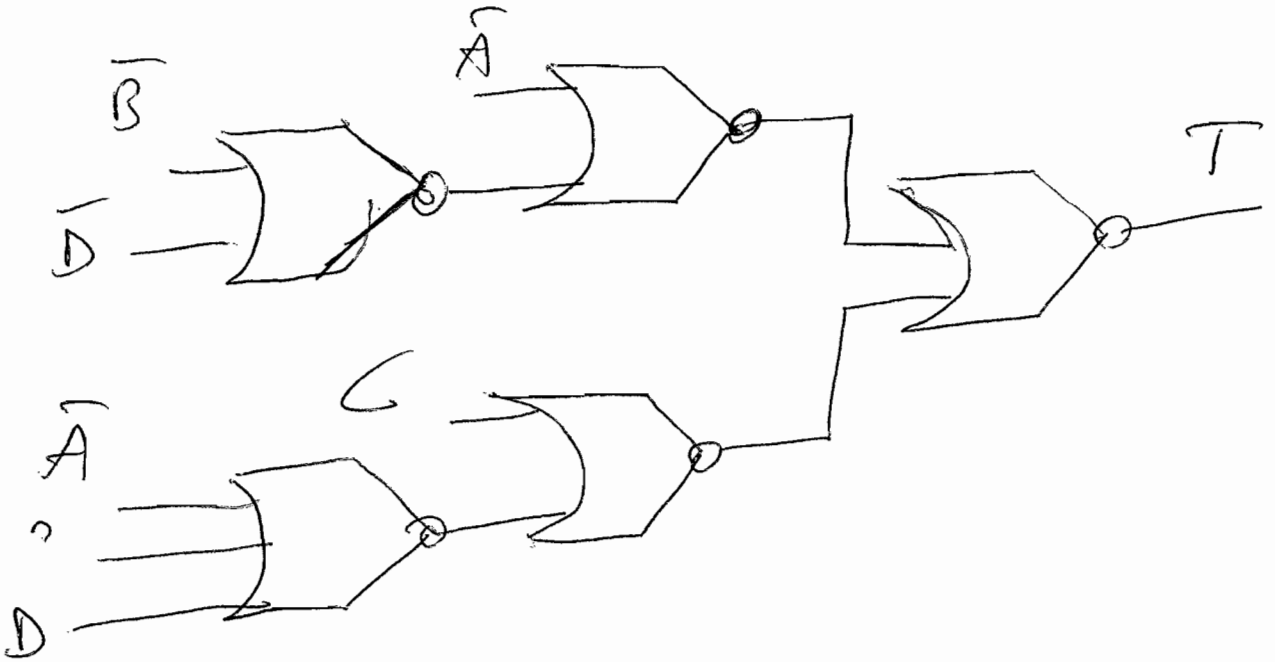
1) (b) (ii)

NOR NAND GATES FOR $\overline{T}$

$$\overline{T} = DA + \bar{C}\bar{D} + AB + \bar{A}\bar{C} + B\bar{C}$$

$$F = \overline{A(B+D) + \bar{C}(D + \bar{A} + B)} =$$

$$= \overline{\overline{A} + \overline{B+D}} + C + \overline{(\bar{A} + B + D)}$$



c) TABULAR METHOD - ORDER TERMS IN (6)
NO OF VARIABLES HIGH.

ONE VALUE

2	0010	✓
8	1000	✓
3	0011	✓
5	0101	✓
6	0110	✓
9	1001	✓
10	1010	✓
7	0111	✓
11	1011	✓

2,3	001x	✓	(2,3)(6,7) } 2 lit
2,6	0x10	✓	(2,6)(3,7) } 2 lit
2,10	x010	✓	(P)
8,9	100x	✓	(2,3)(10,11) } 1 lit
8,10	10x0	✓	(2,10)(3,11) } 1 lit
3,7	0x11	✓	
3,11	x011	✓	
5,7	01x1	(P)	(S)
6,7	011x	✓	(8,9), (10,11) } 1 lit
8,11	10x1	✓	(8,10), (9,11) } 1 lit
10,11	101x	✓	

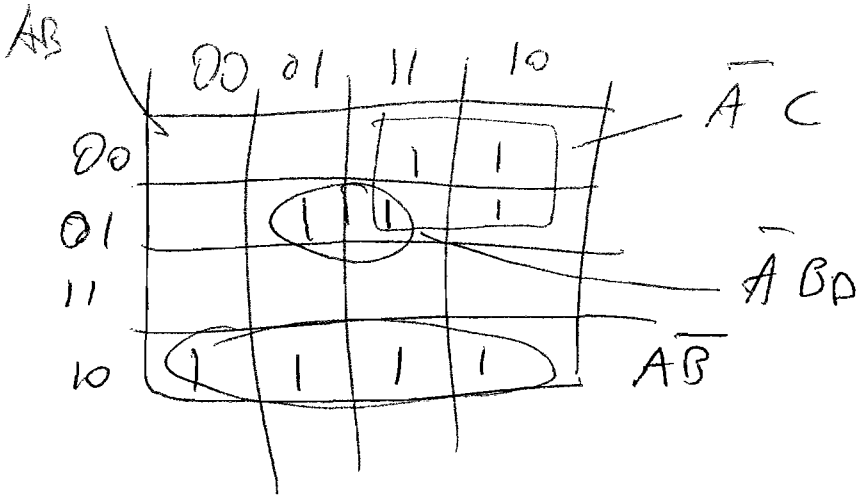
(Q)

THERE ARE 4 PIs, P Q R S

	2	3	5	6	7	8	9	10	11	01x
(P) 5,7 =			●		●					
(Q) = 2,3,6,7 OR 1 lit	●	●		●						
(R) 2,3,10,11	●	●						●	●	
(S) = 8,9,10,11 = 10x x						●	●	●	●	

(P) P, Q, S ARE ESSENTIAL

$$T = \bar{A}BD + \bar{A}C + A\bar{B}$$ (SP)



(5)

$$\bar{F} = A.B + \bar{A}.\bar{B}\bar{C} + \bar{A}\bar{C}\bar{D}$$

(OR $B\bar{C}\bar{D}$)

$$T = \overline{\bar{A}.B} \cdot \overline{(\bar{A}B\bar{C})} \cdot \overline{(\bar{A}\bar{C}\bar{D})}$$

$$= (\bar{A}+\bar{B}) \cdot (A+B+C) \cdot (A+C+D)$$

(OR $\bar{B}+C+D$)

~~(A)~~

(A) A MULTIPLEXER WITH CONTROL LINES P Q, YIELDS AN OUTPUT (1)

$$D_0\bar{P}\bar{Q} + D_1\bar{P}Q + D_2P\bar{Q} + D_3PQ$$

SELECTING THE FOUR DATA LINES D_0, D_1, D_2, D_3 IN TURN AS PQ CHANGES

WE NOTE THAT A, B ARE USED IN ALL THE TERMS IN THE DESIRED FUNCTION

$$Y = \bar{A}\cdot\bar{B} + A\bar{B}\bar{C} + ABC$$

So put $A = P$, $B = \varphi$

$$= 1\,\bar{P}\bar{\varphi} + \bar{C}P\bar{\varphi} + CP\varphi \quad (2)$$

Comparing (1) and (2)

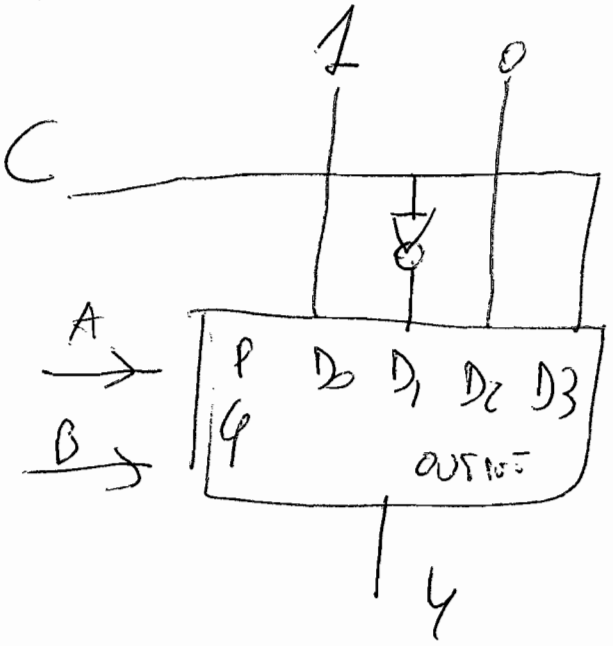
$D_0 = 1$

$D_1 = \bar{C}$

$D_2 = 0$

$D_3 = C$

&



If control line selection $B = P$, $A = \varphi$

(inputs D_1 & D_2 skipped so $D_0 = 1$, $D_1 = 0$, $D_2 = \bar{C}$, $D_3 = C$)

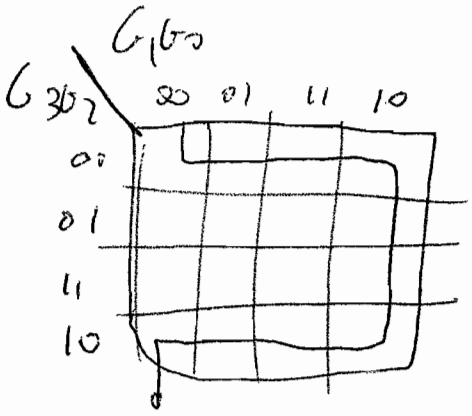
26)

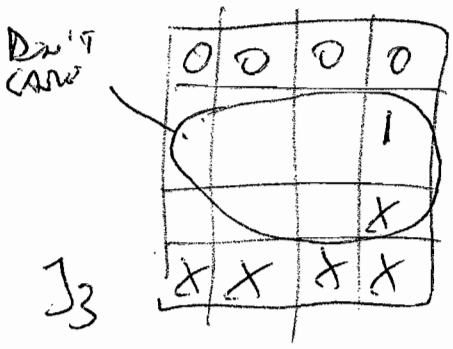
IN THE MOORE SEQUENTIAL NETWORK THE PRIMARY OUTPUTS, Z ARE A FUNCTION OF THE PRESENT STATES ONLY $Z = f(\varphi)$
WHEREAS IN THE MEALY SEQUENTIAL NETWORK THE PRIMARY OUTPUTS ARE A FUNCTION OF BOTH THE PRESENT STATES AND THE PRIMARY INPUTS $Z = f(A, \varphi)$. THE CHOICE OF THE NETWORK IS ONE OF CONVENIENCE AND PERSONAL PREFERENCE, BUT MEALY MODEL IS MORE GENERAL THE MOST SIGNIFICANT OPERATIONAL DIFFERENCE BETWEEN THE TWO IS THAT WHEN A SET OF INPUTS IS APPLIED TO THE MOORE NETWORK, THE RESULTING OUTPUTS DO NOT APPEAR UNTIL AFTER THE CLOCK PULSE CAUSES THE FLIP-FLOPS TO CHANGE STATE

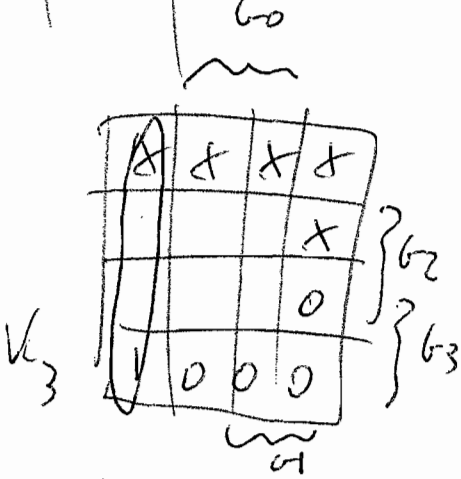
9)

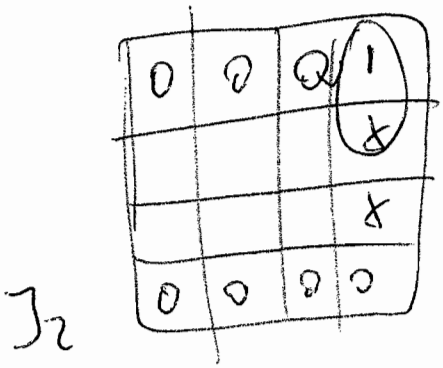
(7)

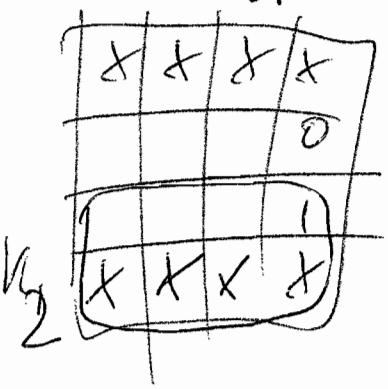
0000	0001	0x	0x	0x	1x
0001	0011	0x	0x	1x	x0
0011	0010	0x	0x	x0	x1
0010	0110	0x	1x	x0	0x
0110	1110	1x	x0	x0	0x
1110	1010	x0	x1	x0	0x
1010	1011	x0	0x	x0	1x
1011	1001	x0	0x	x1	x0
1001	1000	x0	x0	0x	x1
1000	0000	x1	0x	0x	0x

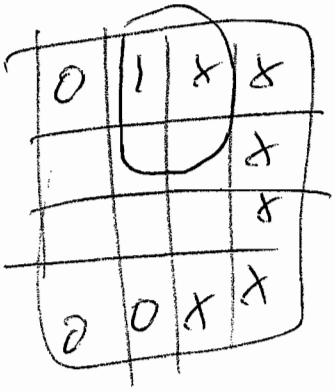


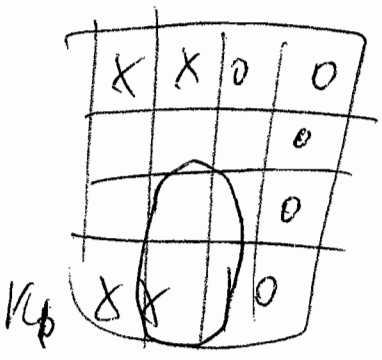


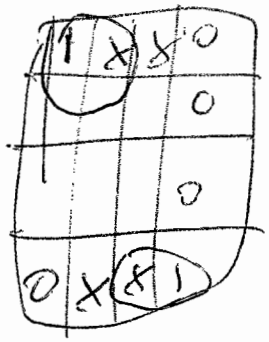




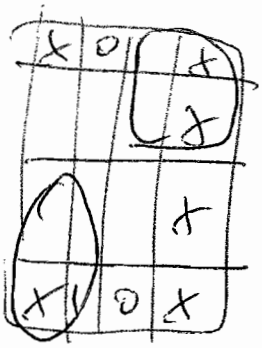








J_0



K_0

$$\begin{cases} J_3 = G_2 \\ K_3 = \bar{G_0} \cdot \bar{G_1} \end{cases}$$

$$\begin{cases} J_2 = \bar{G_3}\, G_1\, G_0 \\ K_2 = G_3 \end{cases}$$

$$\begin{cases} J_1 = \bar{G_3}\, G_0 \\ K_1 = G_3\, G_0 \end{cases}$$

$$\begin{cases} J_0 = \bar{G_3}\, \bar{G_1} + G_3\, \bar{G_2}\, G_1 \\ K_0 = G_3\, \bar{G_1} + \bar{G_3}\, G_1 \end{cases}$$

ONLY J_0 AND K_0 HAVE OR

FROM DE MORGAN

$$J_0 = \overline{\left(\bar{G_3}\, \bar{G_1}\right) \cdot \left(G_3\, \bar{G_2}\, G_1\right)}$$

$$K_0 = \overline{\overline{\left(G_3 \bar{G_1}\right)} \cdot \overline{\left(\bar{G_3}\, G_1\right)}}$$

Qn A

(a) Historically logic circuit development began with bipolar devices operating between saturation and cut-off. Available process technologies encouraged this development in an evolutionary rather than revolutionary way. For saturating bipolar technology:

Advantages:

- superiority over passive (e.g. diode-based) logics
- technological simplicity
- adequately suited to integration
- some scope for enhancement (e.g. use of schottky diode technology)

Disadvantages:

- high device count per function
- high power consumption
- low input resistance
- long propagation times
- limited enhancement potential via scaling

The main problem that had to be surmounted was the undesirable switching delay as devices came out of saturation. This was partly resolved by use of Schottky transistors. Nonetheless, TTL, S/LS TTL, ALS TTL were the primary technology on which much of the emergence of digital computing depended. Fastest logics ran at c. 100 MHz and required a fixed 5V supply. The limited switching speed was circumvented with the introduction of current-mode or non-saturating logic e.g. ECL.

Advantages

- very high speed, to > 1GHz in recent forms
- constant power consumption (approx) leading to:
- good overall noise characteristics

Disadvantages

- very high consumption
- poorly suited to large-scale integration

The introduction of ion implantation facilitated the full development of complementary MOS technology, allowing accurate positioning of n dopants in p substrates and v.v. For CMOS:

Advantages

- very low consumption for LF applications
- very good noise immunity (up to 0.4 VDD for inverter)
- fully restored logic outputs, 0V and VDD
- operable over range of supply voltages
- gate inputs draw no current, easy to drive
- highly suited to integration
- scales well (consumption & speed improve as devices shrink)
- usable up to about 60GHz

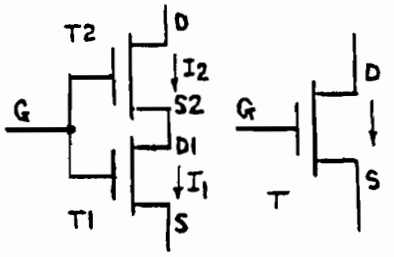
Disadvantages

- comparatively poor drive capability
- not as fast as best bipolar forms for significant loads
- sensitivity to static breakdown
- consumption increases with operating frequency > 1GHz
- liability to destructive latch-up (poor design or peripheral failures)

With CMOS the dominant mode of energy loss is dynamic dissipation as nodal capacitances are charged/discharged. Straightforward approaches to logic involve multiple devices and significant nodal capacitances, so much effort has gone into circuit abstraction. The excellent drive capability of bipolar is put to good use in BiCMOS which has superior performance when driving significant loads. The recent emergence of Ge-doped Si semiconductors is leading towards still greater speed improvements up to about 100 GHz is promised by this approach. The use of III/V semiconductors, e.g. GaAs in MESFETS has offered propagation delays o(1 ps) but so far large scale integration has not been practicable.

(b) As all devices are operating in non-saturation, we can write for I_2 in T_2:

$$I_2 = \frac{k'}{2}\frac{W}{L_2}\left[2(V_{GS2} - V_T)V_{DS2} - V_{DS2}^2\right]$$



Hence $I_2 \frac{2L_2}{k'W} = \left[2(V_{GS2} - V_T)V_{DS2} - V_{DS2}^2\right]$ (1)

Similarly for I1 in T1

$$I_1 \frac{2L1}{k'W} = \left[2(V_{GS} - V_T)V_{D1S} - V_{D1S}^2\right] \quad (2)$$

Note that: $V_{GS2} = V_{GS} - V_{D1S}$ and $V_{DS2} = V_{DS} - V_{D1S}$; substitute (2) into (1)

$$I_2 \frac{2L_2}{k'W} = \left[2(V_{GS} - V_{D1S} - V_T)(V_{DS} - V_{D1S}) - (V_{DS} - V_{D1S})^2\right]$$

$$= [2(V_{GS} - V_T)V_{DS} - 2(V_{GS} - V_T)V_{D1S} - 2V_{D1S}V_{DS} + 2V_{D1S}^2 + V_{DS}^2 + 2V_{DS}V_{D1S} + V_{D1S}^2]$$

$$= [(2(V_{GS} - V_T)V_{DS} + V_{DS}^2) - (2(V_{GS} - V_T)V_{D1S} - V_{D1S}^2)]$$

By inspection, the second term inside the [] square brackets is equivalent to the RHS of (2). So substituting:

$$I_2 \frac{2L_2}{k'W} = \left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right] - I_1 \frac{2L_1}{k'W}$$

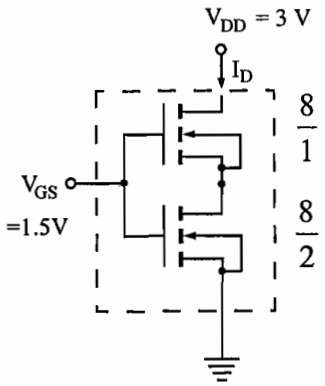
But by Kirchhoff $I_2 = I_1 = I$, say. Hence,

$$\frac{2I(L_1 + L_2)}{k'W} = \left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right], \text{ which gives}$$

$$I = \frac{k'}{2}\frac{W}{L_1 + L_2}\left[2(V_{GS} - V_T)V_{DS} + V_{DS}^2\right]$$

By inspection, this is the current that would flow in a single device T of width W and length $L_2 + L_1$, and whose electrode voltages are V_{GS}, V_{DS} as shown.

(c) From above, the equivalent circuit is:



For the n-type, (from above) $k_n = \frac{k_n' W}{L} = \frac{8 \times 10}{2}$ = 40 μA/V²

For the p-type, $k_p = \frac{k_p' W}{L} = \frac{(4+4) \times 5}{1}$ = 40 μA/V²

Hence, by symmetry, $V_{out} = V_{DS} = V_{DD}/2 = 1.5$ V,
and for each transistor, $V_{DS} > V_{GS} - V_T$

And $I_D = \frac{k}{2}(V_{GS} - V_T)^2 = 40(1.5 - 0.5) = 40$ μA

Qn B

(a) In ECL the transistors are configured as a form of differential amplifier in which current is steered between one member of the differential pair (representing logic 0), and the other member (representing logic 1). Thus the net current in the tail remains reasonably constant. Current is controlled by applying inputs symmetrically disposed about a carefully defined point in the active region determined by an accurate reference voltage applied to the base. The reference voltage is generated on-chip using a circuit that is stable and temperature-compensated. The logic output swing of the circuit is also symmetrical about the reference, and it is small enough to ensure that with the loads provided, no transistor enters saturation. Emitter followers are incorporated to protect the sensitive differential pair from external loading effects and to give large fan-out. In this way the objectionable time delays associated with saturating bipolar logic may be avoided, but the constant significant current drain leads to large power consumption.

(b) The required logic swing, being $V_R \pm 0.4$ V, is symmetric as described above. The logic levels are: $V_{OH} = -1.2 + 0.4 = -0.8$ V, and $V_{OL} = -1.2 - 0.4 = -1.6$ V . In the calculations that follow, all base currents are ignored, i.e. assumed to be zero. This implies that $I_C = I_E$ in all devices.

We begin by determining suitable values for R_1 and R_2 such that the two emitter follower transistors provide the correct V_{OH}. For maximum speed we operate these devices with the highest allowable emitter current I_E of 5 mA.

$$\boldsymbol{R_1 = R_2} = \frac{V_{OH} - V_{EE}}{I_E} = \frac{-0.8 + 5.2}{5 \times 10^{-3}} = \mathbf{0.88\ k\Omega}$$

Next determine the value for R_E by considering the case where T_1 is *on* (conducting more than T_2), with $V_{B1} = V_{OH}$. Again for speed we allow I_{E1} to be the maximum permitted value of 5 mA. Hence:

$$\boldsymbol{R_E} = \frac{V_{OH} - V_{BE1} - V_{EE}}{I_{E1}} = \frac{-0.8 - 0.8 + 5.2}{5 \times 10^{-3}} = \mathbf{0.72\ k\Omega}$$

R_{C1} is then calculated assuming that V_{O1} produces the correct value of V_{OL}.

$$\boldsymbol{R_{C1}} = \frac{V_{CC} - (V_{OL} + V_{BE3})}{I_{E1}} = \frac{0 + 1.6 - 0.8}{5 \times 10^{-3}} = \mathbf{0.16\ k\Omega}$$

When T_2 is *on*, its current is set by the reference voltage $V_R = -1.2$ V applied to its base:

$$I_{E2} = \frac{V_R - V_{BE2} - V_{EE}}{R_E} = \frac{-1.2 - 0.8 + 5.2}{0.72 \times 10^3} = 4.44\ \text{mA}$$

Finally, R_{C2} is determined knowing I_{E2}, requiring V_{O2} to be V_{OL}.

$$\boldsymbol{R_2} = \frac{V_{CC} - (V_{OL} + V_{BE4})}{I_{E2}} = \frac{0 + 1.6 - 0.8}{4.44 \times 10^{-3}} = \mathbf{0.18\ k\Omega}$$

(c) The voltage transfer characteristic is shown below. The transition is centred upon V_R, and is stated to be of width 200 mV. The output swing is likewise centred on V_R but has greater amplitude, of ± 0.4 V which is ample to drive a succeeding ECL stage effectively. Formally, the noise margins may be evaluated, and these can be seen to be 0.3 V for both the high and the low state.

$V_{OH} = -0.8$ V $\qquad$ $V_{OL} = -1.6$ V

$V_{IH} = -1.1$ V $\qquad$ $V_{IL} = -1.3$ V

$NM_H = V_{OH} - V_{IL} = -0.8 + 1.1 = 0.3$ V

$NM_L = V_{IL} - V_{OL} = -1.3 + 1.6 = 0.3$ V